

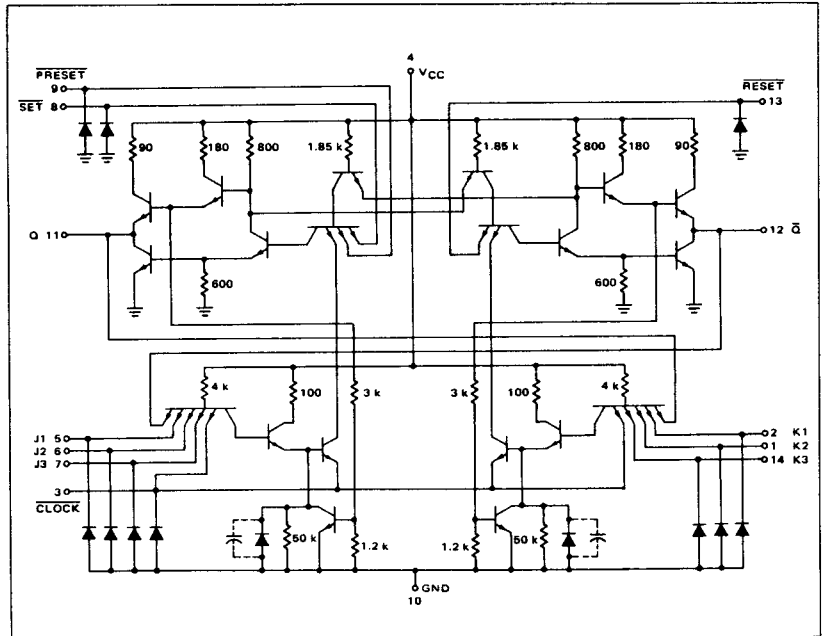
MC2125 • MC2175
MC2025 • MC2075

The MC2025, MC2075, MC2125, and MC2175 are clocked flip-flops that toggle at 50 MHz, trigger on the negative edge of the clock pulse, and perform the J-K logic function. Each flip-flop has an AND-input gating configuration consisting of three J inputs ANDed together and three K inputs ANDed together. The multiple J and K inputs minimize the requirements for external gating in counters and certain other applications. A direct SET, PRESET, and RESET are also available. These devices are pin compatible with the MC2109 series of devices. Electrical differences include input loading factors for the SET, PRESET, and RESET inputs which are approximately twice the loading factors of the MC2109 series.

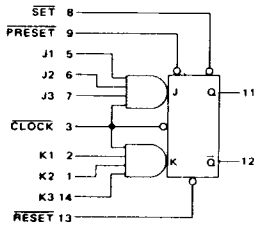
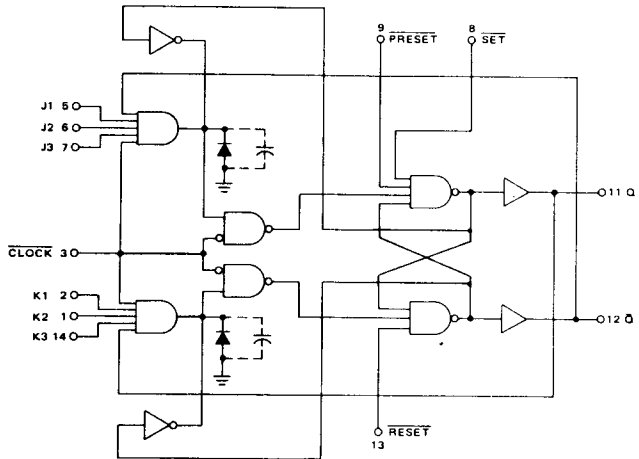
Information is changed on the J and K inputs while the clock is in the low state, since the inputs are inhibited in this condition. Information is transferred into a temporary memory when the clock goes to a high state. When the clock returns low, the information is transferred to the bistable section and the Q and \bar{Q} outputs respond accordingly. The information on the J and K inputs should not be changed while the clock is high.

Each flip-flop can be set or reset directly by the direct SET, PRESET, or RESET inputs. Since these flip-flops are charge-storage devices, there is a restriction on the clock fall time that must be observed.

TYPE NO.	INPUT LOADING FACTOR			(I_f)			OUTPUT DRIVE (I_{OL})	TEMPERATURE RANGE
	CLOCK	SET PRESET RESET	J,K	CLOCK	SET PRESET RESET	J,K		
MC2125 MC2175	1.0	1.2	0.67	(-1.33 mA)	(-2.4 mA)	(-1.33 mA)	11 MC2100 series Gates (22.0 mA) 6 MC2100 series Gates (12.0 mA)	-55°C to +125°C
MC2025 MC2075	1.0	1.2	0.67	(-1.66 mA)	(-2.8 mA)	(-1.66 mA)	9 MC2000 series Gates (22.5 mA) 5 MC2000 series Gates (12.5 mA)	0°C to +75°C



LOGIC DIAGRAM



J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Where $J = J1 + J2 + J3$
 $K = K1 + K2 + K3$

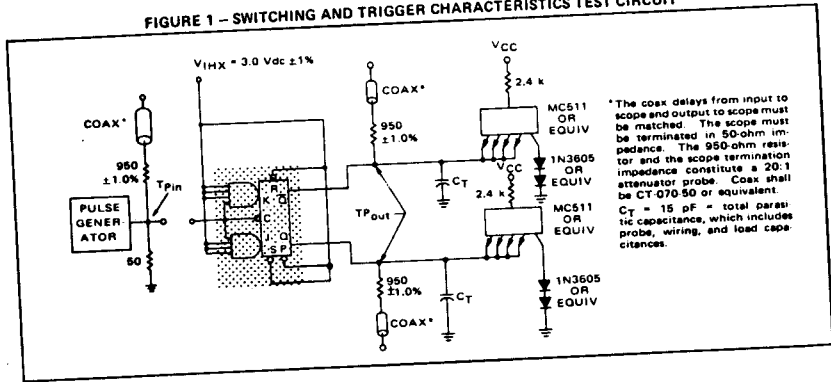
Total Power Dissipation = 50 mW typ/pkg
 Switching Times:
 $t_{pd} = 11$ ns typ
 $t_{pd} = 9.0$ ns typ
 Operating Frequency = 70 MHz typ

OPERATING CHARACTERISTICS

Clock fall time ≤ 100 ns.
 Triggers on clock pulse widths ≥ 10 ns.
 Provides direct SET, PRESET, and RESET inputs. The application of a "0" state to the SET or PRESET will cause Q to go to the "1" state; application of a "0" state to the RESET will cause Q to go to the "0" state. The clock must be in the low state when these functions are performed. Since there is almost no post time associated with these devices, the direct inputs can be applied 15 ns after the clock signal has fallen.
 Data at the J and K inputs must be present before the clock goes to a high state. If the information on the J and K inputs is changed while the clock is in a high state, the flip-flop will require typically $1.0 \mu\text{s}$ to recognize a "1" state to "0" state information change on the J and K terminals. The flip-flop typically requires 10 ns to recognize a "0" state to "1" state change.

By using an internally cross-coupled network and buffered outputs, the propagation delays (t_{pd} and t_{pqs}) are nearly symmetrical. The outputs are capable of driving high capacitive loads without degrading the frequency of operation.
 Negative edge triggering - When the clock goes from the high state to the low state, the information in the temporary storage section is transferred to the bistable network and the data appears at the Q and \bar{Q} outputs. While the clock is in a low state, the J and K terminals are inhibited.
 Unused J and K inputs should be tied to the clock or to a voltage between 2.0 and 5.0 Vdc. Other unused inputs should be tied to a voltage between 2.0 and 5.0 Vdc.
 The maximum allowable clock skew time is 9.0 ns. This is the total of the minimum time to recognize a "0" state to "1" state change (4.0 ns) and the minimum propagation delay (5.0 ns).

FIGURE 1 - SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



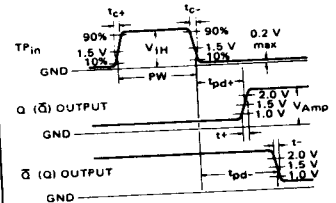
SWITCHING TIMES

TEST	TEST SYMBOL	INPUT PULSE	MIN	MAX	UNIT
Delay Time Off	t_{pd+}	V	-	15	ns
Delay Time On	t_{pd-}	V	-	15	ns
Rise Time	t_r^+	V	-	4.0	ns
Fall Time	t_f^-	V	-	2.5	ns
Amplitude	V_{amp}	V	3.0	-	Volt

WORST-CASE TESTS
 (Device must toggle with each clock pulse)

TEST	SYMBOL	LIMITS	INPUT CONDITIONS
Toggle Frequency	f_{Tog}	50 MHz max	W
Pulse Width	PW	10 ns min	X
Input High Voltage	V_{IH}	1.8 V min	Y
Fall Time	t_f	100 ns max	Z

VOLTAGE WAVEFORMS AND DEFINITIONS



INPUT PULSE CONDITIONS

SYMBOL	V	W	X	Y	Z	UNIT
PRF	5.0	50	5.0	5.0	1.0	MHz
PW	10	10	10	10	200	ns
t_r^+	≤ 2.0	≤ 0.0	≤ 0.0	≤ 0.0	≤ 50	ns
t_f^-	≤ 2.0	≤ 0.0	≤ 0.0	≤ 0.0	100	ns
V_{IH}	3.0	3.0	3.0	2.4	3.0	Volt

FIGURE 2 - J-K TERMINAL CHARACTERISTICS TEST CIRCUIT

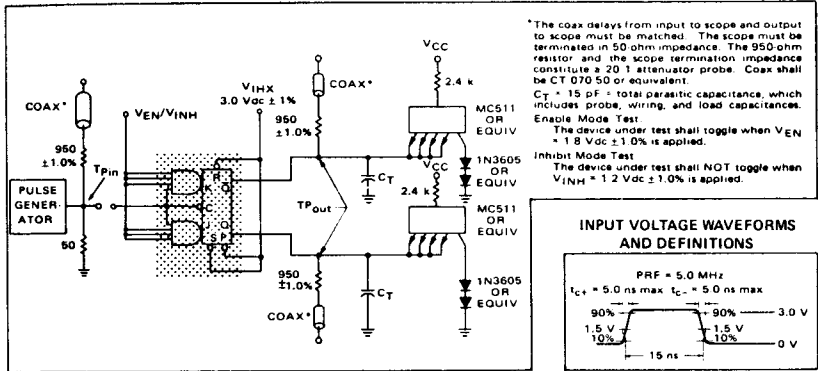
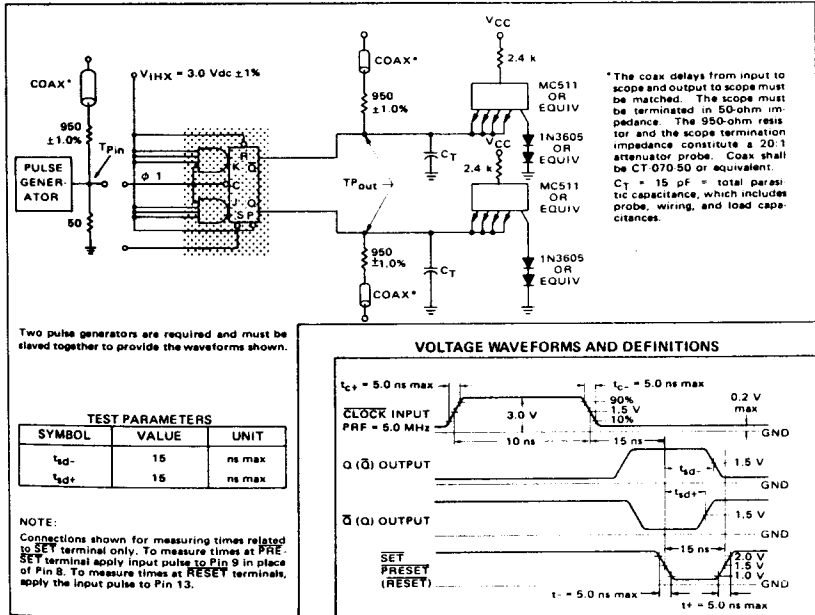


FIGURE 3 - SET-RESET-PRESET TERMINAL CHARACTERISTICS TEST CIRCUIT



Pin-out and Package Information

Table 3-4 DSP56001A Identification by Signal Name (Continued)

Signal Name	132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.	Signal Name	132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.
WT	45	L13	nc	103	
X/Y	48	N13	nc	107	
XTAL	126	A6	nc	110	
nc	3		nc	116	
nc	4		nc	117	
nc	7		nc	122	
nc	17		nc	125	
nc	18		nc	132	
nc	21				

Power and ground pins have special considerations for noise immunity. See the section **Design Considerations**.

Table 3-5 DSP56001A Power Supply Pins

132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.	Power Supply	Circuit Supplied
63	L8	VCCN	Address Bus Buffers
64			
55	L6	GNDN	
56	L9		
73			
74			