Description

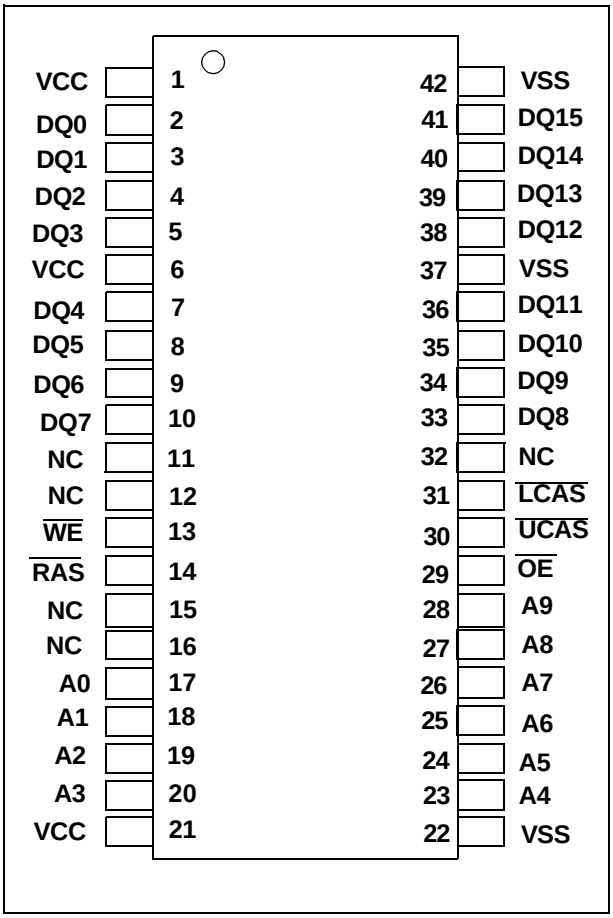
The device CMOS Dynamic RAM organized as 1,048,576 words x 16 bits with extended data out access mode. It is fabricated with an advanced submicron CMOS technology and designed to operate from a single 5V only or 3.3V only power supply. Low voltage operation is more suitable to be used on battery backup, portable electronic application. Self-refresh is supported and CBR cycles are being performed. It is packaged in JEDEC standard 42-pin 400mil SOJ and 50(44)-pin 400mil TSOPII.

Features

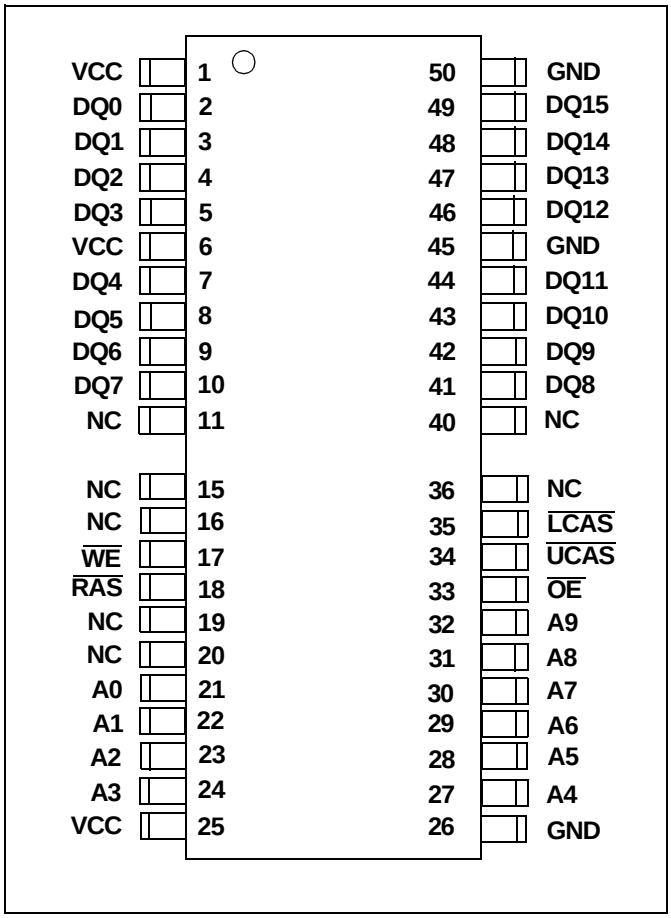
- Single 5V or 3.3V only power supply
- High speed t_{RAC} access time: 50/60ns
- Extended-data-out (EDO) page mode access
- I/O level: TTL compatible (Vcc = 5V)
  LVTTL compatible (Vcc = 3.3V)
- 4 refresh modes:
  - $\overline{RAS}$ only refresh
  - $\overline{CAS}$ - before - $\overline{RAS}$ refresh
  - Hidden refresh
  - Self-refresh
- Refresh interval:
  - $\overline{RAS}$ only refresh, $\overline{CAS}$ - before - $\overline{RAS}$ refresh and hidden refresh: 1024 cycles in 16 ms
  - Self-refresh: 1024 cycles
- JEDEC standard pinout: 42-pin 400mil SOJ and 50(44)-pin 400mil TSOPII

Pin Configuration

42-Pin 400mil SOJ



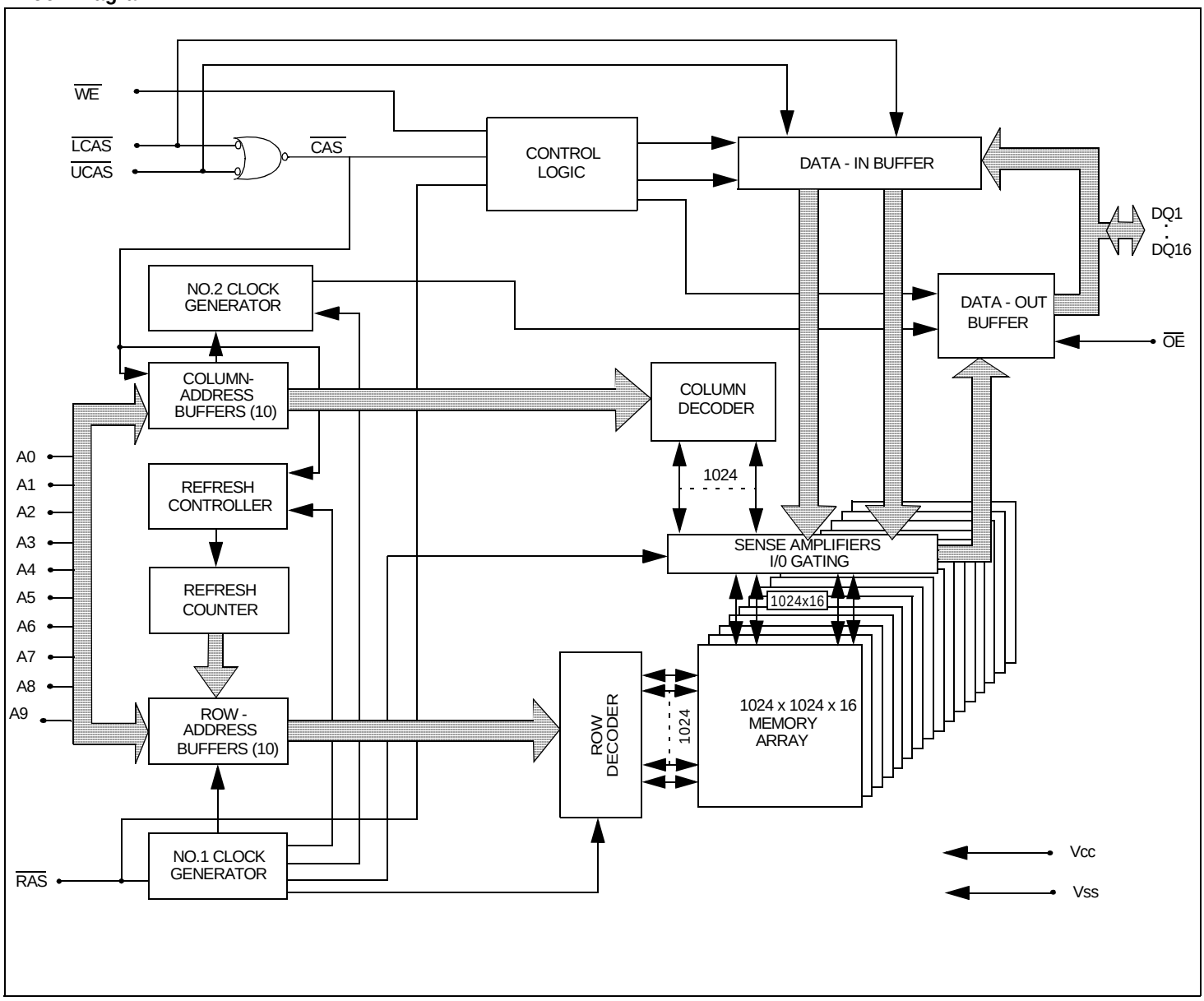
50(44)-Pin 400mil TSOPII



Pin Description

Pin Name	Function
A0-A9	Address inputs - Row address: A0-A9 - Column address: A0-A9 - Refresh address: A0-A9
DQ0~DQ15	Data-in / data-out
$\overline{RAS}$	Row address strobe
$\overline{UCAS}$, $\overline{LCAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
Vcc	Power (+5 V or + 3.3V)
Vss	Ground
NC	No connection

Block Diagram



TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ROW	ADDRESSES COL	DQ_S	Notes
STANDBY		H	H → X	H → X	X	X	X	X	High-Z	
READ : WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ : LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte: Data-Out Upper Byte: High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte: High-Z Upper Byte: Data-Out	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte: Data-In Upper Byte: High-Z	
WRITE : UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte: High-Z Upper Byte: Data-In	
READ WRITE		L	L	L	H → L	L → H	ROW	COL	Data-Out, Data-In	1,2
PAGE-MODE READ	1st Cycle	L	H → L	H → L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H → L	H → L	H	L	n/a	COL	Data-Out	2
PAGE-MODE WRITE	1st Cycle	L	H → L	H → L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H → L	H → L	L	X	n/a	COL	Data-In	1
PAGE-MODE READ-WRITE	1st Cycle	L	H → L	H → L	H → L	L → H	ROW	COL	Data-Out, Data-In	1,2
	2nd Cycle	L	H → L	H → L	H → L	L → H	n/a	COL	Data-Out, Data-In	1,2
HIDDEN REFRESH	READ	L → H → L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L → H → L	L	L	L	X	ROW	COL	Data-In	1,3
$\overline{RAS}$-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H → L	L	L	H	X	X	X	High-Z	4

Notes: 1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{LCAS}$ or $\overline{UCAS}$ active).

2. These READ cycles may also be BYTE READ cycles (either $\overline{LCAS}$ or $\overline{UCAS}$ active).

3. EARLY WRITE only.

4. At least one of the two $\overline{CAS}$ signals must be active ($\overline{LCAS}$ or $\overline{UCAS}$).

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Voltage on an any pin relative to Vss	5V	V_T	-1.0 to + 7.0	V
	3.3V		-0.5 to + 4.6	
Supply voltage relative to Vss	5V	V_{CC}	-1.0 to + 7.0	V
	3.3V		-0.5 to + 4.6	
Short circuit output current		I_{OUT}	50	mA
Power dissipation		P_D	1.0	W
Operating temperature		T_{OPT}	0 to + 70	°C
Storage temperature		T_{STG}	-55 to + 125	°C

Recommended DC Operating Conditions

Parameter/Condition	Sym-bol	5 Volt Version			3.3 Volt Version			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	3.15	3.3	3.6	V
Input High Voltage, all inputs	V_{IH}	2.4	-	V_{CC} + 1.0	2.0	-	V_{CC} + 0.3	V
Input Low Voltage, all inputs	V_{IL}	-1.0	-	0.8	-0.3	-	0.8	V

Capacitance

Ta = 25°C, V_{CC} = 5V ±10 % or 3.3V ±10 %, f = 1MHz

Parameter	Symbol	Max	Unit	Note
Input capacitance (Address)	C_{I1}	5	pF	1
Input capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{OE}$, $\overline{WE}$)	C_{I2}	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	7	pF	1, 2

Note: 1. Capacitance measured with effective capacitance measuring method.
2. $\overline{RAS}$, $\overline{LCAS}$ and $\overline{UCAS}$ = V_{IH} to disable Dout.

DC Characteristics; 5- Volt Verion (T_a = 0 to + 70 °C, V_{CC}= + 5V ±10 %,V_{SS} = 0V)

Parameter	Symbol	Test Conditions	VG26(S)18165				Unit	Notes
			-5		-6			
			Min	Max	Min	Max		
Operating current	I_{CC1}	$\overline{RAS}$ cycling LCAS / UCAS cycling t_{RC} = min	-	160	-	145	mA	1, 2
Standby current	I_{CC2}	TTL interface $\overline{RAS}$,LCAS / UCAS = V_{IH} Dout = High-Z		2	-	2	mA	
		CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ Vcc -0.2V Dout = High-Z		1	-	1	mA	
$\overline{RAS}$-only refresh current	I_{CC3}	$\overline{RAS}$ cycling, LCAS / UCAS = V_{IH} t_{RC} = min	-	160	-	145	mA	1, 2
EDO page mode current	I_{CC4}	t_{RC} = min	-	90	-	80	mA	1, 3
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	t_{RC} = min $\overline{RAS}$, $\overline{LCAS}$ / $\overline{UCAS}$ cycling	-	160	-	145	mA	1, 2
Self-refresh current	I_{CC6}	t_{RAS} ≥ 100µs	-	500	-	500	µA	
Input leakage current	I_{LI}	$0V \le V_{IN} \le V_{CC}$ + 0.5V	-5	5	-5	5	µA	
Output leakage current	I_{LO}	$0V \le V_{OUT} \le V_{CC}$ + 0.5V Dout = Disable	-5	5	-5	5	µA	
Output high Voltage	V_{OH}	I_{OH} = - 5mA	2.4	-	2.4	-	V	
Output low voltage	V_{OL}	I_{OL} = + 4.2mA	-	0.4	-	0.4	V	

Notes:

1. I_{CC} is specified as an average current. It depends on output loading condition and cycle rate when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. For I_{CC4}, address can be changed once or less within one EDO page mode cycle time.

DC Characteristics ; 3.3 - Volt Version (T_a = 0 to 70°C, V_{CC} = + 3.15V~3.6V , V_{SS} = 0V)

Parameter	Symbol	Test Conditions	VG26V(S)18165				Unit	Notes
			-5		-6			
			Min	Max	Min	Max		
Operating current	I_{CC1}	$\overline{RAS}$ cycling LCAS / UCAS cycling t_{RC} = min	-	160	-	145	mA	1, 2
Standby Current	I_{CC2}	LVTTL interface $\overline{RAS}$, LCAS / UCAS = V_{IH} Dout = High-Z	-	2	-	2	mA	
		CMOS interface $\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ -0.2V Dout = High-Z	-	0.5	-	0.5	mA	
$\overline{RAS}$- only refresh current	I_{CC3}	$\overline{RAS}$ cycling LCAS / UCAS = V_{IH} t_{RC} = min	-	160	-	145	mA	1, 2
EDO page mode current	I_{CC4}	t_{PC} = min	-	90	-	80	mA	1, 3
$\overline{CAS}$- before- $\overline{RAS}$ refresh current	I_{CC5}	t_{RC} = min $\overline{RAS}$, $\overline{LCAS}$ / $\overline{UCAS}$ cycling	-	160	-	145	mA	1, 2
Self- refresh current	I_{CC6}	$t_{RASS} \geq 100\mu s$	-	450	-	450	µA	
Input leakage current	I_{LI}	$0V \leq Vin \leq V_{CC}$ + 0.3V	-5	5	-5	5	µA	
Output leakage current	I_{LO}	$0V \leq Vout \leq V_{CC}$ + 0.3V Dout = Disable	-5	5	-5	5	µA	
Output high Voltage	V_{OH}	I_{OH} = -2mA	2.4	-	2.4	-	V	
Output low voltage	V_{OL}	I_{OL} = +2mA	-	0.4	-	0.4	V	

Notes:

1. I_{CC} is specified as an average current. It depends on output loading condition and cycle rate when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. For I_{CC4}, address can be changed once or less within one EDO page mode cycle time.

AC Characteristics(T_a = 0 to + 70°C, V_{cc} = 5V ±10 % or 3.15V~3.6V, V_{ss} = 0V) *1, *2, *3, *4, *5

Test conditions
- Output load:
  two TTL Loads and 50pF (V_{CC} = 5.0V ±10 %); one TTL Load and 50pF (V_{CC} = 3.15V~3.6V)
- Input timing reference levels:
  V_{IH} = 2.4V, V_{IL} = 0.8V (V_{CC} = 5.0V ±10 %); V_{IH} = 2.0V, V_{IL} = 0.8V (V_{CC} = 3.15V~3.6V)
- Output timing reference levels:
  V_{OH} = 2.0V, V_{OL} = 0.8V (V_{CC} = 5.0V ±10 %, 3.15V ~3.6V)

Read, Write, Read- Modify- Write and Refresh Cycles

(Common Parameters)

Parameter	Symbol	VG26(V)(S) 18165				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84	-	104	-	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	-	40	-	ns	
$\overline{LCAS}$ / $\overline{UCAS}$ precharge time in normal mode	t_{CPN}	10	-	10	-	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	6
$\overline{LCAS}$ / $\overline{UCAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	7
Row address setup time	t_{ASR}	0	-	0	-	ns	
Row address hold time	t_{RAH}	8	-	10	-	ns	
Column address setup time	t_{ASC}	0	-	0	-	ns	8
Column address hold time	t_{CAH}	8	-	10	-	ns	
$\overline{RAS}$ to $\overline{LCAS}$ / $\overline{UCAS}$ delay time	t_{RCD}	12	37	14	45	ns	9
$\overline{RAS}$ to column address delay time	t_{RAD}	10	25	12	30	ns	10
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	-	30	-	ns	
$\overline{RAS}$ hold time	t_{RSH}	8	-	10	-	ns	
$\overline{LCAS}$ / $\overline{UCAS}$ hold time	t_{CSH}	38	-	40	-	ns	
$\overline{LCAS}$ / $\overline{UCAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	-	5	-	ns	11
$\overline{OE}$ to Din delay time	t_{OED}	20	-	20	-	ns	
Transition time (rise and fall)	t_T	1	50	1	50	ns	12
Refresh period	t_{REF}	-	16	-	16	ms	
$\overline{LCAS}$ / $\overline{UCAS}$ to output in Low- Z	t_{CLZ}	0	-	0	-	ns	
$\overline{LCAS}$ / $\overline{UCAS}$ delay time from Din	t_{DZC}	0	-	0	-	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	-	0	-	ns	

Read Cycle

Parameter	Symbol	VG26(V)(S)18165				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	-	50	-	60	ns	13
Access time from $\overline{LCAS}$ / $\overline{UCAS}$	t_{CAC}	-	13	-	15	ns	14, 15
Access time from column address	t_{AA}	-	25	-	30	ns	15, 16
Access time from $\overline{OE}$	t_{OEA}	-	12	-	15	ns	
Read command setup time	t_{RCS}	0	-	0	-	ns	8
Read command hold time to $\overline{LCAS}$ / $\overline{UCAS}$	t_{RCH}	0	-	0	-	ns	11, 17
Read command hold time to $\overline{RAS}$	t_{RRH}	10	-	10	-	ns	17
Output buffer turn-off time	t_{OFF}	0	12	0	15	ns	18
Output buffer turn-off time from $\overline{OE}$	t_{OEZ}	0	12	0	15	ns	18

Write Cycle

Parameter	Symbol	VG26(V)(S)18165				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	-	0	-	ns	8, 19
Write command hold time	t_{WCH}	8	-	10	-	ns	
Write command pulse width	t_{WP}	8	-	10	-	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13	-	15	-	ns	
Write command to $\overline{LCAS}$ / $\overline{UCAS}$ lead time	t_{CWL}	8	-	10	-	ns	20
Data-in setup time	t_{DS}	0	-	0	-	ns	21
Data-in hold time	t_{DH}	8	-	10	-	ns	21
$\overline{WE}$ to Data-in delay	t_{WED}	10	-	10	-	ns	

Read- Modify- Write Cycle

Parameter	Symbol	VG26(V)(S)18165				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
Read-modify- write cycle time	t_{RWC}	108	-	133	-	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	64	-	77	-	ns	19
$\overline{LCAS}$ / $\overline{UCAS}$ to $\overline{WE}$ dealy time	t_{CWD}	26	-	32	-	ns	19
Column address to $\overline{WE}$ delay time	t_{AWD}	39	-	47	-	ns	19
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	8	-	10	-	ns	

Refresh Cycle

Parameter	Symbol	VG26(V)(S)18165				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
$\overline{LCAS}$ / $\overline{UCAS}$ setup time (CBR refresh)	t_{CSR}	5	-	5	-	ns	
$\overline{LCAS}$ / $\overline{UCAS}$ hold time (CBR refresh)	t_{CHR}	8	-	10	-	ns	11
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	-	5	-	ns	8
$\overline{RAS}$ pulse width (self refresh)	t_{RASS}	100	-	100	-	µs	
$\overline{RAS}$ precharge time (self refresh)	t_{RPS}	90	-	110	-	ns	
$\overline{LCAS}$ / $\overline{UCAS}$ hold time (CBR self refresh)	t_{CHS}	-50	-	-50	-	ns	
$\overline{WE}$ setup time	t_{WSR}	0	-	0	-	ns	
$\overline{WE}$ hold time	t_{WHR}	10	-	10	-	ns	

EDO Page Mode Cycle

Parameter	Symbol	VG26(V)(S)18165				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
EDO page mode cycle time	t_{PC}	20	-	25	-	ns	
EDO page mode $\overline{LCAS}$ / $\overline{UCAS}$ precharge time	t_{CP}	10	-	10	-	ns	
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	50	10^5	60	10^5	ns	22
Access time from $\overline{LCAS}$ / $\overline{UCAS}$ precharge	t_{CPA}	-	30	-	35	ns	11, 15
$\overline{RAS}$ hold time from $\overline{LCAS}$ / $\overline{UCAS}$ pre-charge	t_{CPRH}	30	-	35	-	ns	
$\overline{OE}$ high hold time from $\overline{LCAS}$ / $\overline{UCAS}$ high	t_{OEHC}	5	-	5	-	ns	
$\overline{OE}$ high pulse width	t_{OEP}	10	-	10	-	ns	
Data output hold time after $\overline{LCAS}$ / $\overline{UCAS}$ low	t_{COH}	5	-	5	-	ns	
Output disable delay from $\overline{WE}$	t_{WHZ}	3	10	3	10	ns	
$\overline{WE}$ pulse width for output disable when $\overline{LCAS}$ / $\overline{UCAS}$ high	t_{WPZ}	10	-	10	-	ns	

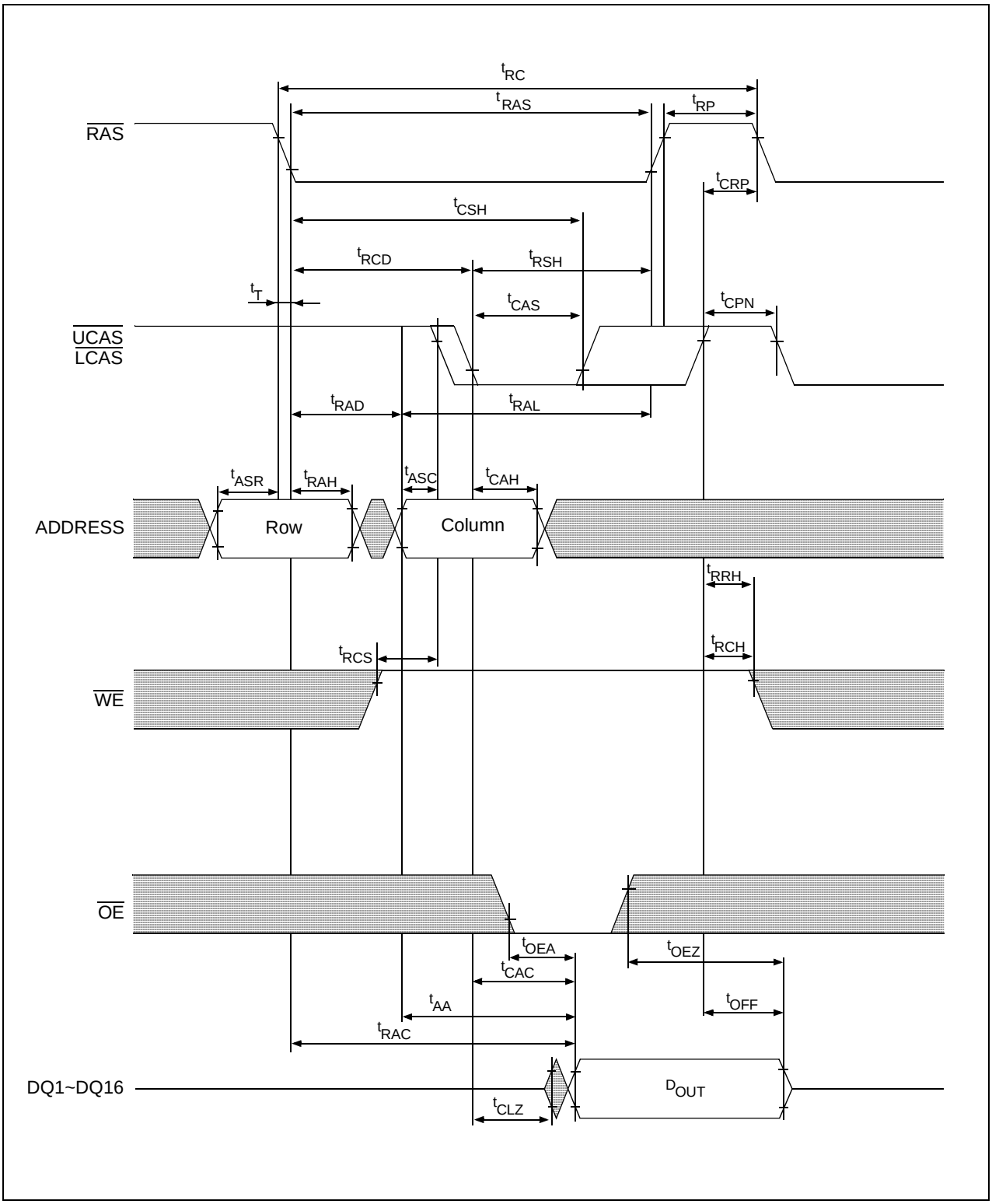
EDO Page Mode Read Modify Write Cycle

Parameter	Symbol	VG26(V)(S)18165				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
EDO page mode read- modify- write cycle $\overline{LCAS}$ / $\overline{UCAS}$ precharge to $\overline{WE}$ delay time	t_{CPW}	45	-	55	-	ns	11
EDO page mode read- modify- write cycle time	t_{PRWC}	56	-	68	-	ns	

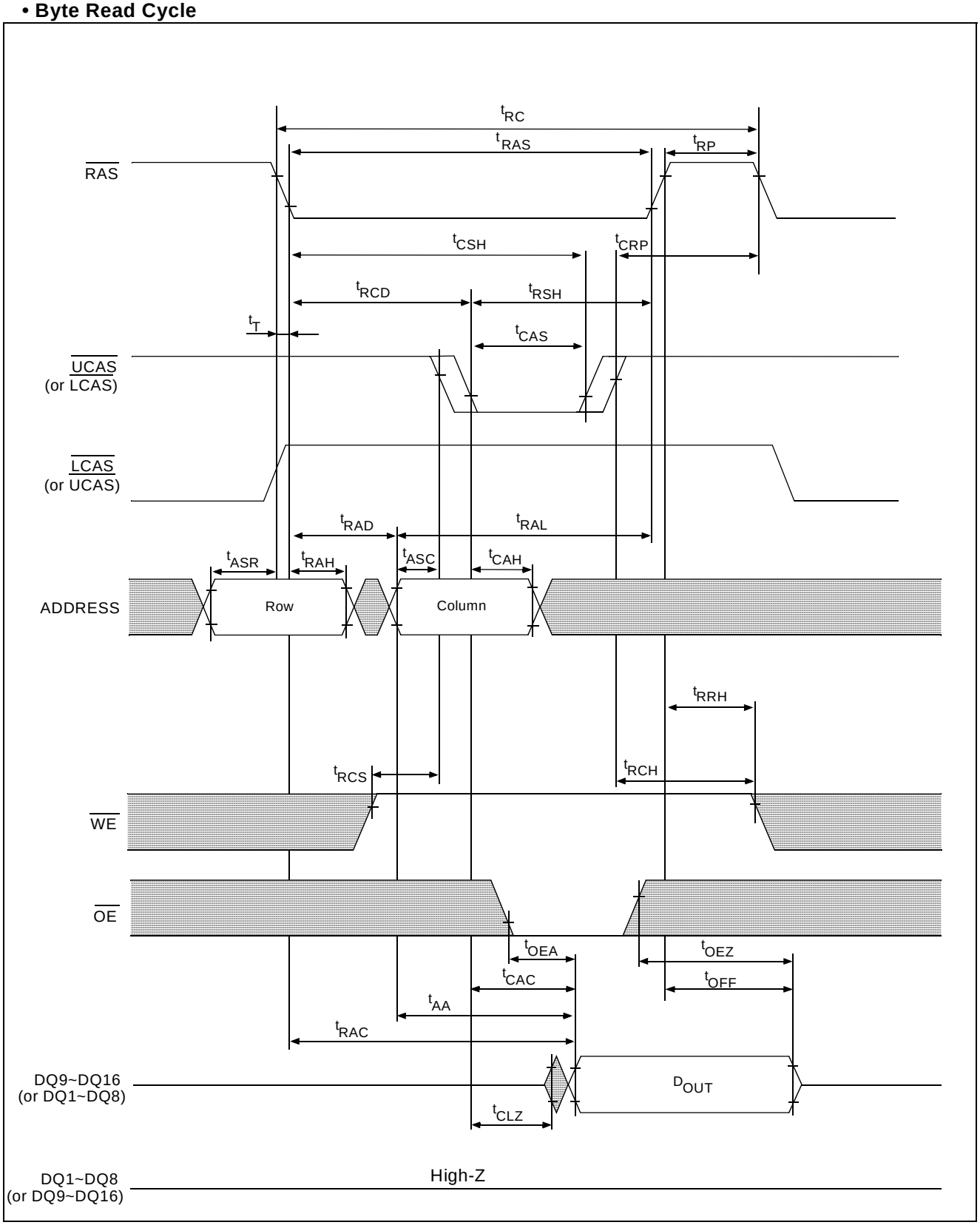
Notes :

1. AC measurements assume t_T = 1ns.
2. An initial pause of 100 μs is required after power up, and it followed by a minimum of eight initialization cycles (RAS - only refresh cycle or CAS - before - RAS refresh cycle). If the internal refresh counter is used, a minimun of eight CAS - before - RAS refresh cycles are required.
3. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
4. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
5. When both $\overline{LCAS}$ and $\overline{UCAS}$ go low at the same time, all 16-bits data are witten into the device. $\overline{LCAS}$ and UCAS cannot be staggered within the same write/read cycles.
6. $t_{RAS}(min) = t_{RWD}(min)+t_{RWL}(min)+t_T$ in read-modify-write cycle.
7. $t_{CAS}(min) = t_{CWD}(min)+t_{CWL}(min)+t_T$ in read-modify-write cycle.
8. $t_{ASC}(min)$, $t_{RCS}(min)$, $t_{WCS}(min)$, and t_{RPC} are determined by the falling edge of $\overline{CAS}$.
9. $t_{RCD}(max)$ is specified as a reference point only, and $t_{RAC}(max)$ can be met with the $t_{RCD}(max)$ limit. Otherwise, t_{RAC} is controlled exclusively by t_{CAC} if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit.
10. $t_{RAD}(max)$ is specified as a reference point only, and $t_{RAC}(max)$ can be met with the $t_{RAD}(max)$ limit. Otherwise, t_{RAC} is controlled exclusively by t_{AA} if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit.
11. t_{CRP}, t_{CHR}, t_{RCH}, t_{CPA} and t_{CPW} are determined by the rising edge of $\overline{CAS}$.
12. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing or input signals. Therefore, transition time is measured between V_{IH} and V_{IL}.
13. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
14. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
15. Access time is determined by the maximum of t_{AA}, t_{CAC}, t_{CPA}.
16. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
17. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
18. $t_{OFF}(max)$ and $t_{OEZ}(max)$ define the time at which the output achieves the open circuit condition (high impedance). t_{OFF} is determined by the later rising edge of $\overline{RAS}$ or $\overline{CAS}$.
19. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(min)$, the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}(min)$, $t_{CWD} \geq t_{CWD}(min)$, $t_{AWD} \geq t_{AWD}(min)$ and $t_{CPW} \geq t_{CPW}(min)$, the cycle is a read-modify-write and the data output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data output (at access time) is indeterminate.
20. t_{CWL} shall be satisfied by both $\overline{LCAS}$ and $\overline{UCAS}$.
21. These parameters are referenced to $\overline{LCAS}$ or $\overline{LCAS}$ separately in an early write cycle and to $\overline{WE}$ edge in a delayed write or a read-modify-write cycle.
22. t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.

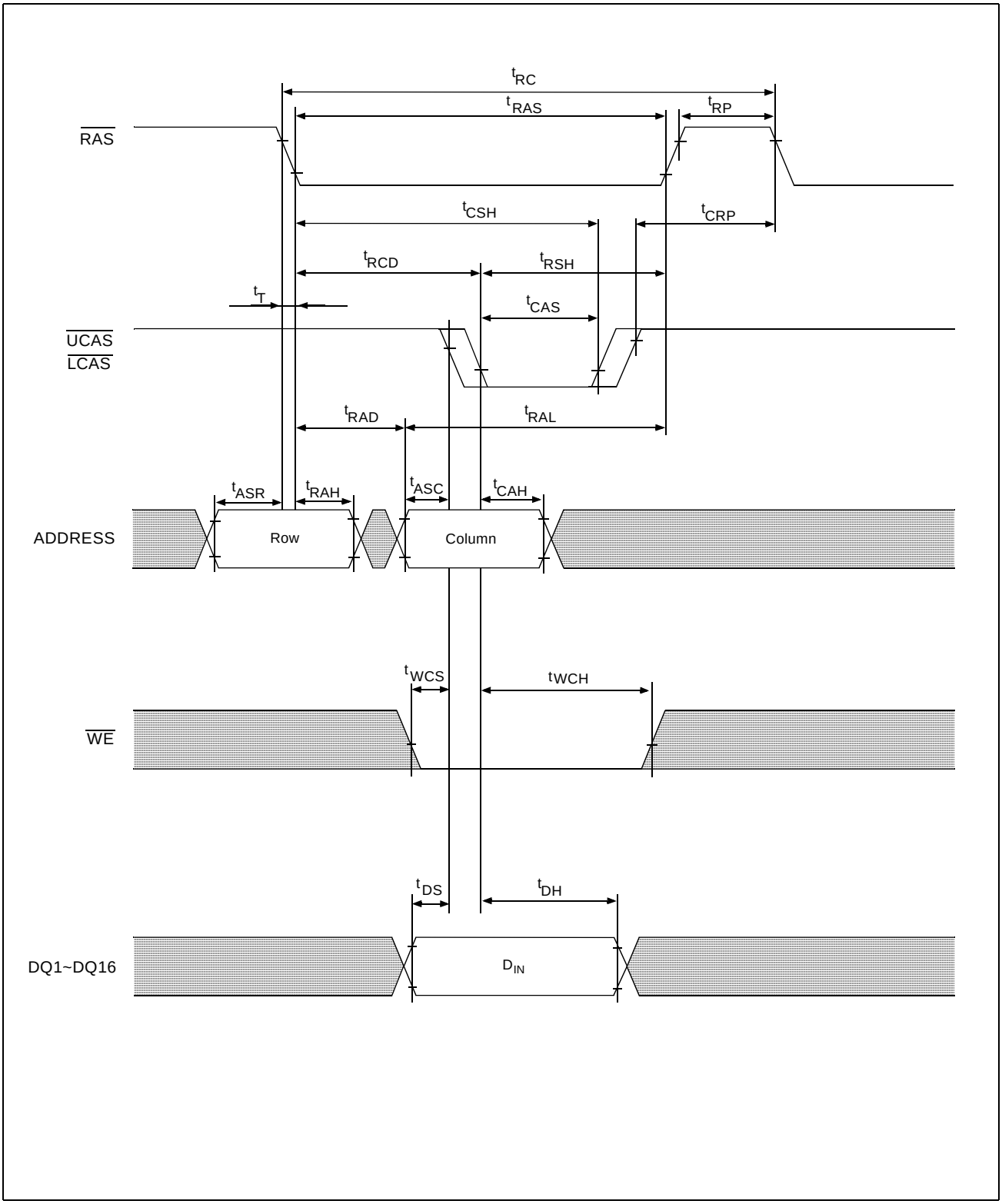
Timing Waveforms
• Word Read Cycle



• **Byte Read Cycle**



• Word Early Write Cycle



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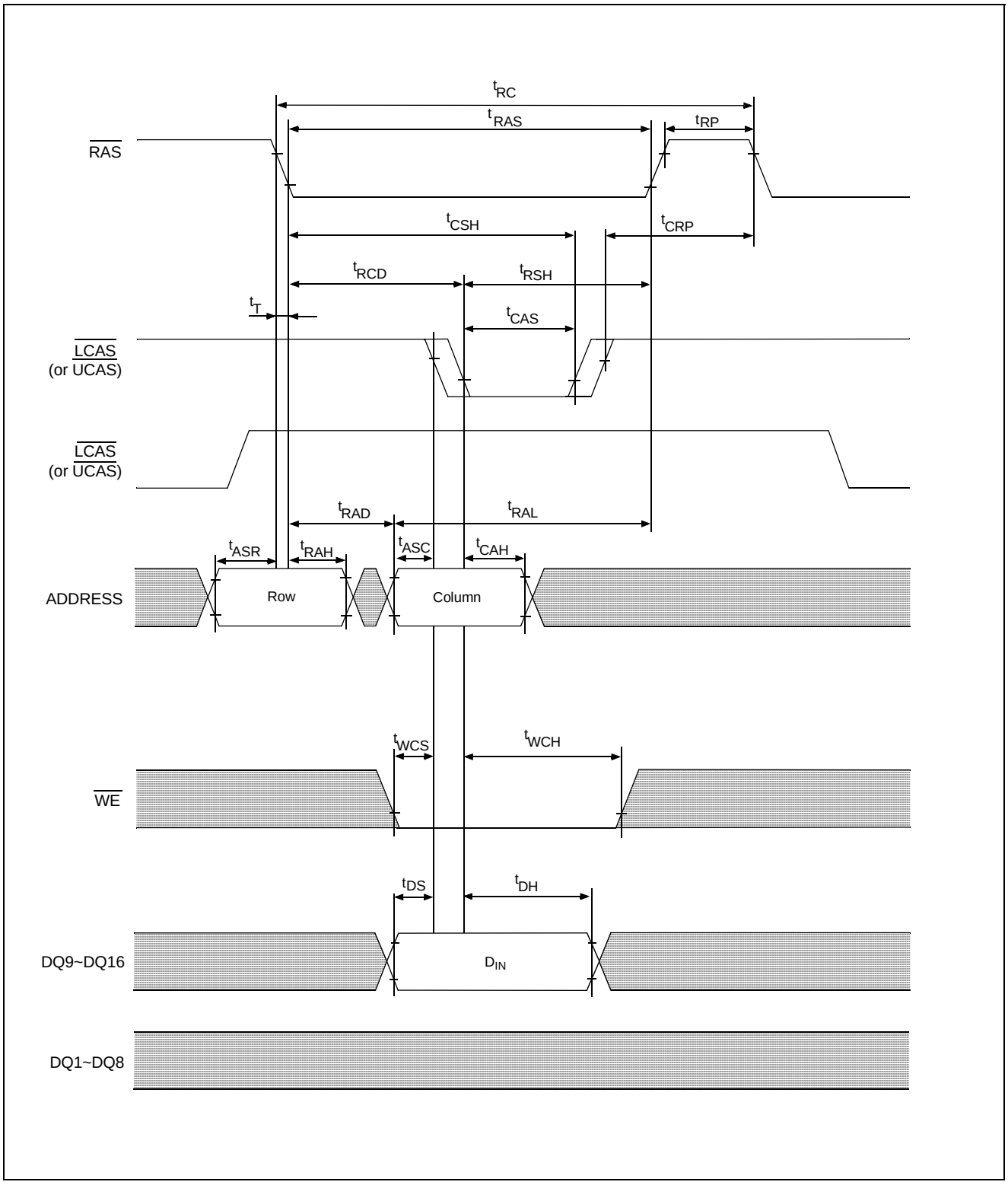
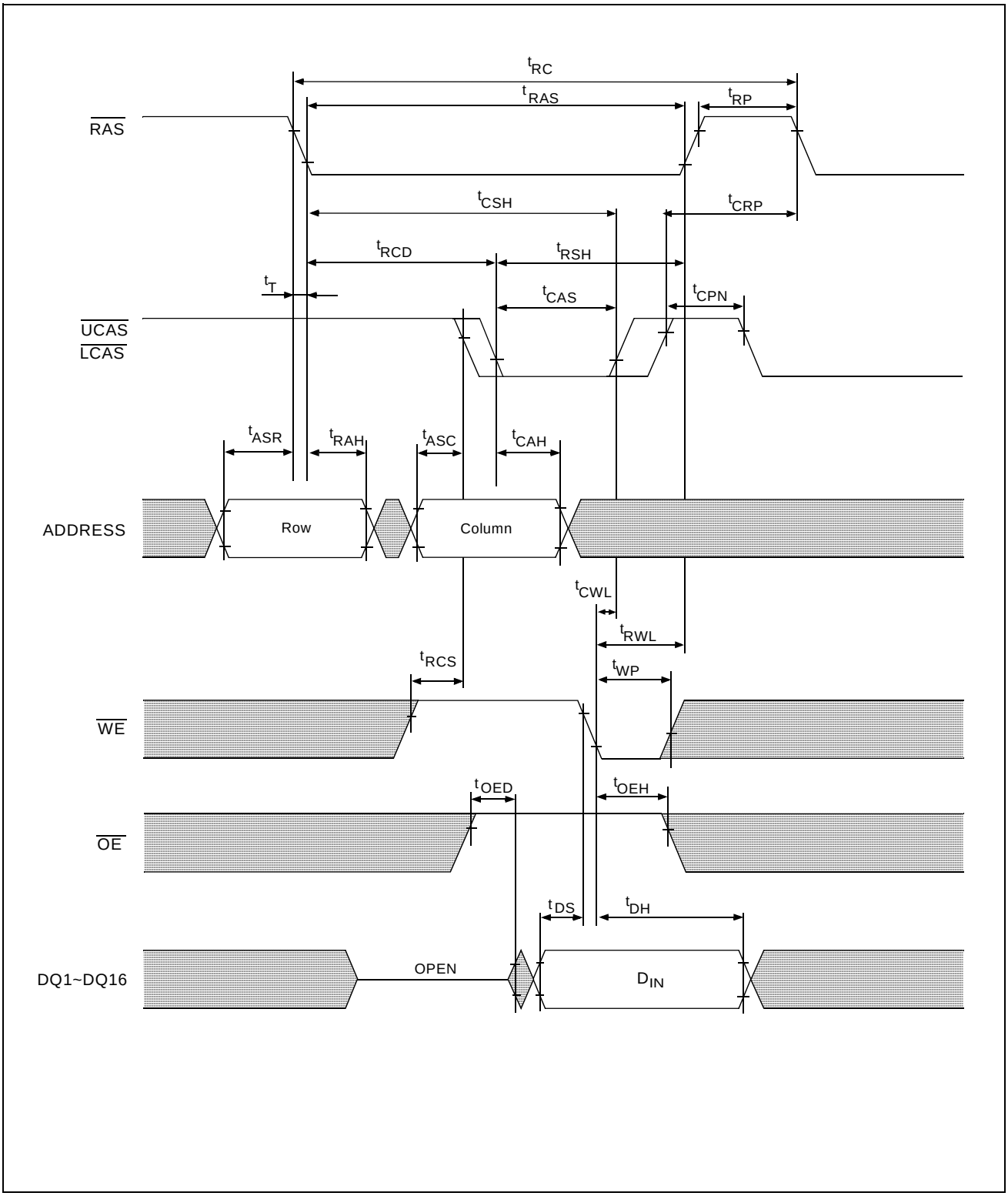
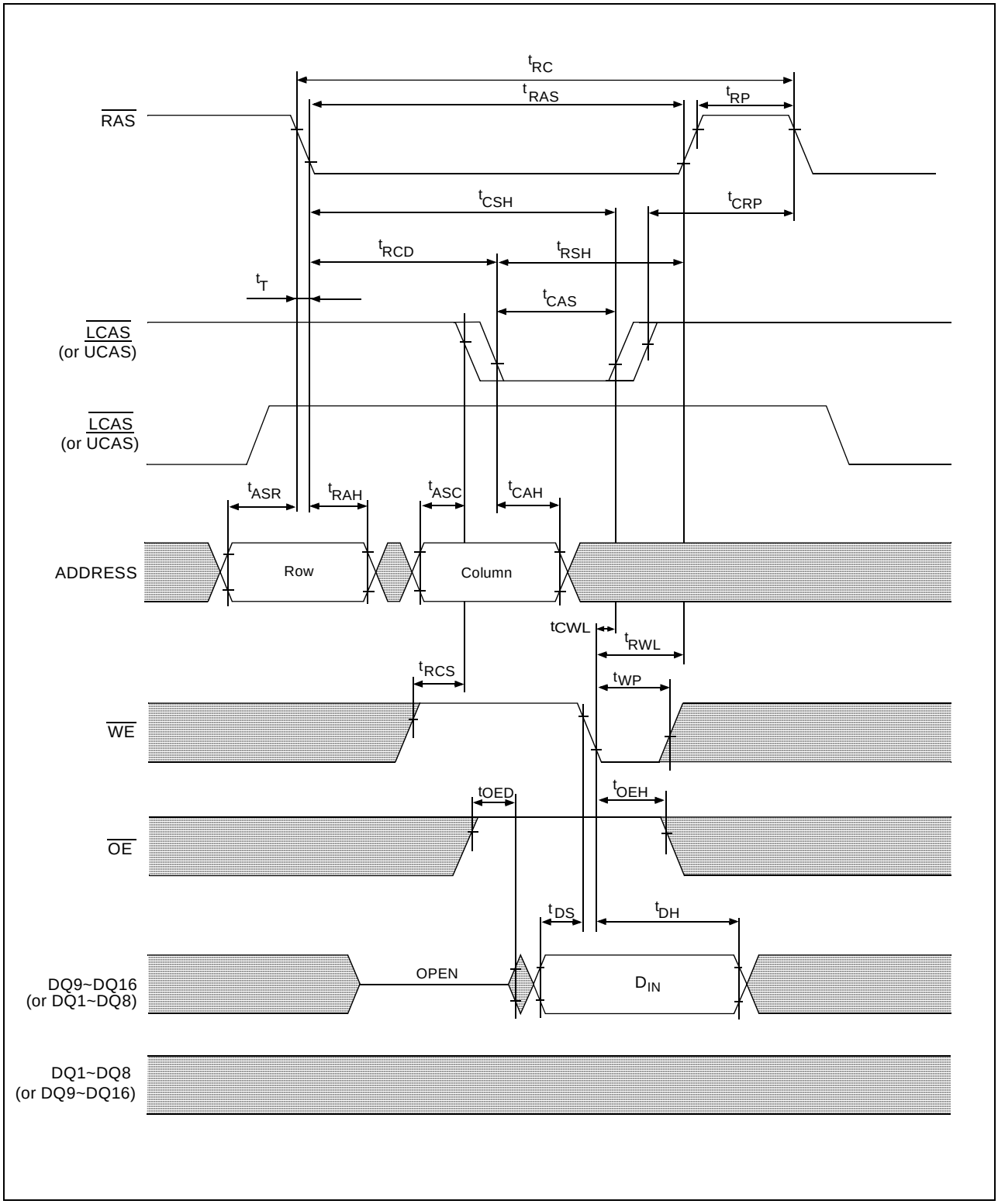


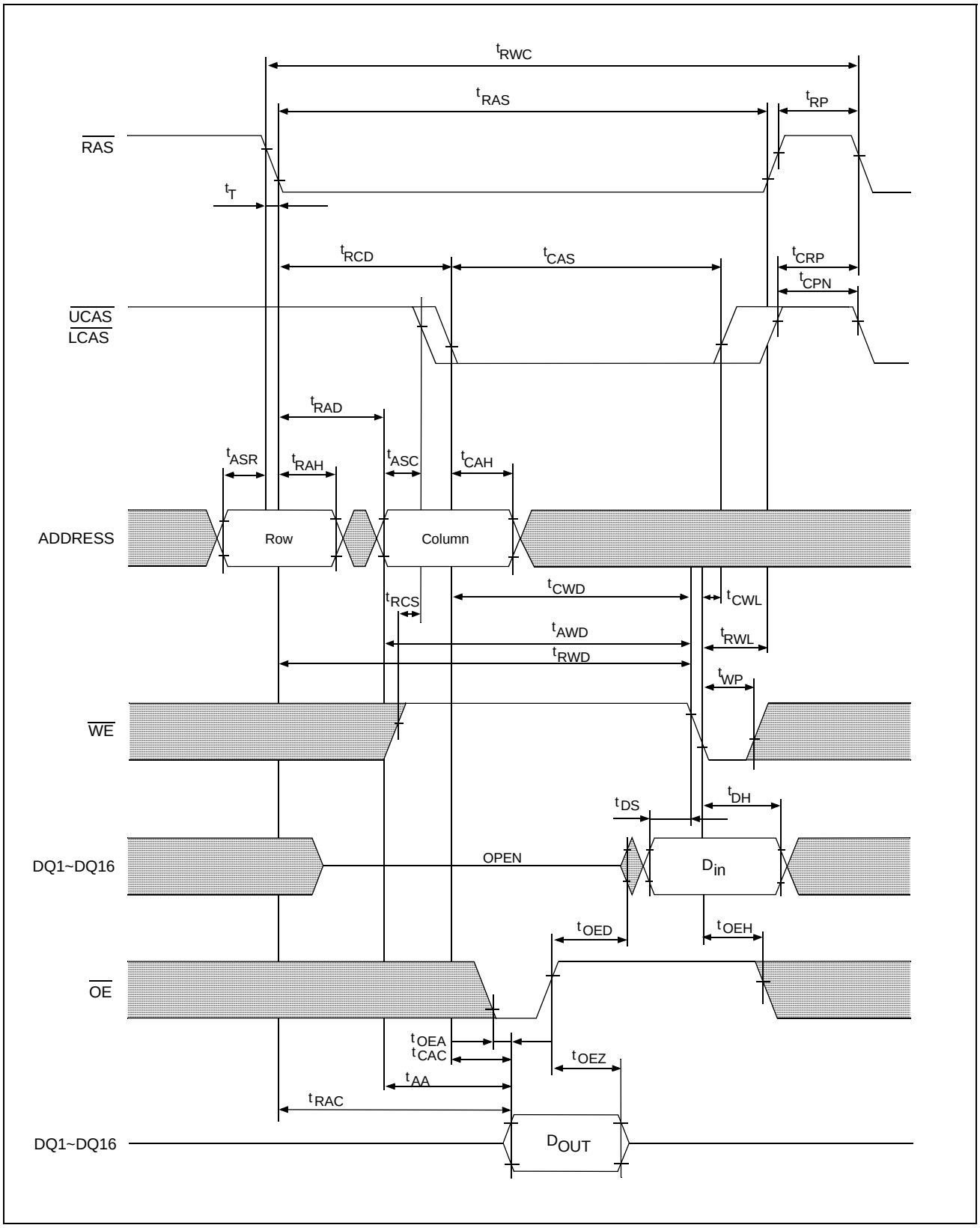
• Word Delayed Write Cycle



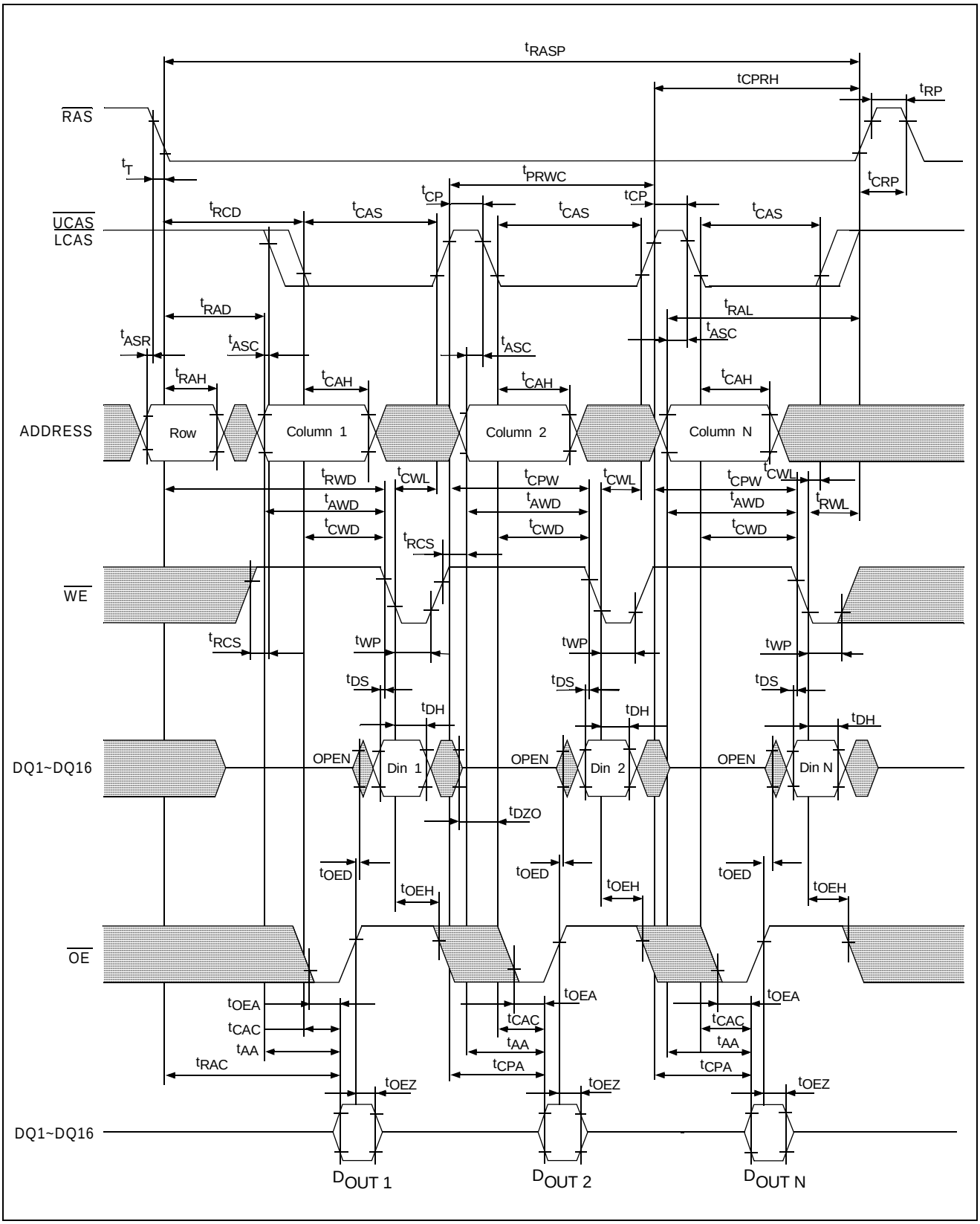
• Byte Delayed Write Cycle



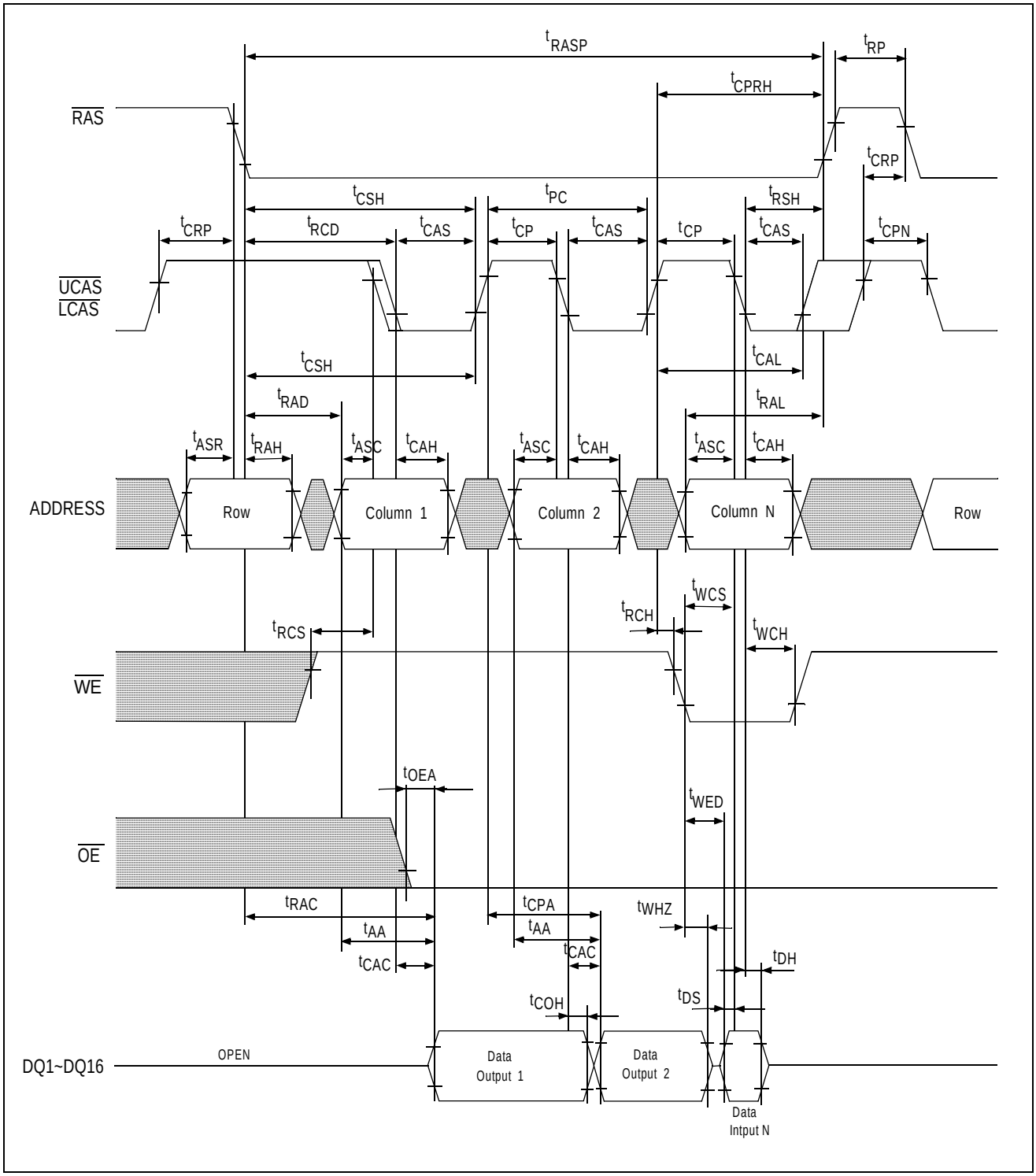
• Word Read-Modify-Write Cycle



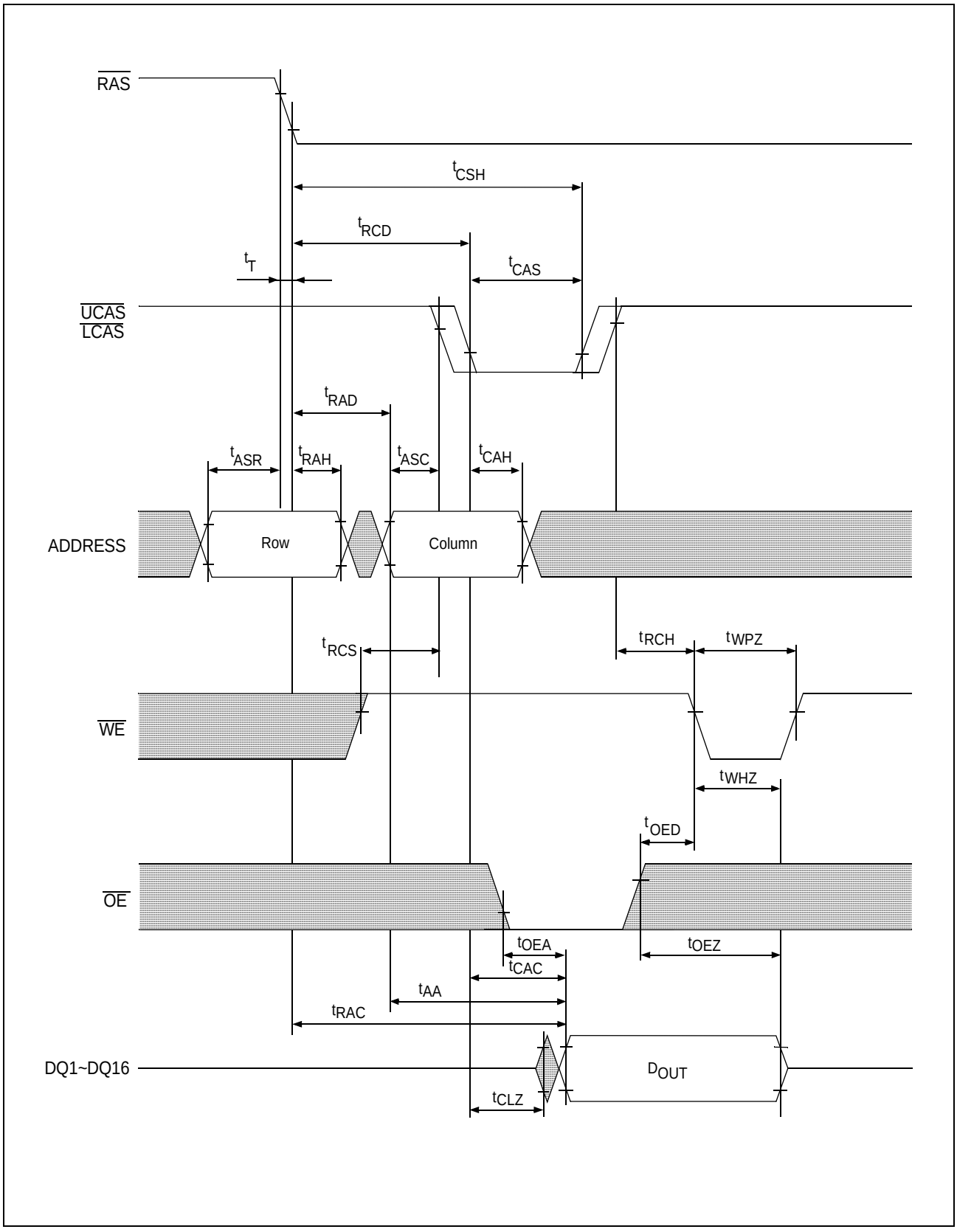
• EDO Page Mode Word Read-Modify-Write Cycle



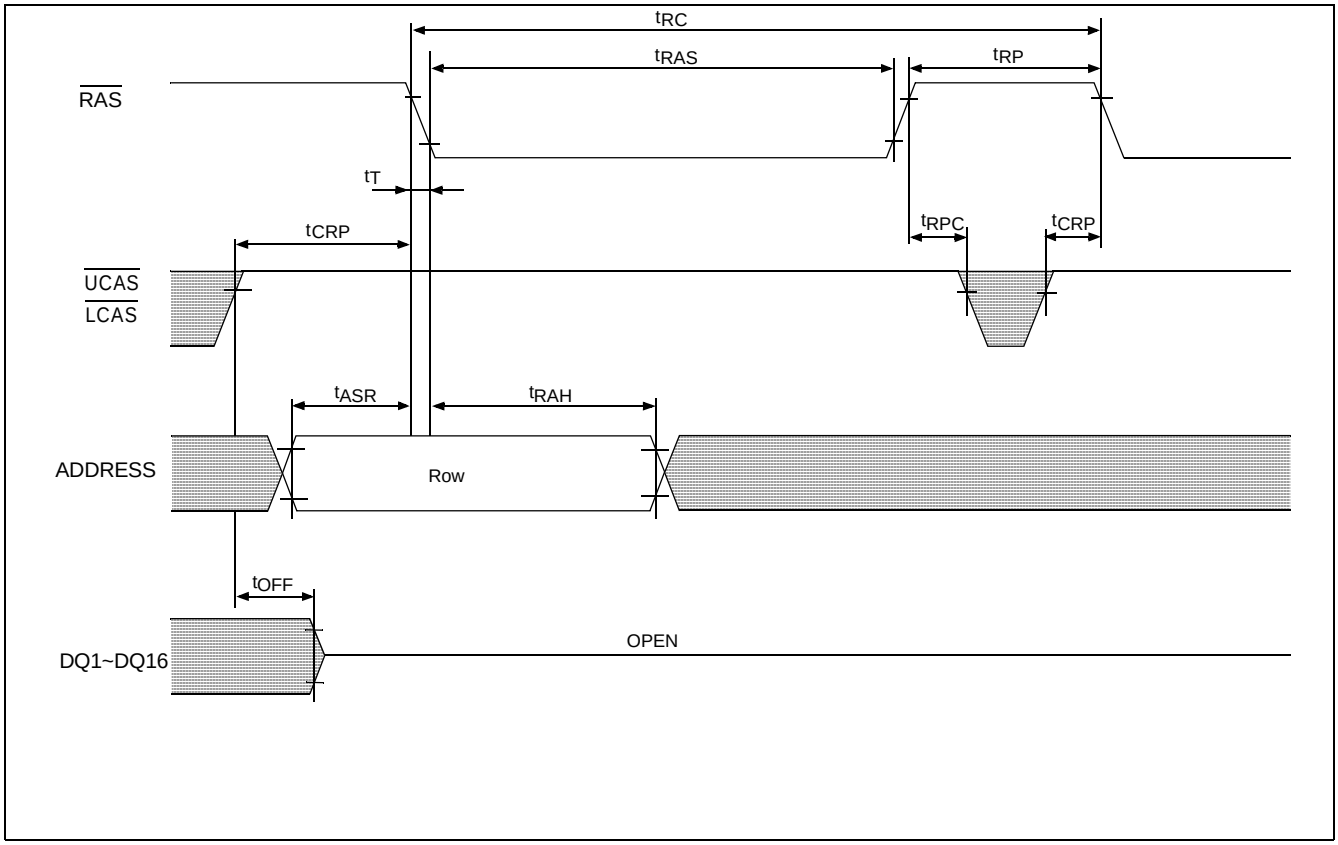
• **EDO Page Mode Word Read-Early-Write Cycle**



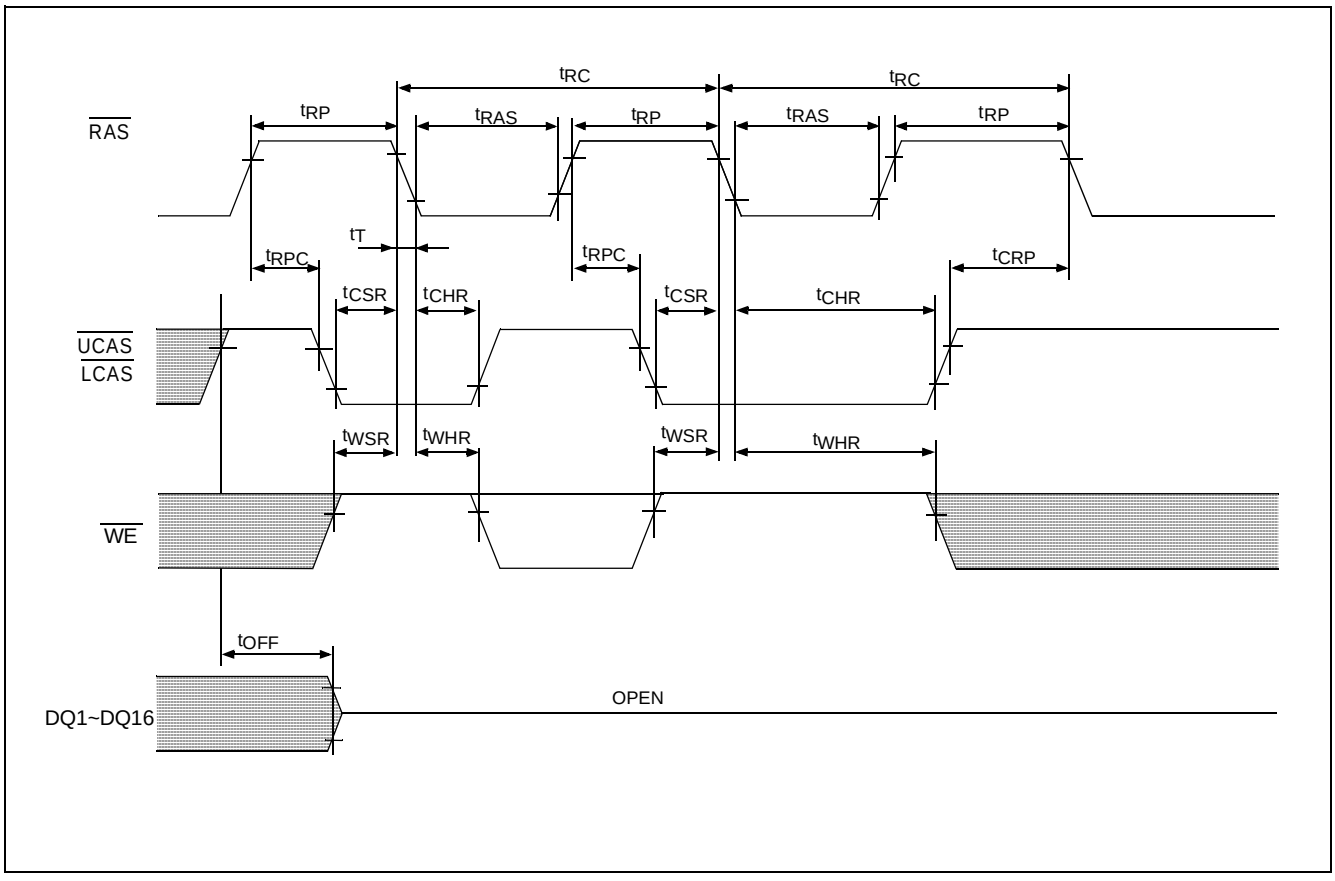
• **Read Cycle with $\overline{WE}$ Controlled Disable**



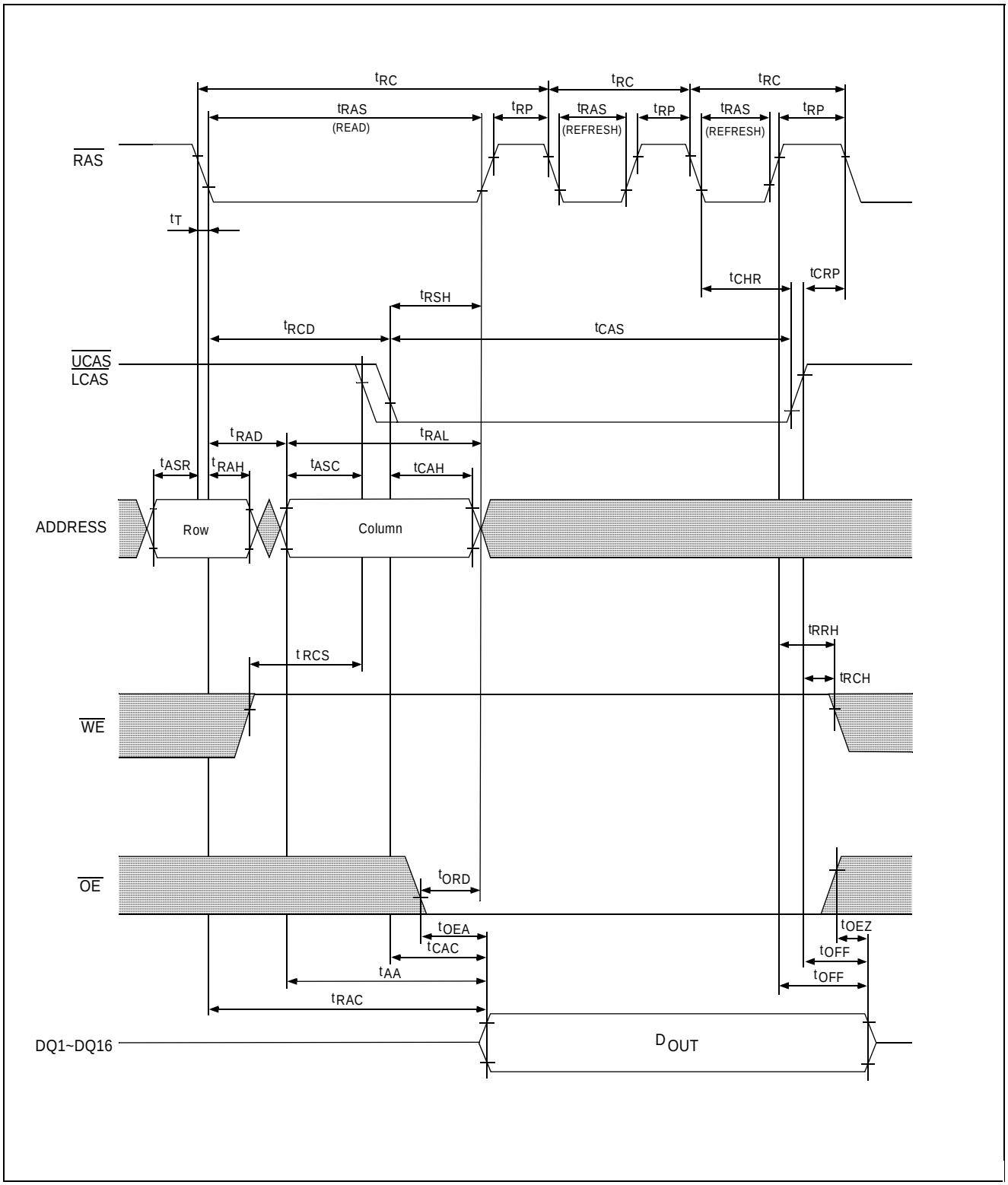
$\overline{\text{RAS}}$ - Only Refresh Cycle



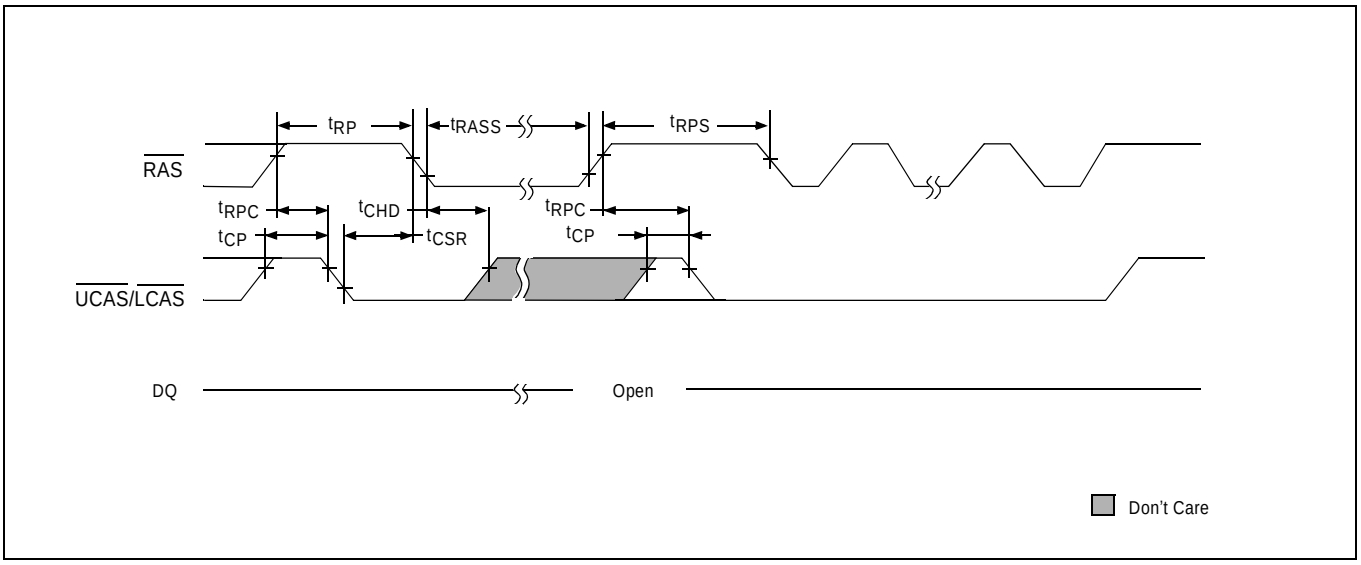
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



• **Hidden Refresh Cycle**



• **SELF REFRESH CYCLE (Addresses, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)**



Ordering information

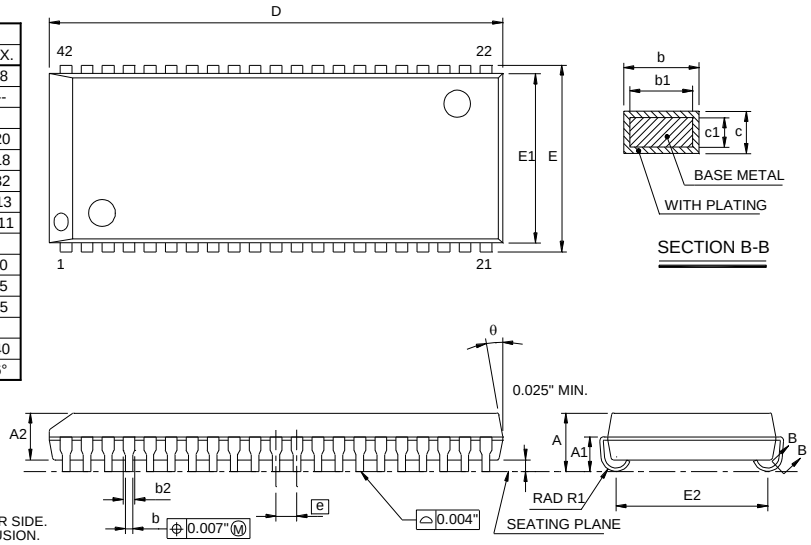
Part Number	Access time	Package
VG26(V)(S)18165CJ-5 VG26(V)(S)18165CJ-6	50 ns 60 ns	400mil 42-Pin Plastic SOJ
VG26(V)(S)18165CT-5 VG26(V)(S)18165CT-6	50 ns 60 ns	400mil 50(44)-Pin TSOPII

VG26(V)(S)18165CJ-5

- VG → VIS Memory Product
- 26 → Technology
- V → V: 3.3V Version; Non: 5V
- 18165 → Device Type and Configuation
- C → Revision (C and D)
- J → Package Type (J : SOJ, T : TSOP II)
- 5 → Speed (5: 50 ns, 6: 60 ns)

Package Information 42-pin SOJ

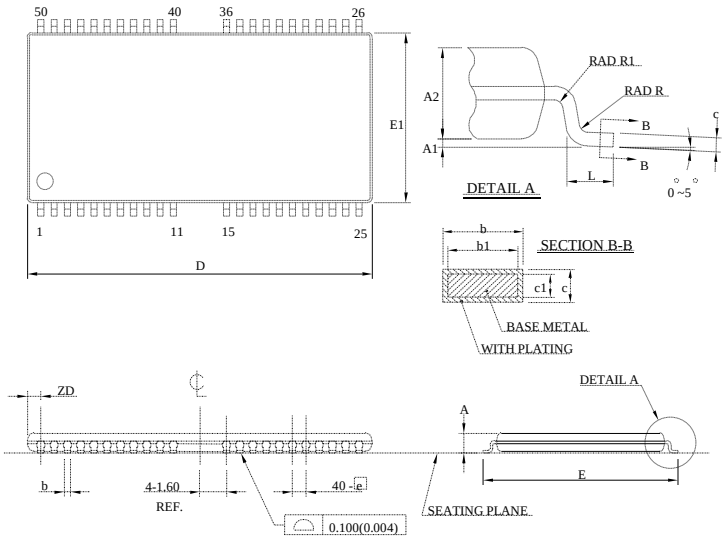
DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	3.25	3.51	3.76	0.128	0.138	0.148
A1	2.08	---	---	0.082	---	---
A2	2.79 REF.			0.110 REF.		
b	0.38	---	0.51	0.015	---	0.020
b1	0.38	---	0.46	0.015	---	0.018
b2	0.66	0.71	0.81	0.026	0.028	0.032
c	0.18	---	0.33	0.007	---	0.013
c1	0.18	0.20	0.28	0.007	0.008	0.011
e	1.27 BASIC			0.050 BASIC		
D	27.18	27.31	27.43	1.070	1.075	1.080
E	11.05	11.18	11.30	0.435	0.440	0.445
E1	10.03	10.16	10.29	0.395	0.400	0.405
E2	9.40 BASIC			0.370 BASIC		
R1	0.76	0.89	1.02	0.030	0.035	0.040
θ	3°	---	16°	3°	---	16°



NOTE:
1. CONTROLLING DIMENSION : INCHES
2. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.006"(0.15) PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD PROTRUSION. INTERLEAD PROTRUSION SHALL NOT EXCEED 0.01"(0.25) PER SIDE.
3. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE SHOULDER WIDTH TO EXCEED b2 MAX BY MORE THAN 0.005"(0.127) DAMBAR INTRUSION SHALL NOT REDUCE THE SHOULDER WIDTH TO LESS THAN 0.001"(0.025) BELOW b2 MIN.

Package Information 50(44)-pin TSOPII

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.20	---	---	0.047
A1	0.05	---	0.15	0.002	---	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	---	0.45	0.012	---	0.018
b1	0.30	---	0.40	0.012	---	0.016
c	0.12	---	0.21	0.005	---	0.008
c1	0.11	---	0.16	0.0045	---	0.006
D	20.82	20.95	21.08	0.820	0.825	0.830
ZD	0.875 BASIC			0.0344 BASIC		
e	0.80 BASIC			0.0315 BASIC		
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
L	0.40	0.50	0.60	0.016	0.020	0.024
R	0.11	---	0.25	0.004	---	0.010
R1	0.11	---	---	0.004	---	---



NOTE:
1. CONTROLLING DIMENSION : MILLIMETERS
2. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15mm(0.006") PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD PROTRUSION. INTERLEAD PROTRUSION SHALL NOT EXCEED 0.25mm(0.01") PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSIONS/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD TO BE WIDER THAN THE MAX b DIMENSION BY MORE THAN 0.13mm. DAMBAR INTRUSION SHALL NOT CAUSE THE LEAD TO BE NARROWER THAN THE MIN b DIMENSION BY MORE THAN 0.07mm.