CL-PS7111

FEATURES

■ **Performance matching 33-MHz Intel®
'486-based PC**
— More than 5 times the performance of the Motorola
"DragonBall" (MC68328)

■ **Ultra low power**
— Designed for applications that require long battery life
while using standard AA/AAA batteries or rechargeable
cells
— Average 45 mW/66 mW in Normal Operation
(2.7 V/3.3 V, 13 MHz/18.432 MHz)
— Average 15 mW in Idle state (clock to the CPU stopped,
everything else running)
— Average 50 μW in Standby state (realtime clock on,
everything else stopped)

■ **LCD controller**
— Interfaces directly to a single-scan panel monochrome
LCD
— Panel width size is programmable from 16 to 1024 pixels
in 16-pixel increments
— Video frame size programmable up to 128 Kbytes
— Bits per pixel programmable from 1, 2, or 4

(cont.)

Ultra-Low-Power
System-on-Chip
## with LCD Controller

OVERVIEW

The CL-PS7111 is designed for ultra-low-power applications such as organizers/PDAs, two-way pagers, smart cellular phones, and industrial hand-held information appliances. The core-logic functionality of the device is built around an ARM710A microprocessor with 8 Kbytes of four-way set-associative unified cache.

At 18.432 MHz (for 3.3-V operation), the CL-PS7111 delivers roughly the same level of performance offered by a 33-MHz Intel® '486-based PC. A 32-bit Y2K-compliant Real-Time Clock (RTC) and comparator is provided.

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Functional Block Diagram

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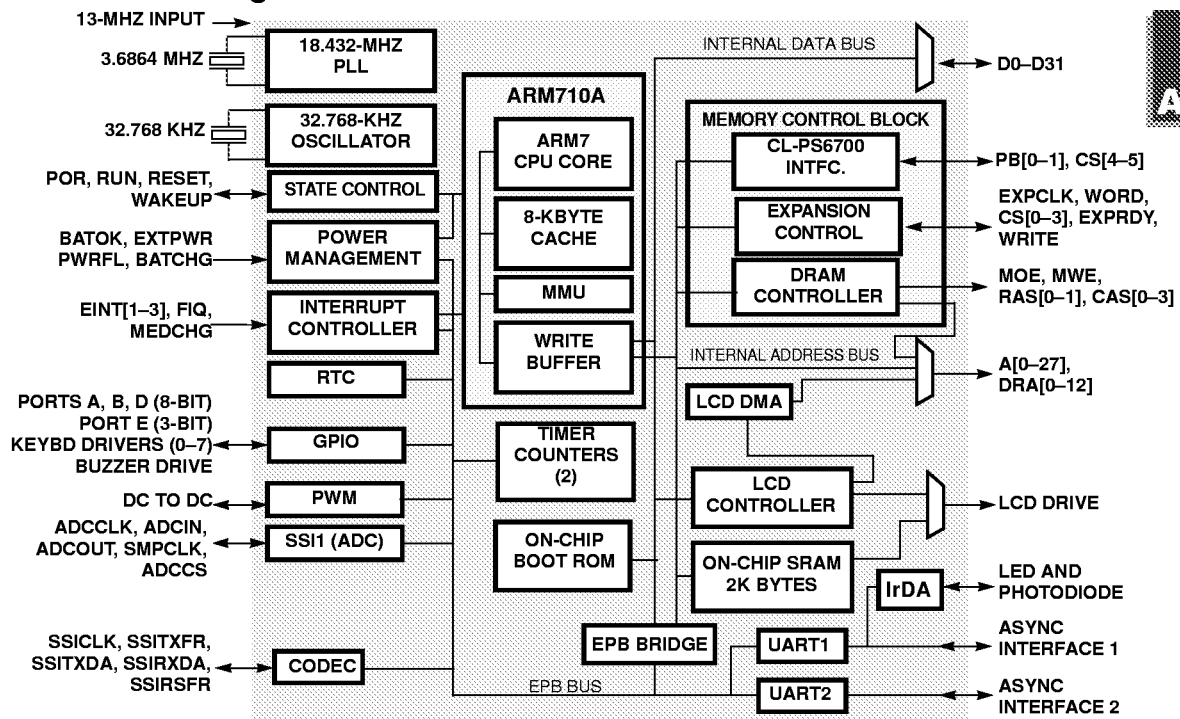
FEATURES (cont.)

■ **ARM710A microprocessor**
— ARM7 CPU
— 8 Kbytes of four-way set-associative cache
— MMU with 64-entry TLB (transition look-aside buffer)

■ **DRAM controller**
— Supports both 16- and 32-bit-wide DRAMs

■ **ROM/SRAM/FLASH memory control**
— Decodes 4, 5, or 6 separate memory segments of up to 256 Mbytes
— Each segment can be configured as 8, 16, or 32 bits wide and supports page-mode access
— Programmable access time for conventional SRAM/ROM/FLASH memory

■ **2 Kbytes of on-chip SRAM for fast program execution or as a frame buffer**

■ **On-chip for manufacturing support boot ROM**

■ **Two synchronous serial interfaces**
— ADC (SSI1) Interface: Master mode only; SPI$^{®1}$ and Microwire$^{®2}$-compatible (128 kbps operation)
— Audio Codec interface (64 kbps operation); for 18 MHz operation only.

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[1] SPI is a registered trademark of Motorola$^{®}$.
[2] Microwire is a registered trademark of National Semiconductor$^{®}$.

■ **27-bit general-purpose I/O**
— Three 8-bit and one 3-bit GPIO port
— Supports scanning keyboard matrix

■ **Two UARTs (16550 type)**
— Supports bit rates up to 115.2 kbps
— Contains two 16-byte FIFOs for Tx and Rx
— UART1 supports modem control signals

■ **SIR (up to 115.2 kbps) infrared encoder**
— IrDA (Infrared Data Association) SIR protocol encoder can be optionally switched into Tx and Rx signals of UART1

■ **DC-to-DC converter interface**
— Provides two 96-kHz clock outputs with programmable duty ratio (from 1-in-16 to 15-in-16)

■ **Two-timer counters**

■ **3.3 V at 18.432 MHz and 2.7 V at 13 MHz**

■ **208-pin LQFP and 256-ball PBGA packages**

■ **Evaluation kit available with BOM, schematics, and design database**

■ **Support for up to two ultra-low-power CL-PS6700 PC Card controllers**

OVERVIEW (cont.)

Power Management

The CL-PS7111 is designed for ultra-low-power operation. There are three basic power states:

● **Operating/Normal** — This state is the full performance state. All the clocks and peripheral logic are enabled.

● **Idle** — This state is the same as the Operating state, except the CPU clock is halted while waiting for an event such as a key press.

● **Standby** — This state is equivalent to the computer being switched off (no display), and the main oscillator shut down. An event such as a key press can wake-up the processor.

Memory Interfaces

There are two main external memory interfaces and a DMA controller that fetches video display data for the LCD controller from main DRAM memory.

The SRAM/ROM-style interface has programmable wait-state timings and includes burst-mode capability, with six chip selects decoding six 256-Mbyte sec-

tions of addressable space. For maximum flexibility, each bank can be specified to be 8, 16, or 32 bits wide to enable the use of low-cost memory in a 32-bit system. The system can have an 8-bit-wide boot option to optimize memory size. The on-chip boot ROM can be used in manufacturing to serially download system code into on-board FLASH.

The programmable 16- or 32-bit-wide DRAM interface allows direct connection of up to two banks of DRAM, each bank containing up to 256 Mbytes. To assure the lowest possible power consumption, the CL-PS7111 supports self-refresh DRAMs, which are placed in a low-power state by the device when it enters low-power Standby mode.

Serial Interfaces

For RS-232 serial communications, the CL-PS7111 includes two 16550-type UARTs, both of which have two 16-byte FIFOs for receive and transmit data. The UARTs support bit rates up to 115.2 kbps. An IrDA SIR protocol encoder/decoder can be optionally switched into the Rx/Tx signals to/from one of

OVERVIEW *(cont.)*

the UARTs to enable these signals to drive an infra-red communication interface directly.
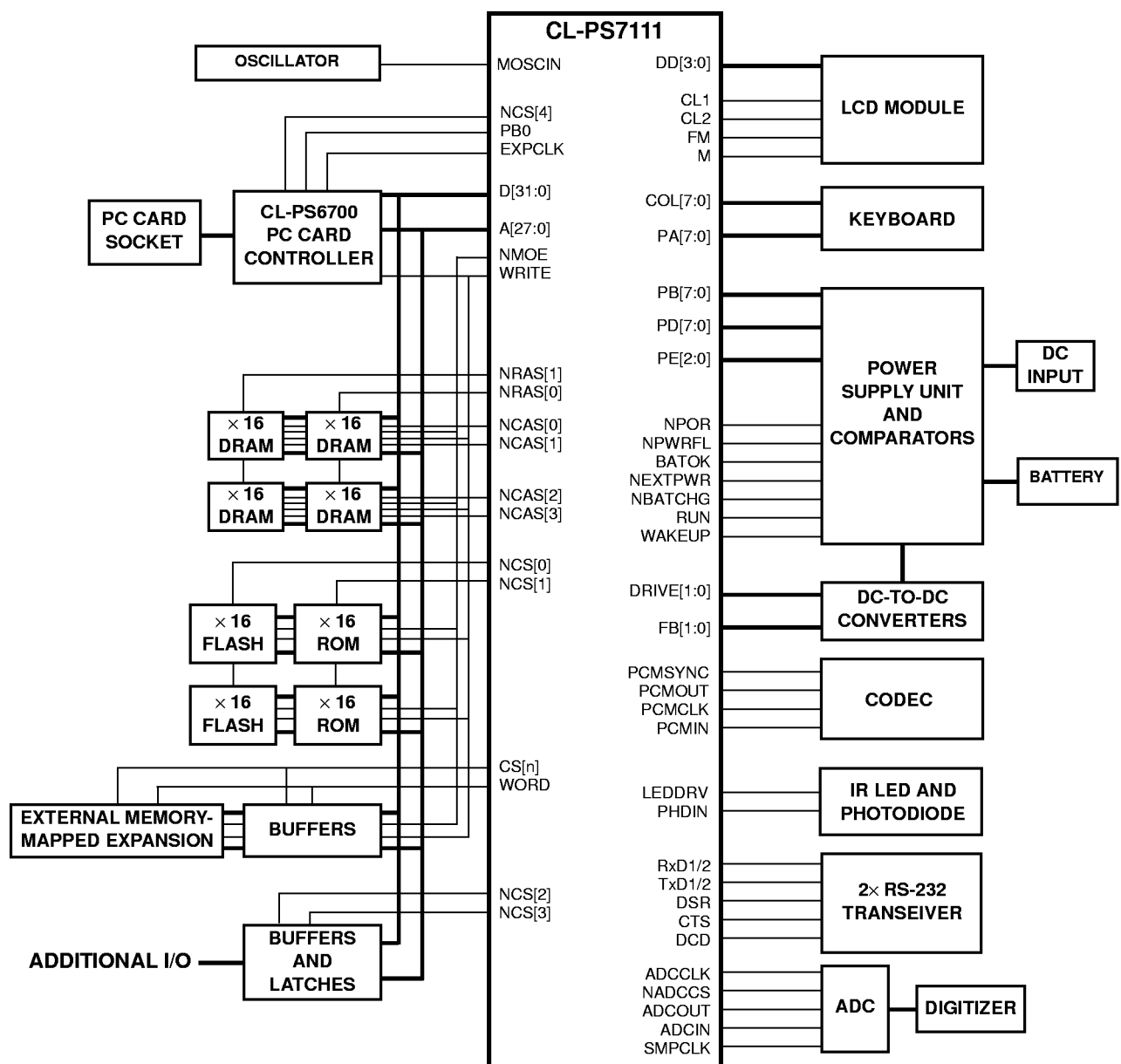
A full-duplex codec interface allows direct connection of a standard audio codec chip to the CL-PS7111, allowing storage and playback of sound. A separate synchronous serial interface supports two industry-standard protocols (SPI® and Microwire®) for interfacing to standard devices (like an ADC), allowing for peripheral expansion (for example, a digitizer pen).

Packaging

The CL-PS7111 is available in a 208-pin LQFP package and a 256-ball PBGA package.

System Design

As shown in the system block diagram below, simply adding desired memory and peripherals to the highly integrated CL-PS7111 completes a low-power device system board. All the interface logic is integrated on-chip.

A CL-PS7111–Based System