8V 2W GaAs Power Amplifier Die (4.5 - 7.1 GHz)
ITT6401D

FEATURES

- Broadband Performance
- High Linear Power (P1dB): 33 dBm typical
- High Power Added Efficiency: 40% typical at P1dB
- High Linear Gain: 18 dB typical
- Efficient performance with 3 to 10 Volt power supply
- 50 Ω Input/Output Impedance
- Self-Aligned MSAG® MESFET Process
- Unconditionally stable

DESCRIPTION

The ITT6401D is a two stage MMIC power amplifier fabricated on GaAsTEK's mature GaAs Self-Aligned MSAG ® MESFET Process. This product is fully matched to 50 ohms on both the input and the output and can be used as either a driver or an output stage amplifier. Although it can be used for several different applications, it is ideally suited for VSAT and ISM applications.

MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Drain Supply Voltage	V_{DD}	12V	Vdc
DC Gate Supply Voltage	V_{GG}	-4V	Vdc
RF Input Power	P_{IN}	200	mW
Junction Temperature (See maximum operating temperature chart in Fig. 5)	T_J	+175	°C
Storage Temperature	T_{STG}	-40 to +175	°C

ELECTRICAL CHARACTERISTICS V_{DD}=8.0 V, I_{DQ}=360 mA, P_{IN}=18 dBm, T_A=25 °C

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency	f	4.5	—	7.1	GHz
Load Power	P_{OUT}	33	34	—	dBm
Power Gain	G_P	15	16	—	dB
Power Gain Variation Over Frequency		—	1	1.5	dB
Power Added Efficiency	η	39	47	—	%
Drain Current	I_{DS}		660	—	mA
Gate Bias Voltage (No RF Input)	V_{GG}	-3.1	-2.1	-1.1	V
Gate Current	I_{GG}	-4	1	4	mA
Input VSWR		—	2.1:1	3:1	
Harmonics (f_o=5.5 GHz, P_{OUT}=34 dBm)	$2f_o$ $3f_o$	— —	-25 -27	-20 -23	dBc dBc
Thermal Resistance (Junction of 2nd stage FET to $T_{CARRIER}$, Note 1)	R_{TH}	—	20	—	°C/W
Noise Figure	NF	—	8.8	—	dB
Third-Order Intercept Point (I_{DQ}=525 mA)	TOI	—	43	—	dBm
Stability (P_{IN}= 5 to 20 dBm, V_{DD}=3 to 10 V, Load VSWR = 3:1)	—	All non-harmonically related outputs more than 70dB below desired signal			

Note 1: R_{TH} includes the thermal resistance between the bottom of the die and the carrier, assuming the die attachment guidelines on page 3 are followed. The second stage FET determines the overall thermal performance. Therefore, when performing thermal calculations, the dissipated power needs only to be calculated for the amplifier's 2nd stage.

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TYPICAL CHARACTERISTICS

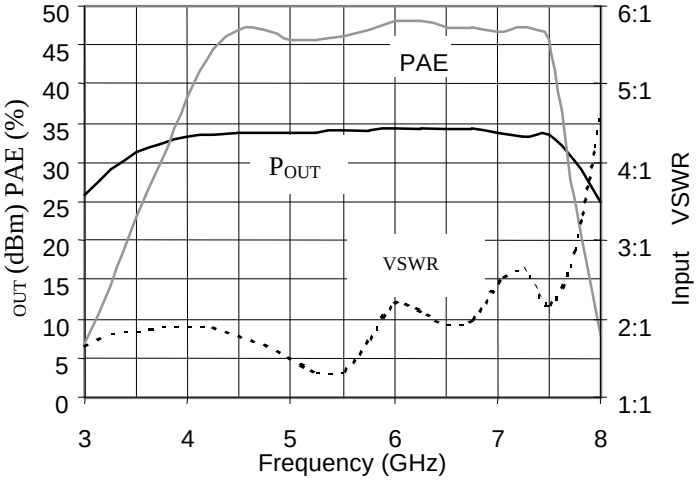

Figure 1. Output power, efficiency, and input VSWR vs. frequency

Conditions for Figure 1:
V_{DD} = 8V, I_{DQ} = 360 mA (no RF), P_{IN} = 18 dBm

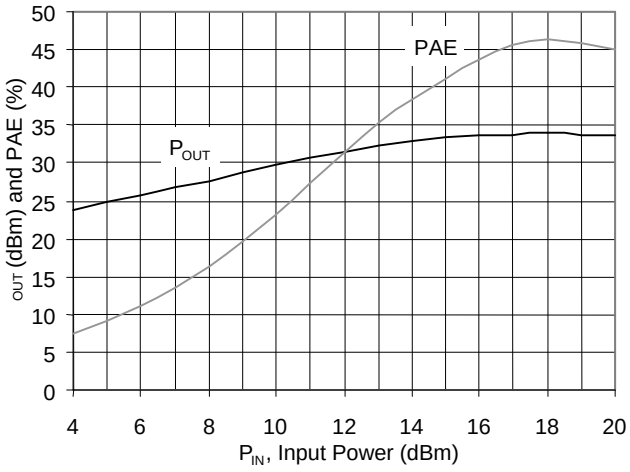

Figure 2. Output power and efficiency vs. input power

Conditions for Figure 2:
V_{DD} = 8V, I_{DQ} = 360 mA (no RF), f = 5.5 GHz

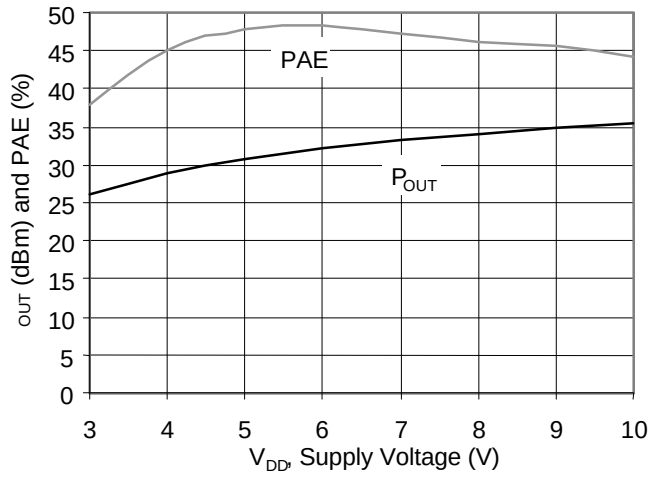

Figure 3. Output power and efficiency vs. supply voltage

Conditions for Figure 3:
I_{DQ} = 360 mA (no RF), P_{IN} = 18 dBm, f = 5.5 GHz

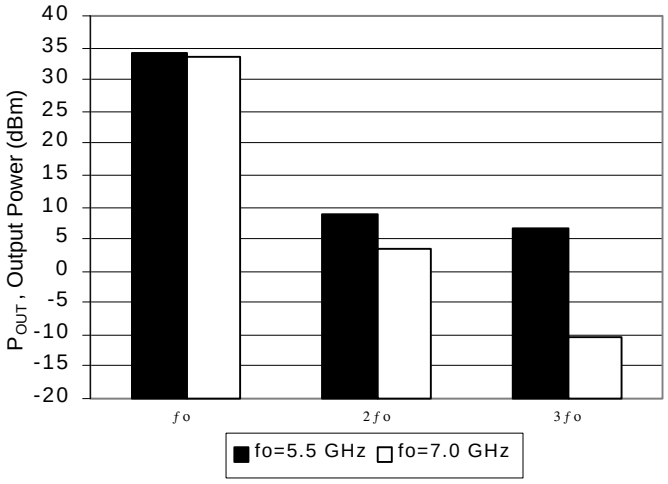

Figure 4. Harmonics

Conditions for Figure 4:
V_{DD} = 8V, I_{DQ} = 360 mA (no RF), P_{IN} = 18 dBm

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APPLICATION INFORMATION

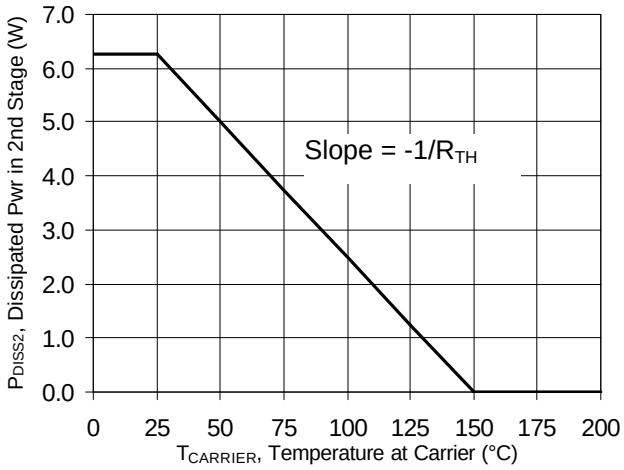

Figure 5. Maximum operating temperature

Conditions for Figure 5.

- $P_{DISS2} = I_{DD2}*V_{DD} – P_{OUT}$, which refers to the dissipated power in the hottest area of the die (Stage 2 FET)
- I_{DD2} is the supply current consumed by the second stage FET and is typically 80% of I_{DD}.

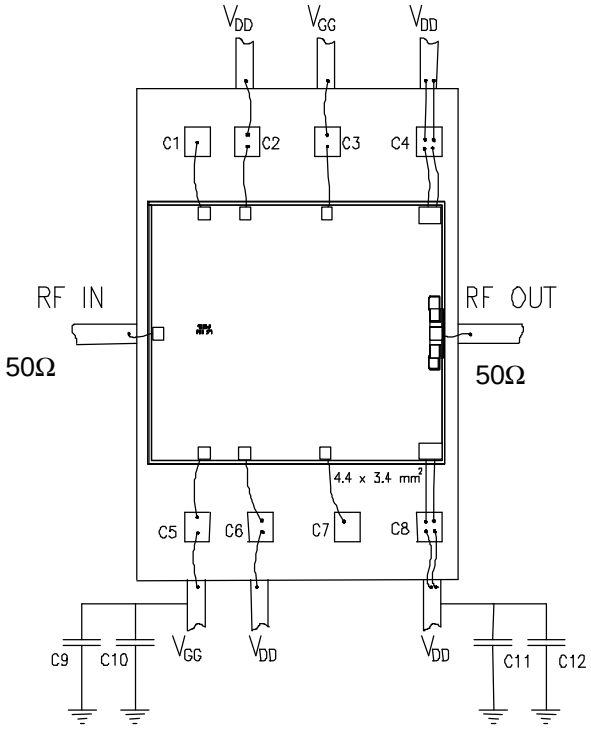

Figure 6. Bonding diagram

List of components:
C1 thru C8 = 100pF single layer ceramic chip capacitor
C9 = C11 = 0.1 uF ceramic chip capacitor
C10 = C12 = 5000 pF capacitor

Assembly:

Chip dimensions: 4.4mm x 3.4mm, .003" thickness.

Die attach: Use AuSn (80/20) 1 mil. preform solder. Limit time @ 300 °C to less than 5 minutes.

Wirebonding: Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.

Biasing:

1. User must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.
2. Nominal bias is I_{DQ}=360mA (10% IDSS) at +8.0 Volts on V_{DD}. This requires a typical V_{GG} bias of –2.1 Volts (no RF input drive).

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