

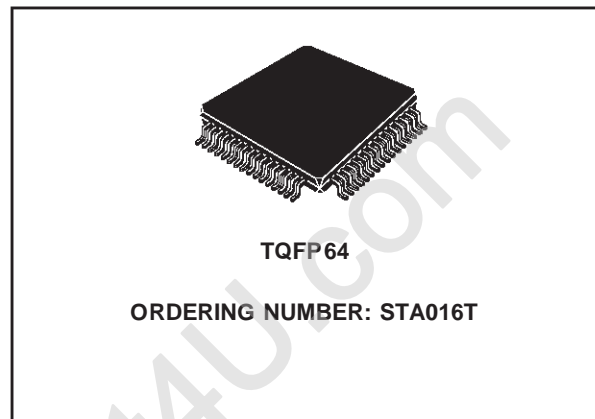


## STA016T

# MPEG 2.5 LAYER III AUDIO DECODER SUPPORTING CD-ROM CAPABILITY & ADPCM

PRODUCT PREVIEW

- SINGLE CHIP MPEG LAYER 3 DECODER SUPPORTING:
  - All features specified for Layer III in ISO/IEC 11172-3 (MPEG 1 Audio)
  - All features specified for Layer III in ISO/IEC 13818-3.2 (MPEG 2 Audio)
  - Lower sampling frequencies syntax extension, (not specified by ISO) called MPEG 2.5
- DECODES LAYER III STEREO CHANNELS, DUAL CHANNEL, SINGLE CHANNEL (MONO)
- SUPPORTING ALL THE MPEG 1 & 2 SAMPLING FREQUENCIES AND THE EXTENSION TO MPEG 2.5:48, 44.1,32, 24,22.05, 16, 12,11. 025, 8 KHz
- ACCEPTS MPEG 2.5 LAYER III ELEMENTARY COMPRESSED BITSTREAM WITH DATA RATE FROM 8 Kbit/s UP TO 320 Kbit/s
- BYPASS MODE FOR EXTERNAL AUXILIARY AUDIO SOURCE
- ADPCM ENCODING/DECODING CAPABILITY:
  - sample frequency from 8 kHz to 32 kHz
  - sample size from 8 bits to 32 bits
  - encoding algorithm: DVI, ITU-G726 pack (G723-24, G721,G723-40)
- EMBEDDED ISO9660 LAYER FOR FILE-SYSTEM DECODING (JOLIET)
- EMBEDDED CD-ROM DECODER BLOCKS INCLUDING ECC/EDC CAPABILITY
- FLEXIBLE I<sup>2</sup>S INPUT INTERFACE FOR EASY CONNECTION WITH MOST CD-SERVO DEVICES
- EMBEDDED BROWSING COMMAND INTERPRETER FOR EASY FILE-SYSTEM BROWSING
- CUE-SHEET CAPABILITY UP TO 100 ENTRIES
- BROWSER COMMAND INTERPRETER (BCI)
  - Parent Dir
  - Enter Dir
  - Previous Entry
  - Next Entry
  - Get Record Infos



- EASY PROGRAMMABLE GPSO INTERFACE (MONO/STEREO) FOR ENCODED DATA UP TO 5Mbit/s
- DIGITAL VOLUME
- BASS & TREBLE CONTROL
- SERIAL BITSTREAM INPUT INTERFACE
- EASY PROGRAMMABLE ADC INPUT INTERFACE
- SERIAL PCM OUTPUT INTERFACE (I<sup>2</sup>S AND OTHER FORMATS)
- PLL FOR INTERNAL CLOCK AND FOR OUTPUT PCM CLOCK GENERATION
- CRC CHECK AND SYNCHRONISATION ERROR DETECTION WITH SOFTWARE INDICATORS
- I<sup>2</sup>C CONTROL BUS
- LOW POWER 2.4V CMOS TECHNOLOGY WITH 3.3V TOLERANT AND CAPABLE I/O
- FAST FORWARD AND PAUSE CAPABILITIES

### APPLICATIONS

- AUDIO CD PLAYERS
- MULTIMEDIA PLAYERS
- CD-ROM PLAYERS
- CAR RADIO PLAYERS

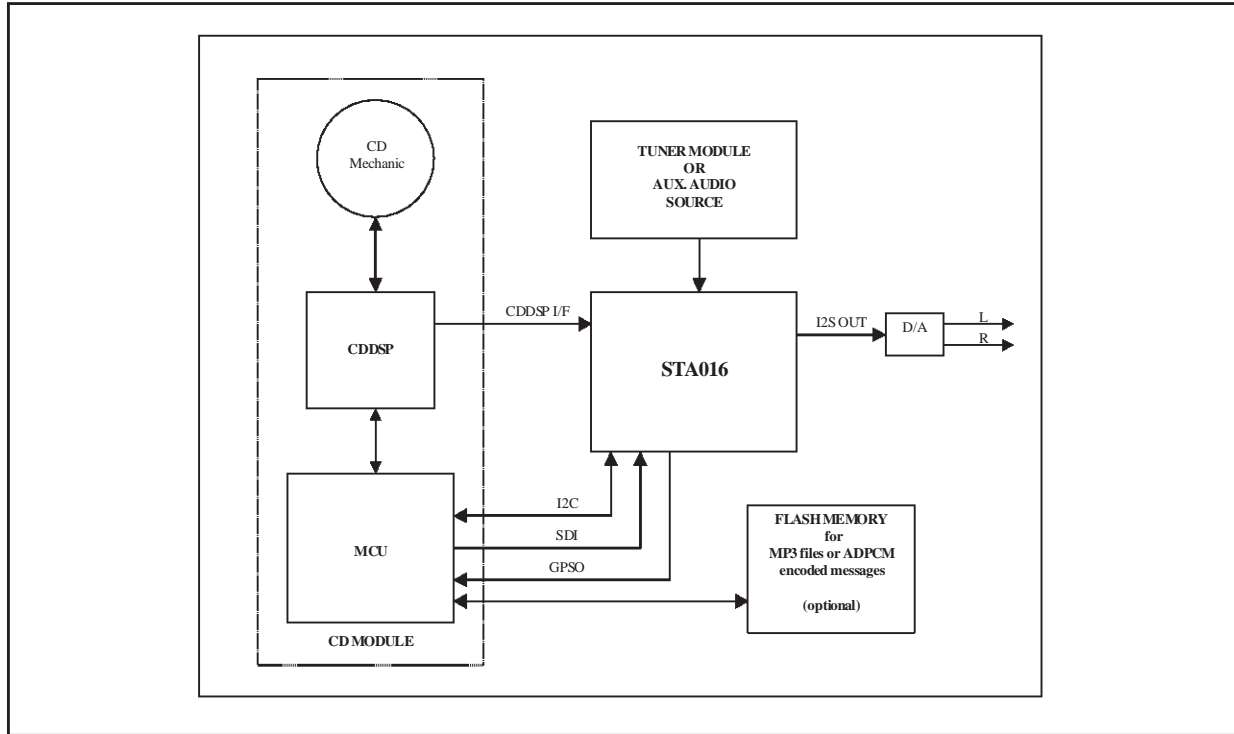
# STA016T

## DESCRIPTION

The STA016 is a single chip MPEG 1, 2 and 2.5 Layer III audio decoder with embedded CDROM decoding capability. It can be easily connected to most existing CDDSP devices via a software configurable serial link. A typical application block diagram is show in Figure 1. Besides MPEG decoding the device can also perform ADPCM encoding/decoding from different audio sources and the encoded stream, for instance, can be stored on an external flash memory.

A useful bypass mode allow using this device also as an audio processor for volume and tone controls.

**Figure 1. Typical CD-Player application**



## ABSOLUTE MAXIMUM RATINGS

| Symbol                         | Parameter                               | Value                        | Unit |
|--------------------------------|---|------------------------------|------|
| V <sub>DD</sub>                | Digital Power Supply at 2.5V (nominal)  | -0.5 to 3.3                  | V    |
| V <sub>CC</sub>                | Digital Power Supply at 3.3V (nominal)  | -0.5 to 4                    | V    |
| P <sub>LL-V<sub>CC</sub></sub> | Analog Supply Voltage at 2.5V (nominal) | -0.5 to 3.3                  | V    |
| V <sub>IH/VIL</sub>            | Voltage on input pins (3.3V pads)       | -0.5 to V <sub>CC</sub> +0.5 | V    |
| T <sub>stg</sub>               | Storage Temperature                     | -40 to +150                  | °C   |
| T <sub>op</sub>                | Operative ambient temp                  | -40 to +85(*)                | °C   |
| T <sub>j</sub>                 | Operating Junction Temperature          | -40 to 125                   | °C   |

(\*) guaranteed by design

## THERMAL DATA

| Symbol                | Parameter                              | Value | Unit |
|-----------------------|--|-------|------|
| R <sub>th j-amb</sub> | Thermal resistance Junction to Ambient | 85    | °C/W |

## 1 OVERVIEW

The device can decode/process data coming from three possible sources, as showed in Figure 2:

- **CDDSP serial link:** using this input interface, besides MP3 encoded data CD, it's possible to playback also standard Audio CD using the available volume and tone equalizer features of the device and allowing the use of only one D/A converter with no external analog switch.
- **SDI input interface:** through this input interface it's possible to decode any MP3 bitstream coming, for instance, from an external flash memory. This same interface is also used to decode ADPCM streams.
- **I<sup>2</sup>S input interface:** this interface can be used both to encode an external audio source (with variable compression based on 4 different ADPCM algorithm) or to process an external audio source (tuner, for instance) through the DSP based volume and tone controls: this BYPASS mode can avoid the use of additional D/A converters or postprocessing units.

### 1.1 MP3 decoder engine

The MP3 decoder engine is able to decode any Layer III compliant bitstream: MPEG1, MPEG2 and MPEG2.5 streams are supported.

Decoded audio data goes through a software volume control and a two-band equalizer blocks before feeding the output I<sup>2</sup>S interface. This results in no need for an external audio processor.

**Table 1. MPEG Sampling Rates (KHz)**

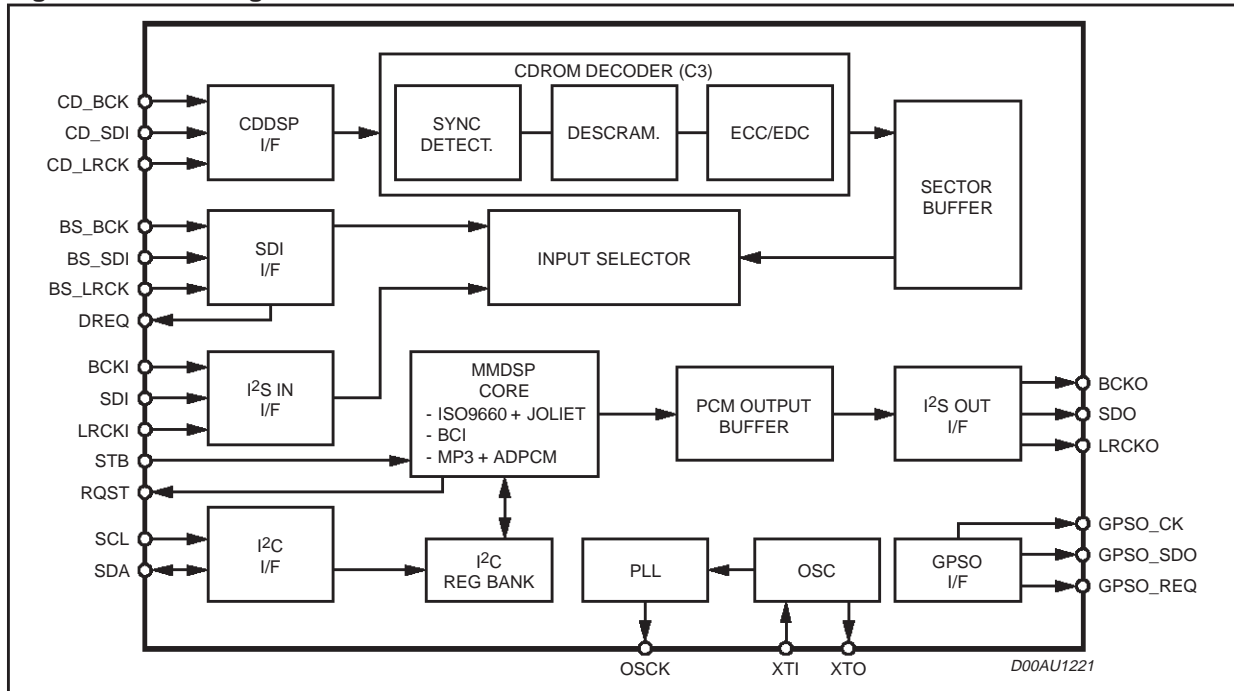
| MPEG 1 | MPEG 2 | MPEG 2.5 |
|--------|--------|----------|
| 48     | 24     | 12       |
| 44.1   | 22.05  | 11.025   |
| 32     | 16     | 8        |

### 1.2 ADPCM encoder/decoder engine

This device also embeds a multistandard ADPCM encoder/decoder supporting different sample rates (from 8 KHz up to 32 KHz) and different sample sizes (from 8 bit to 32 bits). During encoding process two different interfaces can be used to feed data: the serial input interface (same interface used also to feed MP3 bitstream) or the ADC input interface, which provides a seamless connection with an external A/D converter. The currently used interface is selected via I2C bus.

Also to retrieve encoded data a specific interface is available: the fast GPSO output interface. GPSO interface is able to output data with a bitrate up to 5 Mbit/s and its control pins (GPSO\_SCKR, GPSO\_DATA and GPSO\_REQ) can be configured in order to easily fit the target application.

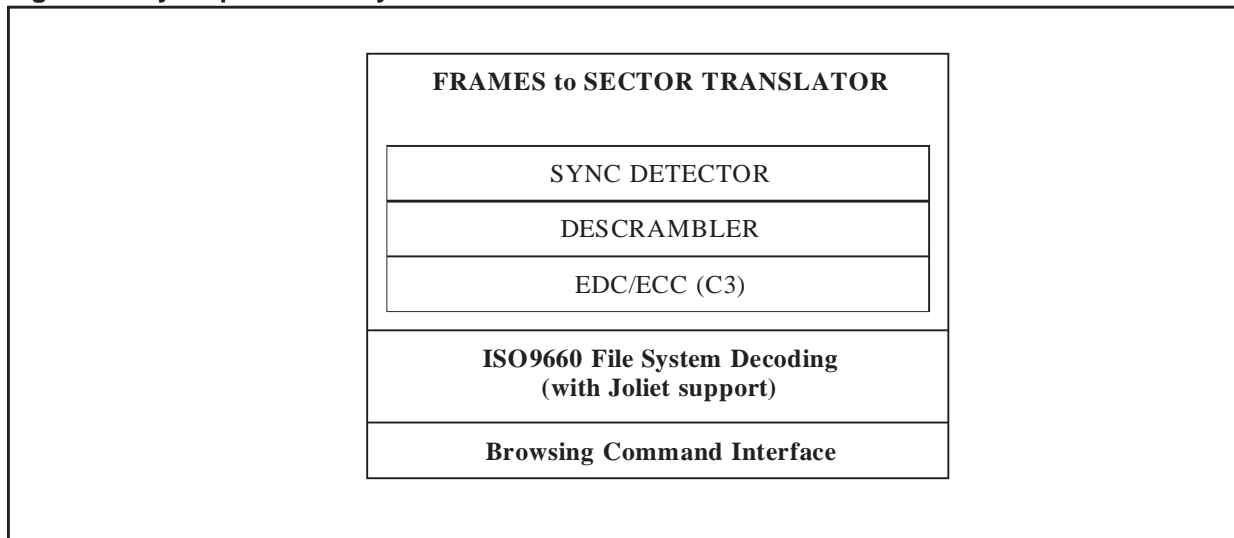
Figure 2. Block Diagram



The basic functions of the device can be fully operated via the I<sup>2</sup>C bus. Besides that the GPSO interface can be used to move huge amount of data this fast and flexible interface can achieve transfer rates up to 5 Mbit/s.

The embedded DSP firmware implements all the layers required to decode a standard data CD, as shown in the Figure 3:

Figure 3. Layers performed by embedded DSP firmware



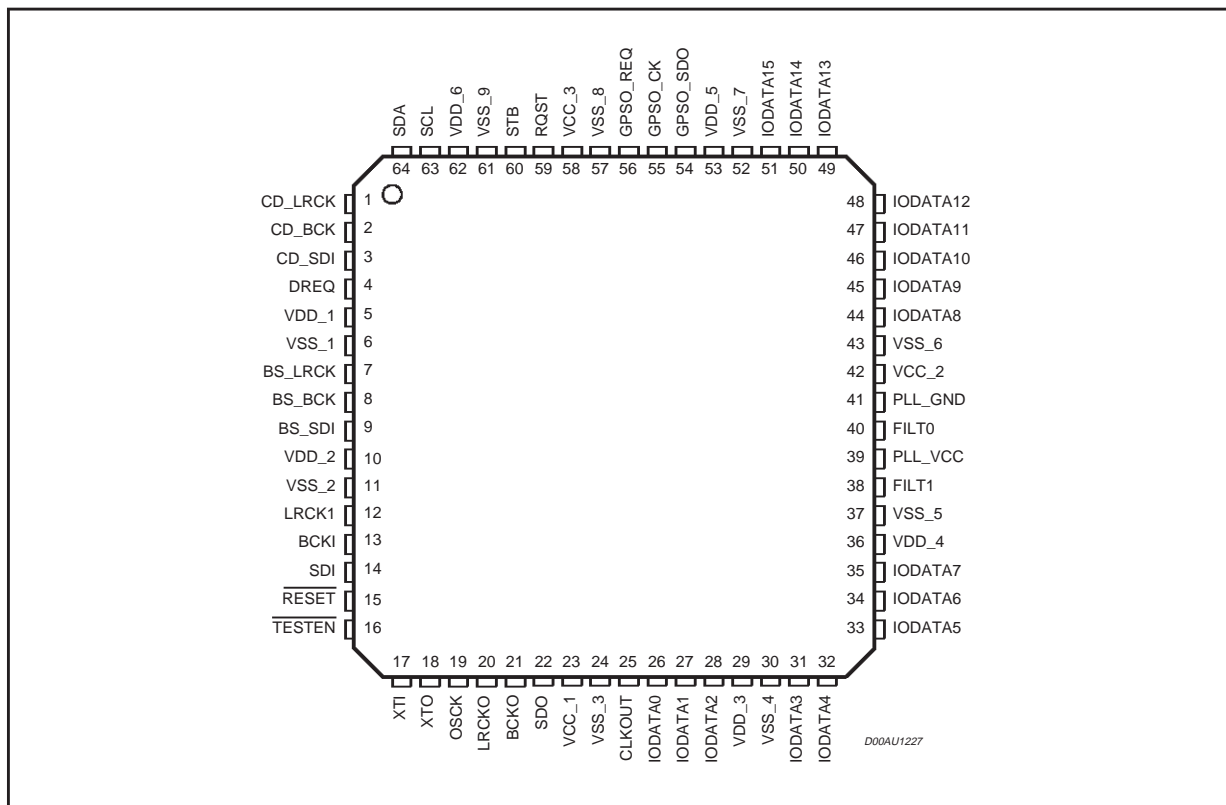
The whole CDROM and file-system decoding task is performed by embedded firmware. The application MCU, basically, must manage CDDSP device according to STA016 requests. Three basic command flows exist:

- MCU -> STA016: commands used to handle decoder operation and to ask for specific information like filename, filelength, sector raw data, etc. This flow will use I<sup>2</sup>C (GPSO for special operations) interface.
- STA016 -> MCU: this channel is used to retrieve inquired information and to inform MCU that a CDDSP

specific operation must be performed (like pick-up repositioning). This flow is based on I<sup>2</sup>C link plus an additional interrupt signal in order to avoid time consuming polling techniques.

- MCU -> CDDSP: the CDDSP management is fully up to the application MCU. This architecture allows maximum flexibility and easy migration from existing CDPlayers to MP3 CDPlayers.

**PIN CONNECTION**



**PIN DESCRIPTION**

| PIN                     | Pin Name | Type | Description                          | Sourde/Dest |
|-------------------------|----------|------|--------------------------------------|-------------|
| <b>CDDSP interface</b>  |          |      |                                      |             |
| 1                       | CD_LRCK  | I    | DSP Interface left/right Clock       | From DSP    |
| 3                       | CD_SDI   | I    | DSP interface serial data            | From DSP    |
| 2                       | CD_BCK   | I    | DSP interface bit clock              | From DSP    |
| <b>SDI interface</b>    |          |      |                                      |             |
| 9                       | BS_SDI   | I    | Bitstream interface serial data      | From MCU    |
| 7                       | BS_LRCK  | I    | Bitstream interface left/right Clock | From MCU    |
| 8                       | BS_BCK   | I    | Bitstream interface clock            | From MCU    |
| 4                       | DREQ     | O    | Bitstream data request               | To MCU      |
| <b>PCM IN interface</b> |          |      |                                      |             |
| 13                      | BCKI     | I    | ADC bit clock                        | From ADC    |

**PIN DESCRIPTION (continued)**

| <b>PIN</b>               | <b>Pin Name</b> | <b>Type</b> | <b>Description</b>             | <b>Sourde/Dest</b> |
|--------------------------|-----------------|-------------|--------------------------------|--------------------|
| 14                       | SDI             | I           | ADC serial data                | From ADC           |
| 12                       | LRCKI           | I           | ADC left/right Clock           | From ADC           |
| <b>PCM OUT interface</b> |                 |             |                                |                    |
| 20                       | LRCKO           | O           | DAC Interface left/right Clock | To DAC             |
| 22                       | SDO             | O           | DAC serial data                | To DAC             |
| 21                       | BCKO            | O           | DAC bit clock                  | To DAC             |
| 19                       | OSCK            | O           | DAC oversampling clock         | To DAC/ADC         |
| <b>GPSO interface</b>    |                 |             |                                |                    |
| 55                       | GPSO_CK         | I           | GPSO bit clock                 | From MCU           |
| 54                       | GPSO_SDO        | O           | GPSO serial data               | To MCU             |
| 56                       | GPSO_REQ        | O           | GPSO request signal            | To MCU             |
| <b>GPIO interface</b>    |                 |             |                                |                    |
| 26                       | IODATA0         | I/O         | GPIO DATA0                     |                    |
| 27                       | IODATA1         | I/O         | GPIO DATA1                     |                    |
| 28                       | IODATA2         | I/O         | GPIO DATA2                     |                    |
| 31                       | IODATA3         | I/O         | GPIO DATA3                     |                    |
| 32                       | IODATA4         | I/O         | GPIO DATA4                     |                    |
| 33                       | IODATA5         | I/O         | GPIO DATA5                     |                    |
| 34                       | IODATA6         | I/O         | GPIO DATA6                     |                    |
| 35                       | IODATA7         | I/O         | GPIO DATA7                     |                    |
| 44                       | IODATA8         | I/O         | GPIO DATA8                     |                    |
| 45                       | IODATA9         | I/O         | GPIO DATA9                     |                    |
| 46                       | IODATA10        | I/O         | GPIO DATA10                    |                    |
| 47                       | IODATA11        | I/O         | GPIO DATA11                    |                    |
| 48                       | IODATA12        | I/O         | GPIO DATA12                    |                    |
| 49                       | IODATA13        | I/O         | GPIO DATA13                    |                    |
| 50                       | IODATA14        | I/O         | GPIO DATA14                    |                    |
| 51                       | IODATA15        | I/O         | GPIO DATA15                    |                    |

## PIN DESCRIPTION (continued)

| PIN                        | Pin Name | Type | Description                        | Source/Dest |
|----------------------------|----------|------|------------------------------------|-------------|
| <b>HANDSHAKE SIGNALS</b>   |          |      |                                    |             |
| 60                         | STB      | I    | Strobe signal                      | From MCU    |
| 59                         | RQST     | O    | I2C data signal                    | To MCU      |
| <b>I<sup>2</sup>C LINK</b> |          |      |                                    |             |
| 63                         | SCL      | I    | I2C clock signal                   | From MCU    |
| 64                         | SDA      | I/O  | I2C data signal                    | To MCU      |
| <b>MISCELLANEOUS</b>       |          |      |                                    |             |
| 17                         | XTI      | I    | Oscillator input                   |             |
| 18                         | XTO      | O    | Oscillator output                  |             |
| 25                         | CLKOUT   | O    | Buffered output clock              |             |
| 15                         | -RESET   | I    | Reset                              |             |
| 16                         | -TESTEN  | I    | Reserved for test purpose          |             |
| 40                         | FILT0    | I    | PLL external filter                |             |
| 38                         | FILT1    |      | PLL external filter                |             |
| <b>POWER SUPPLY</b>        |          |      |                                    |             |
| 39                         | PLL_VCC  |      | Digital supply (2.5V Power Supply) |             |
| 41                         | PLL_GND  |      | Ground                             |             |
| 5                          | VDD_1    |      | Digital supply (2.5V Power Supply) |             |
| 10                         | VDD_2    |      | Digital supply (2.5V Power Supply) |             |
| 29                         | VDD_3    |      | Digital supply (2.5V Power Supply) |             |
| 36                         | VDD_4    |      | Digital supply (2.5V Power Supply) |             |
| 53                         | VDD_5    |      | Digital supply (2.5V Power Supply) |             |
| 62                         | VDD_6    |      | Digital supply (2.5V Power Supply) |             |
| 23                         | VCC_1    |      | Digital supply (3.3V Power Supply) |             |
| 42                         | VCC_2    |      | Digital supply (3.3V Power Supply) |             |
| 58                         | VCC_3    |      | Digital supply (3.3V Power Supply) |             |
| 6                          | VSS_1    |      | Ground                             |             |
| 11                         | VSS_2    |      | Ground                             |             |
| 24                         | VSS_3    |      | Ground                             |             |
| 30                         | VSS_4    |      | Ground                             |             |
| 37                         | VSS_5    |      | Ground                             |             |
| 43                         | VSS_6    |      | Ground                             |             |
| 52                         | VSS_7    |      | Ground                             |             |
| 57                         | VSS_8    |      | Ground                             |             |
| 61                         | VSS_9    |      | Ground                             |             |

**ELECTRICAL CHARACTERISTICS**

 (T<sub>amb</sub> = 25°C; R<sub>g</sub> = 50Ω unless otherwise specified)

**DC OPERATING CONDITIONS**

| Symbol              | Parameter            | Value      | Unit |
|---------------------|----------------------|------------|------|
| V <sub>DD</sub>     | Power Supply Voltage | 2.5 ± 0.25 | V    |
| V <sub>CC</sub>     | Power Supply Voltage | 3.3 ± 0.3  | V    |
| PLL_V <sub>CC</sub> | Power Supply Voltage | 2.5 ± 0.25 | V    |

**GENERAL INTERFACE ELECTRICAL CHARACTERISTICS**

| Symbol           | Parameter  | Test Condition                   | Min. | Typ. | Max. | Unit | Note |
|------------------|--|----------------------------------|------|------|------|------|------|
| I <sub>IL</sub>  | Low Level Input Current<br>Without pull-up device  | V <sub>i</sub> = 0V              | -10  |      | 10   | μA   | 1    |
| I <sub>IH</sub>  | High Level Input Current<br>Without pull-up device | V <sub>i</sub> = V <sub>DD</sub> | -10  |      | 10   | μA   | 1    |
| V <sub>esd</sub> | Electrostatic Protection                           | Leakage < 1μA                    | 2000 |      |      | V    | 2    |

**Note 1:** The leakage currents are generally very small, < 1nA. The value given here is a maximum that can occur after an electrostatic stress on the pin.

**Note 2:** Human Body Model.

**DC ELECTRICAL CHARACTERISTICS**

| Symbol          | Parameter                 | Test Condition        | Min.                 | Typ. | Max.                | Unit | Note |
|-----------------|---------------------------|-----------------------|----------------------|------|---------------------|------|------|
| V <sub>IL</sub> | Low Level Input Voltage   |                       |                      |      | 0.2*V <sub>CC</sub> | V    |      |
| V <sub>IH</sub> | High Level Input Voltage  |                       | 0.8*V <sub>CC</sub>  |      |                     | V    |      |
| V <sub>oL</sub> | Low Level Output Voltage  | I <sub>oL</sub> = Xma |                      |      | 0.4V                | V    | 1, 2 |
| V <sub>oH</sub> | High Level Output Voltage |                       | 0.85*V <sub>CC</sub> |      |                     | V    | 1, 2 |

**Note1:** Takes into account 200mV voltage drop in both supply lines.

**Note 2:** X is the source/sink current under worst case conditions and is reflected in the name of the I/O cell according to the drive capability.

| Symbol          | Parameter                     | Test Condition                                | Min. | Typ. | Max. | Unit | Note |
|-----------------|-------------------------------|---|------|------|------|------|------|
| I <sub>pu</sub> | Pull-up current               | V <sub>i</sub> = 0V; pin numbers 7, 24 and 26 | -25  | -66  | -125 | μA   | 1    |
| R <sub>pu</sub> | Equivalent Pull-up Resistance |   |      | 50   |      | kΩ   |      |

Note 1: Min. condition: V<sub>DD</sub> = 2.7V, 125°C Min process Max. condition: V<sub>DD</sub> = 3.6V, -20°C Max.

**POWER DISSIPATION**

| Symbol         | Parameter                                 | Test Condition         | Min. | Typ.   | Max. | Unit | Note |
|----------------|---|------------------------|------|--------|------|------|------|
| P <sub>D</sub> | Power Dissipation@ V <sub>DD</sub> = 2.4V | Sampling_freq ≤ 24 kHz |      | t.b.d. |      | mW   |      |
|                |   | Sampling_freq ≤ 32 kHz |      | t.b.d. |      | mW   |      |
|                |   | Sampling_freq ≤ 48 kHz |      | t.b.d. |      | mW   |      |



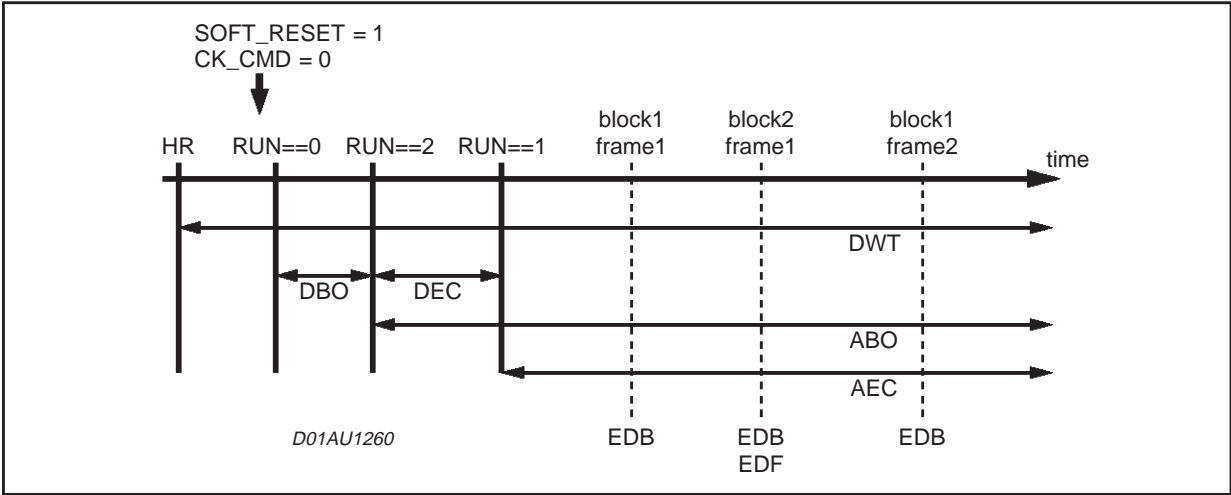
## 2 HOST REGISTERS

The following table gives a description of STA016 register list.

The STA016 device includes 256 I<sup>2</sup>C registers. In this document, only the user-oriented registers are described. The undocumented registers are reserved or unused. These registers must never be accessed (in Read or in Write mode). The Read-Only registers must never be written

We can split the data flux in different time periods (see following diagram) meanwhile host registers can be read or written :

- DWT : During Whole Time (at any time during process).
- DEC : During External Config (period between RUN=2 and RUN=1).
- DBO : During Boot (period between RUN=0 and RUN=2).
- ABO : After B0ot (period after RUN=1).
- AEC : After External Config (period after RUN=2).
- EDF : Every Decoded Frame (each time a frame has been decoded).
- EDB : Every Decoded Block (each time a block has been decoded).



**REGISTER MAP BY FUNCTION**

| Register function        | Hex  | Dec | Name                 | Type | When |
|--------------------------|------|-----|----------------------|------|------|
| VERSION                  | 0x00 | 0   | VERSION              | RO   | DWT  |
|                          | 0x01 | 1   | IDENT                | RO   | DWT  |
|                          | 0xD3 | 211 | SOFT_VERSION         | RO   | DWT  |
| PLL_AUDIO_CONFIGURATION  | 0xDC | 220 | PLL_AUDIO_PEL_192    | RW   | DEC  |
|                          | 0xDD | 221 | PLL_AUDIO_PEH_192    | RW   | DEC  |
|                          | 0xDE | 222 | PLL_AUDIO_NDIV_192   | RW   | DEC  |
|                          | 0xDF | 223 | PLL_AUDIO_XDIV_192   | RW   | DEC  |
|                          | 0xE0 | 224 | PLL_AUDIO_MDIV_192   | RW   | DEC  |
|                          | 0xE1 | 225 | PLL_AUDIO_PEL_176    | RW   | DEC  |
|                          | 0xE2 | 226 | PLL_AUDIO_PEH_176    | RW   | DEC  |
|                          | 0xE3 | 227 | PLL_AUDIO_NDIV_176   | RW   | DEC  |
|                          | 0xE4 | 228 | PLL_AUDIO_XDIV_176   | RW   | DEC  |
|                          | 0xE5 | 229 | PLL_AUDIO_MDIV_176   | RW   | DEC  |
| PLL_SYSTEM_CONFIGURATION | 0xE6 | 230 | PLL_SYSTEM_PEL_50    | RW   | DEC  |
|                          | 0xE7 | 231 | PLL_SYSTEM_PEH_50    | RW   | DEC  |
|                          | 0xE8 | 232 | PLL_SYSTEM_NDIV_50   | RW   | DEC  |
|                          | 0xE9 | 233 | PLL_SYSTEM_XDIV_50   | RW   | DEC  |
|                          | 0xEA | 234 | PLL_SYSTEM_MDIV_50   | RW   | DEC  |
|                          | 0xEB | 235 | PLL_SYSTEM_PEL_42_5  | RW   | DEC  |
|                          | 0xEC | 236 | PLL_SYSTEM_PEH_42_5  | RW   | DEC  |
|                          | 0xED | 237 | PLL_SYSTEM_NDIV_42_5 | RW   | DEC  |
|                          | 0xEE | 238 | PLL_SYSTEM_XDIV_42_5 | RW   | DEC  |
|                          | 0xEF | 239 | PLL_SYSTEM_MDIV_42_5 | RW   | DEC  |
| I2Sout_CONFIGURATION     | 0x66 | 102 | OUTPUT_CONF          | RW   | DEC  |
|                          | 0x67 | 103 | PCM_DIV              | RW   | DEC  |
|                          | 0x68 | 104 | PCM_CONF             | RW   | DEC  |
|                          | 0x69 | 105 | PCM_CROSS            | RW   | DEC  |
| GPSO_CONFIGURATION       | 0x66 | 102 | OUTPUT_CONF          | RW   | DEC  |
|                          | 0x6A | 106 | GPSO_CONF            | RW   | DEC  |
| I2Sin_CONFIGURATION      | 0x5A | 90  | INPUT_CONF           | RW   | DEC  |
|                          | 0x5B | 91  | I_AUDIO_CONFIG_1     | RW   | DEC  |
|                          | 0x5C | 92  | I_AUDIO_CONFIG_2     | RW   | DEC  |
|                          | 0x5D | 93  | I_AUDIO_CONFIG_3     | RW   | DEC  |

| Register function   | Hex  | Dec | Name              | Type | When |
|---------------------|------|-----|-------------------|------|------|
| CDBSA_CONFIGURATION | 0x5A | 90  | INPUT_CONF        | RW   | DEC  |
|                     | 0x5B | 91  | I_AUDIO_CONFIG_1  | RW   | DEC  |
|                     | 0x5C | 92  | I_AUDIO_CONFIG_2  | RW   | DEC  |
|                     | 0x5D | 93  | I_AUDIO_CONFIG_3  | RW   | DEC  |
|                     | 0x5E | 94  | I_AUDIO_CONFIG_4  | RW   | DEC  |
|                     | 0x5F | 95  | I_AUDIO_CONFIG_5  | RW   | DEC  |
|                     | 0x60 | 96  | I_AUDIO_CONFIG_6  | RW   | DEC  |
|                     | 0x61 | 97  | I_AUDIO_CONFIG_7  | RW   | DEC  |
|                     | 0x62 | 98  | I_AUDIO_CONFIG_8  | RW   | DEC  |
|                     | 0x63 | 99  | I_AUDIO_CONFIG_9  | RW   | DEC  |
|                     | 0x64 | 100 | I_AUDIO_CONFIG_10 | RW   | DEC  |
|                     | 0x65 | 101 | I_AUDIO_CONFIG_11 | RW   | DEC  |
| BSB_CONFIGURATION   | 0x59 | 89  | POL_REQ           | RW   | DEC  |
|                     | 0x5A | 90  | INPUT_CONF        | RW   | DEC  |
|                     | 0x5B | 91  | I_AUDIO_CONFIG_1  | RW   | DEC  |
| CD_CONFIGURATION    | 0x40 | 64  | BASIC_COMMAND     | WO   | AEC  |
|                     | 0x41 | 65  | FAST_FUNCTION_VAL | RW   | ABO  |
|                     | 0x42 | 66  | REQUIRED_TRACK    | RW   | ABO  |
|                     | 0x43 | 67  | REQUIRED_DIR      | RW   | ABO  |
|                     | 0x44 | 68  | PLAY_MODE         | RW   | ABO  |
|                     | 0x46 | 70  | TYPE_CD_EXT_REQ   | RO   | AEC  |
|                     | 0x47 | 71  | MINUTE_REQ        | RO   | AEC  |
|                     | 0x48 | 72  | SECOND_REQ        | RO   | AEC  |
|                     | 0x49 | 73  | SECTOR_REQ        | RO   | AEC  |
|                     | 0x4A | 74  | MINUTE_SPENT      | RO   | AEC  |
|                     | 0x4B | 75  | SECOND_SPENT      | RO   | AEC  |
|                     | 0x4C | 76  | SCANNING_TIME     | RW   | ABO  |
|                     | 0x4D | 77  | PLAY_LIST_INDEX   | RW   | ABO  |
|                     | 0x4E | 78  | PLAY_LIST_VALUE   | RW   | ABO  |

| Register function | Hex  | Dec | Name              | Type | When |
|-------------------|------|-----|-------------------|------|------|
|                   | 0x86 | 134 | CD_SONG_INFO_C1   | RO   | AEC  |
|                   | 0x87 | 135 | CD_SONG_INFO_C2   | RO   | AEC  |
|                   | 0x88 | 136 | CD_SONG_INFO_C3   | RO   | AEC  |
|                   | 0x89 | 137 | CD_SONG_INFO_C4   | RO   | AEC  |
|                   | 0x8A | 138 | CD_SONG_INFO_C5   | RO   | AEC  |
|                   | 0x8B | 139 | CD_SONG_INFO_C6   | RO   | AEC  |
|                   | 0x8C | 140 | CD_SONG_INFO_C7   | RO   | AEC  |
|                   | 0x8D | 141 | CD_SONG_INFO_C8   | RO   | AEC  |
|                   | 0x8E | 142 | CD_SONG_INFO_C9   | RO   | AEC  |
|                   | 0x8F | 143 | CD_SONG_INFO_C10  | RO   | AEC  |
|                   | 0x90 | 144 | CD_SONG_INFO_C11  | RO   | AEC  |
|                   | 0x91 | 145 | CD_SONG_INFO_C12  | RO   | AEC  |
|                   | 0x92 | 146 | CD_SONG_INFO_C13  | RO   | AEC  |
|                   | 0x93 | 147 | CD_SONG_INFO_C14  | RO   | AEC  |
|                   | 0x94 | 148 | CD_SONG_INFO_C15  | RO   | AEC  |
|                   | 0x95 | 149 | CD_SONG_INFO_C16  | RO   | AEC  |
|                   | 0x96 | 150 | CD_SONG_INFO_C17  | RO   | AEC  |
|                   | 0x97 | 151 | CD_SONG_INFO_C18  | RO   | AEC  |
|                   | 0x98 | 152 | CD_SONG_INFO_C19  | RO   | AEC  |
|                   | 0x99 | 153 | CD_SONG_INFO_C20  | RO   | AEC  |
|                   | 0x9A | 154 | CD_SONG_INFO_C21  | RO   | AEC  |
|                   | 0x9B | 155 | CD_SONG_INFO_C22  | RO   | AEC  |
|                   | 0x9C | 156 | CD_SONG_INFO_C23  | RO   | AEC  |
|                   | 0x9D | 157 | CD_SONG_INFO_C24  | RO   | AEC  |
|                   | 0x9E | 158 | CD_SONG_INFO_C25  | RO   | AEC  |
|                   | 0x9F | 159 | CD_SONG_INFO_C26  | RO   | AEC  |
|                   | 0xA0 | 160 | CD_SONG_INFO_C27  | RO   | AEC  |
|                   | 0xA1 | 161 | CD_SONG_INFO_C28  | RO   | AEC  |
|                   | 0xA2 | 162 | CD_SONG_INFO_C29  | RO   | AEC  |
|                   | 0xA3 | 163 | CD_SONG_INFO_C30  | RO   | AEC  |
|                   | 0xA4 | 164 | CD_SONG_INFO_C31  | RO   | AEC  |
|                   | 0xA5 | 165 | CD_SONG_INFO_C32  | RO   | AEC  |
|                   | 0xA6 | 166 | CD_SONG_TYPE_INFO | RO   | AEC  |

| Register function | Hex  | Dec | Name                | Type | When |
|-------------------|------|-----|---------------------|------|------|
|                   | 0xA7 | 167 | NB_OF_CUR_TRACK     | RO   | AEC  |
|                   | 0xA8 | 168 | NB_OF_CUR_DIR       | RO   | AEC  |
|                   | 0xA9 | 169 | CD_CUR_STATUS       | RO   | AEC  |
|                   | 0xAA | 170 | CD_TRACK_FORMAT     | RO   | AEC  |
|                   | 0xAB | 171 | CD_NB_OF_SUB_DIR    | RO   | AEC  |
|                   | 0xAC | 172 | CD_NB_OF_SUB_FILE   | RO   | AEC  |
|                   | 0xAD | 173 | DIRECTORY_LEVEL     | RO   | AEC  |
|                   | 0xAE | 174 | DIR_IDENTIFIER_B1   | RO   | AEC  |
|                   | 0xAF | 175 | DIR_IDENTIFIER_B2   | RO   | AEC  |
|                   | 0xB0 | 176 | DIR_IDENTIFIER_B3   | RO   | AEC  |
|                   | 0xB1 | 177 | DIR_IDENTIFIER_B4   | RO   | AEC  |
|                   | 0xB2 | 178 | VOL_IDENTIFIER_B1   | RO   | AEC  |
|                   | 0xB3 | 179 | VOL_IDENTIFIER_B2   | RO   | AEC  |
|                   | 0xB4 | 180 | VOL_IDENTIFIER_B3   | RO   | AEC  |
|                   | 0xB5 | 181 | VOL_IDENTIFIER_B4   | RO   | AEC  |
|                   | 0xB6 | 182 | EXTRACT_BYTE_IDX_B1 | RW   | ABO  |
|                   | 0xB7 | 183 | EXTRACT_BYTE_IDX_B2 | RW   | ABO  |
|                   | 0xB8 | 184 | EXTRACT_BYTE_IDX_B3 | RW   | ABO  |
|                   | 0xB9 | 185 | EXTRACT_BYTE_IDX_B4 | RW   | ABO  |
|                   | 0xBA | 186 | EXTRACT_ADR_MODE    | RW   | ABO  |
|                   | 0xBC | 188 | CONFIG_MODULE       | RW   | DEC  |
| COMMAND           | 0x10 | 16  | SOFT_RESET          | WO   | DWT  |
|                   | 0x3A | 58  | CK_CMD              | WO   | DBO  |
|                   | 0x55 | 85  | DEC_SEL             | RW   | DEC  |
|                   | 0x56 | 86  | RUN                 | RW   | DEC  |
|                   | 0x52 | 82  | CRC_IGNORE          | RW   | ABO  |
|                   | 0x53 | 83  | MUTE                | RW   | ABO  |
|                   | 0x57 | 87  | SKIP                | RW   | ABO  |
|                   | 0x58 | 88  | PAUSE               | RW   | ABO  |

| Register function     | Hex  | Dec | Name             | Type | When |
|-----------------------|------|-----|------------------|------|------|
| STATUS                | 0xCC | 204 | STATUS_MODE      | RO   | EDF  |
|                       | 0xCD | 205 | STATUS_CHAN_NB   | RO   | EDF  |
|                       | 0xCE | 206 | STATUS_SF        | RO   | EDF  |
|                       | 0x6F | 111 | STATUS_FE        | RO   | EDF  |
|                       | 0xD4 | 212 | HEADER_1         | RO   | EDF  |
|                       | 0xD5 | 213 | HEADER_2         | RO   | EDF  |
|                       | 0xD6 | 214 | HEADER_3         | RO   | EDF  |
|                       | 0xD7 | 215 | HEADER_4         | RO   | EDF  |
|                       | 0xD8 | 216 | HEADER_5         | RO   | EDF  |
|                       | 0xD9 | 217 | HEADER_6         | RO   | EDF  |
| BYPASSA_CONFIGURATION | 0x70 | 112 | CHAN_NB          | RW   | DEC  |
|                       | 0x71 | 113 | SAMPLING_FREQ    | RW   | DEC  |
|                       | 0xCB | 203 | PCMCLK_INPUT     | RW   | DEC  |
| MP3_CONFIGURATION     | 0x52 | 82  | CRC_IGNORE       | RW   | ABO  |
|                       | 0x6B | 107 | ERR_DEC_LEVEL    | RO   | EDB  |
|                       | 0x6C | 108 | ERR_DEC_NB_1     | RO   | EDB  |
|                       | 0x6D | 109 | ERR_DEC_NB_2     | RO   | EDB  |
| ADPCM_CONFIGURATION   | 0x70 | 112 | CHAN_NB          | RW   | DEC  |
|                       | 0x71 | 113 | SAMPLING_FREQ    | RW   | DEC  |
|                       | 0x72 | 114 | ENC_STATE_REPEAT | RW   | DEC  |
|                       | 0x73 | 115 | ENC_CODEC        | RW   | DEC  |
|                       | 0x74 | 116 | ENC_FRAME_LEN    | RW   | DEC  |
| MIX_CONFIGURATION     | 0x75 | 117 | MIX_MODE         | RW   | ABO  |
|                       | 0x76 | 118 | MIX_DLA          | RW   | ABO  |
|                       | 0x77 | 119 | MIX_DLB          | RW   | ABO  |
|                       | 0x78 | 120 | MIX_DRA          | RW   | ABO  |
|                       | 0x79 | 121 | MIX_DRB          | RW   | ABO  |
| TONE_CONFIGURATION    | 0x7A | 122 | TONE_ON          | RW   | ABO  |
|                       | 0x7B | 123 | TONE_FCUTH       | RW   | ABO  |
|                       | 0x7C | 124 | TONE_FCUTL       | RW   | ABO  |
|                       | 0x7D | 125 | TONE_GAINH       | RW   | ABO  |
|                       | 0x7E | 126 | TONE_GAINL       | RW   | ABO  |
|                       | 0x7F | 127 | TONE_GAIN_ATTEN  | RW   | ABO  |

### 3 REGISTER DESCRIPTION

#### 3.1 VERSION registers description

VERSION :

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |

Address : 0x00 (0)

Type : RO - DWT

Software Reset : 0x10

Hardware Reset : 0x10

Description :

The VERSION register is Read-only and it is used to identify the IC on the application board.

IDENT :

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|
| 1  | 0  | 1  | 0  | 1  | 1  | 0  | 0  |

Address : 0x01 (1)

Type : RO - DWT

Software Reset : 0xAC

Hardware Reset : 0xAC

Description :

IDENT is a read-only register and it is used to identify the IC on an application board. IDENT always has the value 0xAC.

SOFT\_VERSION :

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |

Address : 0xD3 (211)

Type : RO - DWT

Software Reset : X

Description :

The SOFT\_VERSION register is Read-only and it is used to identify the software running on the IC.

#### 3.2 PLL\_AUDIO\_CONFIGURATION registers description

PLL\_AUDIO\_PEL\_192 :

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |

Address : 0xDC (220)

Type : RW - DEC

Software Reset : 58

Description :

This register must contain a PEL value that enables the audio PLL to generate a frequency of ofact\*192 kHz for the PCMCK. See table 1, 2 & 3.

ofact is the oversampling factor needed by the DAC (ofac==246 or ofac==384).

Default value at soft reset assume :

- ofact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

PLL\_AUDIO\_PEH\_192 :

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |

Address : 0xDD (221)

Type : RW - DEC

Software Reset : 187

Description :

This register must contain a PEH value that enables the audio PLL to generate a frequency of ofact\*192 kHz for the PCMCK. See table 1, 2 & 3.

Default value at soft reset assume :

- ofact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

PLL\_AUDIO\_NDIV\_192 :

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |

Address : 0xDE (222)

Type : RW - DEC

Software Reset : 0

**Description :**

This register must contain a NDIV value that enables the audio PLL to generate a frequency of ofact\*192 kHz for the PCMCK. See table 1, 2 & 3.

Default value at soft reset assume :

- ofact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

**PLL\_AUDIO\_XDIV\_192 :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xDF (223)

Type : RW - DEC

Software Reset : 3

**Description :**

This register must contain a XDIV value that enables the audio PLL to generate a frequency of ofact\*192 kHz for the PCMCK. See table 1, 2 & 3.

Default value at soft reset assume :

- ofact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

**PLL\_AUDIO\_MDIV\_192 :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xE0 (224)

Type : RW - DEC

Software Reset : 12

**Description :**

This register must contain a MDIV value that enables the audio PLL to generate a frequency of ofact\*192 kHz for the PCMCK. See table 1, 2 & 3.

Default value at soft reset assume :

- ofact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

**PLL\_AUDIO\_PEL\_176 :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xE1 (225)

Type : RW - DEC

Software Reset : 54

**Description :**

This register must contain a PEL value that enables the audio PLL to generate a frequency of ofact\*176 kHz for the PCMCK. See table 1, 2 & 3.

Default value at soft reset assume :

- fact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

**PLL\_AUDIO\_PEH\_176 :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xE2 (226)

Type : RW - DEC

Software Reset : 118

**Description :**

This register must contain a PEH value that enables the audio PLL to generate a frequency of ofact\*176 kHz for the PCMCK. See table 1, 2 & 3.

Default value at soft reset assume :

- ofact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

**PLL\_AUDIO\_NDIV\_176 :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xE3 (227)

Type : RW - DEC

Software Reset : 0

**Description :**

This register must contain a NDIV value that enables the audio PLL to generate a frequency of ofact\*176 kHz for the PCMCK. See table 1, 2 & 3.

Default value at soft reset assume :

- ofact == 256
- external crystal provide a CRYCK running at 14.31818 MHz



**PLL\_AUDIO\_XDIV\_176 :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xE4 (228)

Type : RW - DEC

Software Reset : 2

**Description :**

This register must contain a XDIV value that enables the audio PLL to generate a frequency of ofact\*176 kHz for the PCMCK. See table 1, 2 & 3.

Default value at soft reset assume :

- ofact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

**PLL\_AUDIO\_MDIV\_176 :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xE5 (229)

Type : RW - DEC

Software Reset : 8

**Description :**

This register must contain a MDIV value that enables the audio PLL to generate a frequency of ofact\*176 kHz for the PCMCK. See table 1, 2 & 3.

Default value at soft reset assume :

- ofact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

**PLL\_SYSTEM\_CONFIGURATION registers description**

**PLL\_SYSTEM\_PEL\_50 :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xE6 (230)

Type : RW - DEC

Software Reset : 0

**Description :**

This register must contain a PEL value that enables the system PLL to generate a frequency of 50 MHz for the SYSCK. See table 4.

Default value at soft reset assume :

- external crystal provide a CRYCK running at 14.31818 MHz

**PLL\_SYSTEM\_PEH\_50 :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xE7 (231)

Type : RW - DEC

Software Reset : 0

**Description :**

This register must contain a PEH value that enables the system PLL to generate a frequency of 50 MHz for the SYSCK. See table 4.

Default value at soft reset assume :

- external crystal provide a CRYCK running at 14.31818 MHz

**PLL\_SYSTEM\_NDIV\_50 :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xE8 (232)

Type : RW - DEC

Software Reset : 0

**Description :**

This register must contain a NDIV value that enables the system PLL to generate a frequency of 50 MHz for the SYSCK. See table 4.

Default value at soft reset assume :

- external crystal provide a CRYCK running at 14.31818 MHz

**PLL\_SYSTEM\_XDIV\_50 :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xE9 (233)

Type : RW - DEC

Software Reset : 1

**Description :**

This register must contain a XDIV value that enables the system PLL to generate a frequency of 50 MHz for the SYSCK. See table 4.

Default value at soft reset assume :

- external crystal provide a CRYCK running at 14.31818 MHz

**PLL\_SYSTEM\_MDIV\_50 :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xEA (234)

Type : RW - DEC

Software Reset : 13

**Description :**

This register must contain a MDIV value that enables the system PLL to generate a frequency of 50 MHz for the SYSCK. See table 4.

Default value at soft reset assume :

- external crystal provide a CRYCK running at 14.31818 MHz

**PLL\_SYSTEM\_PEL\_42\_5 :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xE6 (230)

Type : RW - DEC

Software Reset : 126

**Description :**

This register must contain a PEL value that enables the system PLL to generate a frequency of 42.5 MHz for the SYSCK. See table 4.

Default value at soft reset assume :

- external crystal provide a CRYCK running at 14.31818 MHz

**PLL\_SYSTEM\_PEH\_42\_5 :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xE7 (231)

Type : RW - DEC

Software Reset : 223

**Description :**

This register must contain a PEH value that enables the system PLL to generate a frequency of 42.5 MHz for the SYSCK. See table 4.

Default value at soft reset assume :

- external crystal provide a CRYCK running at 14.31818 MHz

**PLL\_SYSTEM\_NDIV\_42\_5 :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xE8 (232)

Type : RW - DEC

Software Reset : 0

**Description :**

This register must contain a NDIV value that enables the system PLL to generate a frequency of 42.5 MHz for the SYSCK. See table 4.

Default value at soft reset assume :

- external crystal provide a CRYCK running at 14.31818 MHz

**PLL\_SYSTEM\_XDIV\_42\_5 :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xE9 (233)

Type : RW - DEC

Software Reset : 1

**Description :**

This register must contain a XDIV value that enables the system PLL to generate a frequency of 42.5 MHz for the SYSCK. See table 4.

Default value at soft reset assume :

- external crystal provide a CRYCK running at 14.31818 MHz

**PLL\_SYSTEM\_MDIV\_42\_5 :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xEA (234)

Type : RW - DEC

Software Reset : 10

Description :

This register must contain a MDIV value that enables the system PLL to generate a frequency of 42.5 MHz for the SYSCK. See table 4.

Default value at soft reset assume :

- external crystal provide a CRYCK running at 14.31818 MHz

### 3.3 I2Sout\_CONFIGURATION registers description

**OUTPUT\_CONF :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x66 (102)

Type : RW - DEC

Software Reset : 0

Description :

If set to 1 enable the configurability of the PCM-BLOCK Output thanks to following registers, else disable this configurability and take embedded default configuration for PCM-BLOCK registers.

Note that this embedded default configuration can be retrieved by user thanks to following setting :

- PCM\_DIV = 3;
- PCM\_CONF = 0;
- PCM\_CROSS = 0;

**PCM\_DIV :**

|    |    |     |     |     |     |     |     |
|----|----|-----|-----|-----|-----|-----|-----|
| b7 | b6 | b5  | b4  | b3  | b2  | b1  | b0  |
| 0  | 0  | DV5 | DV4 | DV3 | DV2 | DV1 | DV0 |

Address : 0x67 (103)

Type : RW - DEC

Software Reset : 0

Description :

If OUTPUT\_CONF == 1, configure the divider to generate the bit clock of the I2Sout interface, called BCKO, from PCMCK. according the following relation :  $BCKO = PCMCK / 2 * (PCM\_DIV + 1)$

**PCM\_CONF :**

|    |     |     |     |     |     |     |     |
|----|-----|-----|-----|-----|-----|-----|-----|
| b7 | b6  | b5  | b4  | b3  | b2  | b1  | b0  |
| 0  | CO6 | CO5 | CO4 | CO3 | CO2 | CO1 | CO0 |

Address : 0x68 (104)

Type : RW - DEC

Software Reset : 0

Description :

If OUTPUT\_CONF == 1, configure the I2Sout interface according following table.

| Bit fields | Comment  |
|------------|--|
| CO[1:0]    | 0 : 16 bits mode (16 slots transmitted).<br>1 : 18 bits mode (18 slots transmitted).<br>2 : 20 bits mode (20 slots transmitted).<br>3 : 24 bits mode (24 slots transmitted). |
| CO2        | Polarity of BCKO :<br>0 : data are sent on the falling edge & stable on the rising).<br>1 : (data are sent on the rising edge & stable on the falling).                      |
| CO3        | 0 : I2S format is selected<br>1 : other format is selected   |
| CO4        | Polarity of LRCKO :<br>0 : low->right, high->left).<br>1 : low->left, high->right so compliant to I2S format ).  |
| CO5        | 0 : data are in the last BCKO cycles of LRCKO (right aligned data).<br>1 : data are in the first BCKO cycles of LRCKO (left aligned data).                                   |
| CO6        | 0 : the transmission is LS bit first.<br>1 : the transmission is MS bit first.   |

**PCM\_CROSS :**

|    |    |    |    |    |    |     |     |
|----|----|----|----|----|----|-----|-----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1  | b0  |
| 0  | 0  | 0  | 0  | 0  | 0  | CR1 | CR0 |

Address : 0x69 (105)

Type : RW - DEC

Software Reset : 0

Description :

If OUTPUT\_CONF == 1, CR[1:0] is used to configure the output crossbar according following table.

| CR1 | CR0 | Comment  |
|-----|-----|--|
| 0   | 0   | Left channel is mapped on the left output.<br>Right channel is mapped on the right output. |
| 0   | 1   | Left channel is duplicated on both output channels.  |
| 1   | 0   | Right channel is duplicated on both output channels.                                       |
| 1   | 1   | Right and left channels are toggled.   |

### 3.4 GPSO\_CONFIGURATION registers description

OUTPUT\_CONF :

| b7 | b6 | b5 | b4 | b3 | b2  | b1  | b0  |
|----|----|----|----|----|-----|-----|-----|
| X  | X  | X  | X  | X  | OC2 | OC1 | OC0 |

Address : 0x66 (102)

Type : RW - DEC

Software Reset : 0

Description :

| Bit fields | Comment   |
|------------|---|
| OC0        | Configuration of gpso :<br>0 : take embedded default configuration.<br>1 : configure gpso from register GPSO_CONF.                    |
| OC1        | Use of block PCM to generate clocks (PCMCK, LRCK & BCK):<br>0 : no use.<br>1 : use it.  |
| OC2        | Configuration of PCM block:<br>0 : take embedded default configuration.<br>1 : configure PCM block from PCM_DIV & PCM_CONF registers. |

Note that embedded default configuration for GPSO can be retrieved by user thanks to following setting :

- GPSO\_CONF = b00000011;

Note that embedded default configuration for PCM block is described at previous chapter.

GPSO\_CONF :

| b7  | b6  | b5  | b4  | b3  | b2  | b1  | b0  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| CF7 | CF6 | CF5 | CF4 | CF3 | CF2 | CF1 | CF0 |

Address : 0x6A (106)

Type : RW - DEC

Software Reset : 0

Description :

If OUTPUT\_CONF == 1, this register configure the GPSO interface.

| Bit fields | Comment   |
|------------|---|
| CF0        | Polarity of GPSO_CK :<br>0 : data provided on rising edge & stable on falling edge<br>1 : data provided on falling edge & stable on rising edge |
| CF1        | Polarity of GPSO_REQ :<br>0 : data are valid when GPSO_REQ is high<br>1 : data are valid when GPSO_REQ is low                                   |
| CF[7:2]    | Reserved : to be set to 0.  |

### 3.5 I2Sin\_CONFIGURATION registers description

INPUT\_CONF :

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|

Address : 0x5A (90)

Type : RW - DEC

Software Reset : 0

Description :

If set to 1 enable the configurability of the I2Sin Input thanks to following registers, else disable this configurability and take embedded default configuration for I2Sin registers.

Note that this embedded default configuration can be retrieved by user thanks to following setting :

- I\_AUDIO\_CONFIG\_1 = b00000110;
- I\_AUDIO\_CONFIG\_2 = b11100000;
- I\_AUDIO\_CONFIG\_3 = b00000001;

**I\_AUDIO\_CONFIG\_1:**

|           |           |           |           |           |           |           |           |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| <b>b7</b> | <b>b6</b> | <b>b5</b> | <b>b4</b> | <b>b3</b> | <b>b2</b> | <b>b1</b> | <b>b0</b> |
| CF7       | CF6       | CF5       | CF4       | CF3       | CF2       | CF1       | CF0       |

Address : 0x5B (91)

Type : RW - DEC

Software Reset : 0

Description :

If INPUT\_CONF == 1, this register configure the I2Sin interface.

| Bit fields | Comment  |
|------------|--|
| CF0        | Relative synchro :<br>0 : synchro with first data bit<br>1 : synchro one bit before first data bit   |
| CF1        | Data reception configuration :<br>0 : LSB first<br>1 : MSB first   |
| CF2        | Polarity of bit clock BCK :<br>0 : data provided on falling edge & stable on rising edge.<br>1 : data provided on rising edge & stable on falling edge |
| CF3        | Polarity of LR clock LRCK :<br>0 : negative<br>1 : positive  |
| CF4        | Start value of LRCK : combined with CF3, this bit enable user to determine left/right couple according to the following table.                         |
| CF[7:5]    | Reserved : to be set to 0.   |

| CF3 | CF4 | Left/Right couples               |
|-----|-----|----------------------------------|
| 0   | 0   | (data1/data2), (data3/data4),... |
| 1   | 0   | (data0/data1), (data2/data3),... |
| 0   | 1   | (data0/data1), (data2/data3),... |
| 1   | 1   | (data1/data2), (data3/data4),... |

**I\_AUDIO\_CONFIG\_2:**

|           |           |           |           |           |           |           |           |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| <b>b7</b> | <b>b6</b> | <b>b5</b> | <b>b4</b> | <b>b3</b> | <b>b2</b> | <b>b1</b> | <b>b0</b> |
| LR7       | LR6       | LR5       | LR4       | LR3       | LR2       | LR1       | LR0       |

Address : 0x5C (92)

Type : RW - DEC

Software Reset : 0

Description :

See I\_AUDIO\_CONFIG\_3 register description..

**I\_AUDIO\_CONFIG\_3 :**

|           |           |           |           |           |           |           |           |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| <b>b7</b> | <b>b6</b> | <b>b5</b> | <b>b4</b> | <b>b3</b> | <b>b2</b> | <b>b1</b> | <b>b0</b> |
| 0         | 0         | 0         | 0         | 0         | 0         | LR9       | LR8       |

Address : 0x5D (93)

Type : RW - DEC

Software Reset : 0

Description :

If INPUT\_CONF == 1, this register is used to configure the phase of the LRCK of the I2Sin.

| Bit fields | Comment  |
|------------|--|
| LR[4:0]    | Position of the data within the LRCK phase :<br>- if CF1 = 0 (LSB), value must be set to [31 - SL[9:5] - bit position of the first bit of data within the LRCK phase].<br>- if CF1 = 1 (MSB), value must be set to bit position of the first bit of data within the LRCK phase.<br>Note that range of value for this bit position is [0:31]. |
| LR[9:5]    | Length-1 of the data.<br>Max value is 31.  |
| LR[15:10]  | Reserved : to be set to 0  |

**3.6 CDBSA\_CONFIGURATION registers description**

**INPUT\_CONF :**

|           |           |           |           |           |           |           |           |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| <b>b7</b> | <b>b6</b> | <b>b5</b> | <b>b4</b> | <b>b3</b> | <b>b2</b> | <b>b1</b> | <b>b0</b> |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|

Address : 0x5A (90)

Type : RW - DEC

Software Reset : 0

## STA016T

Description :

If set to 1 enable the configurability of the CD & BS input interfaces in audio mode thanks to following registers, else disable this configurability and take embedded default configuration.

Note that this embedded default configuration can be retrieved by user thanks to following setting :

- I\_AUDIO\_CONFIG1 = b00010010;  
// clocks in input  
// & polarity negative
- I\_AUDIO\_CONFIG2 = b00110010;  
// synchro with first data bit  
// data unsigned, MSB first
- I\_AUDIO\_CONFIG3 = b11001111;  
// LRCK phase length is 1
- I\_AUDIO\_CONFIG4 = b00000011;  
// LRCK phase length is 16
- I\_AUDIO\_CONFIG5 = 0xFF;  
// received 16 bits
- I\_AUDIO\_CONFIG6 = 0xFF;  
// received 16 bits
- I\_AUDIO\_CONFIG7 = 0x00;  
// received 16 bits
- I\_AUDIO\_CONFIG8 = 0x00;  
// received 16 bits
- I\_AUDIO\_CONFIG9 = 16;  
// data size is 16
- I\_AUDIO\_CONFIG10 = 0x00;  
// no use because clock in input
- I\_AUDIO\_CONFIG11 = 0x00;  
// no use because clock in input

### I\_AUDIO\_CONFIG\_1 :

| b7  | b6  | b5  | b4  | b3  | b2  | b1  | b0  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| CF7 | CF6 | CF5 | CF4 | CF3 | CF2 | CF1 | CF0 |

Address : 0x5B (91)

Type : RW - DEC

Software Reset : 0

Description :

If INPUT\_CONF == 1, this register is used to configure CD & BS input interfaces in audio mode.

| Bit | Comment  |
|-----|--|
| CF0 | Reserved : to be set to 0  |
| CF1 | Reserved : to be set to 1  |
| CF2 | Direction of bit clocks CD_BCK & BS_BCK:<br>0 : input<br>1 : output  |
| CF3 | Polarity of bit clocks CD_BCK & BS_BCK :<br>0 : data provided on falling edge & stable on rising edge<br>1 : data provided on rising edge & stable on falling edge     |
| CF4 | Reserved : to be set to 1  |
| CF5 | Direction of LR clocks CD_LRCK & BS_LRCK :<br>0 : input<br>1 : output  |
| CF6 | Polarity of LR clocks CD_LRCK & BS_LRCK :<br>0 : left sample corresponds to the low level phase of LRCK<br>1 : left sample corresponds to the high level phase of LRCK |
| CF7 | Reserved : to be set to 0  |

### I\_AUDIO\_CONFIG\_2 :

| b7   | b6   | b5   | b4   | b3   | b2   | b1  | b0  |
|------|------|------|------|------|------|-----|-----|
| CF15 | CF14 | CF13 | CF12 | CF11 | CF10 | CF9 | CF8 |

Address : 0x5C (92)

Type : RW - DEC

Software Reset : 0

Description :

If INPUT\_CONF == 1, this register is used to configure CD & BS input interfaces in audio mode.

| Bit  | Comment  |
|------|--|
| CF8  | Relative synchro :<br>0 : synchro with first data bit<br>1 : synchro one bit before first data bit |
| CF9  | Data reception configuration :<br>0 : LSB first<br>1 : MSB first                                   |
| CF10 | Arithmetic type of the reception :<br>0 : unsigned data<br>1 : signed data                         |

| Bit  | Comment  |
|------|--|
| CF11 | Bit to select the reference clock used to generate BCK if clocks are in output (CF2=1 & CF5=1). Otherwise this bit is useless.<br>0 : SYSCK<br>1 : PCMCK |
| CF12 | Reserved : to be set to 1  |
| CF13 | Reserved : to be set to 1  |
| CF14 | Reserved : to be set to 0  |
| CF15 | Reserved : to be set to 0  |

**I\_AUDIO\_CONFIG\_3 :**

| b7  | b6  | b5  | b4  | b3  | b2  | b1  | b0  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| LR7 | LR6 | LR5 | LR4 | LR3 | LR2 | LR1 | LR0 |

Address : 0x5D (93)

Type : RW - DEC

Software Reset : 0

Description :

See I\_AUDIO\_CONFIG\_4 register description..

**I\_AUDIO\_CONFIG\_4 :**

| b7   | b6   | b5   | b4   | b3   | b2   | b1  | b0  |
|------|------|------|------|------|------|-----|-----|
| LR15 | LR14 | LR13 | LR12 | LR11 | LR10 | LR9 | LR8 |

Address : 0x5E (94)

Type : RW - DEC

Software Reset : 0

Description :

If INPUT\_CONF == 1, this register is used to configure LR clocks (CD\_LRCK & BS\_LRCK) of CD & BS input interfaces in audio mode.

| Bit fields | Comment   |
|------------|---|
| LR[5:0]    | Length-1 of phase 1 of LR clocks CD_LRCK & BS_LRCK.<br>Max value is 31. |

| Bit fields | Comment   |
|------------|---|
| LR[11:6]   | Length-1 of phase 2 of LR clocks CD_LRCK & BS_LRCK.<br>Max value is 31. |
| LR[15:12]  | Reserved : to be set to 0   |

**I\_AUDIO\_CONFIG\_5:**

| b7  | b6  | b5  | b4  | b3  | b2  | b1  | b0  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| MA7 | MA6 | MA5 | MA4 | MA3 | MA2 | MA1 | MA0 |

Address : 0x5F (95)

Type : RW - DEC

Software Reset : 0

Description :

See I\_AUDIO\_CONFIG\_8 register description.

**I\_AUDIO\_CONFIG\_6 :**

| b7   | b6   | b5   | b4   | b3   | b2   | b1  | b0  |
|------|------|------|------|------|------|-----|-----|
| MA15 | MA14 | MA13 | MA12 | MA11 | MA10 | MA9 | MA8 |

Address : 0x60 (96)

Type : RW - DEC

Software Reset : 0

Description :

See I\_AUDIO\_CONFIG\_8 register description..

**I\_AUDIO\_CONFIG\_7 :**

| b7   | b6   | b5   | b4   | b3   | b2   | b1   | b0   |
|------|------|------|------|------|------|------|------|
| MA23 | MA22 | MA21 | MA20 | MA19 | MA18 | MA17 | MA16 |

Address : 0x61 (97)

Type : RW - DEC

Software Reset : 0

Description :

See I\_AUDIO\_CONFIG\_8 register description..

**I\_AUDIO\_CONFIG\_8 :**

| b7   | b6   | b5   | b4   | b3   | b2   | b1   | b0   |
|------|------|------|------|------|------|------|------|
| MA31 | MA30 | MA29 | MA28 | MA27 | MA26 | MA25 | MA24 |

Address : 0x62 (98)  
 Type : RW - DEC  
 Software Reset : 0

Description :

If INPUT\_CONF == 1, those registers are used to configure the MASK to be applied to CD\_LRCK & BS\_LRCK phase 1 & 2.

- if MA<sub>i</sub> set to 0, then bit i of both phases is not received.
- if MA<sub>i</sub> set to 1, then bit i of both phases is received.

**I\_AUDIO\_CONFIG\_9 :**

| b7  | b6  | b5  | b4  | b3  | b2  | b1  | b0  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| DL7 | DL6 | DL5 | DL4 | DL3 | DL2 | DL1 | DL0 |

Address : 0x63 (99)  
 Type : RW - DEC  
 Software Reset : 0

Description :

If INPUT\_CONF == 1, this register is used to configure the size of the data to be received by CD & BS input interfaces in audio mode. Max is 32.

**I\_AUDIO\_CONFIG\_10 :**

| b7  | b6  | b5  | b4  | b3  | b2  | b1  | b0  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| DV7 | DV6 | DV5 | DV4 | DV3 | DV2 | DV1 | DV0 |

Address : 0x64 (100)  
 Type : RW - DEC  
 Software Reset : 0

Description :

See I\_AUDIO\_CONFIG\_11 register description.

**II\_AUDIO\_CONFIG\_11 :**

| b7   | b6   | b5   | b4   | b3   | b2   | b1  | b0  |
|------|------|------|------|------|------|-----|-----|
| DV15 | DV14 | DV13 | DV12 | DV11 | DV10 | DV9 | DV8 |

Address : 0x65 (101)  
 Type : RW - DEC  
 Software Reset : 0

Description :

If INPUT\_CONF == 1, those registers are used to create BCK if configured in output (so if CF2=1 & CF5=1): then value of DV[15:0] is the divider factor to be applied to the selected clock (CF11 select either SYSCLK or PCMCLK) to create BCK.

Note : value 0 & 1 correspond to a bypass of the dividers.

**3.7 BSB\_CONFIGURATION registers description**

**POL\_REQ :**

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|

Address : 0x59 (89)  
 Type : WO - DEC  
 Software Reset : 0

Description :

This register manage the polarity of the data REQ signal DREQ of the BS input interface.

If set to 0, data are requested when REQ = 0.

If set to 1, data are requested when REQ = 1.

**INPUT\_CONF :**

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|

Address : 0x5A (90)  
 Type : RW - DEC  
 Software Reset : 0

Description :



If set to 1 enable the configurability of the BSB input interfaces in burst mode thanks to following register, else disable this configurability and take embedded default configuration.

Note that this embedded default configuration can be retrieved by user thanks to following setting :

- I\_AUDIO\_CONFIG1 = b00000000;// polarity choice

**I\_AUDIO\_CONFIG\_1 :**

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0  |
|----|----|----|----|----|----|----|-----|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | CF0 |

Address : 0x5B (91)

Type : RW - DEC

Software Reset : 0

Description :

If INPUT\_CONF == 1, this register is used to configure BSB bit clock.

| Bit | Comment  |
|-----|--|
| CF0 | Polarity of bit clock BS_BCK :<br>0 : data provided on falling edge & stable on rising edge.<br>1 : data provided on rising edge & stable on falling edge. |

**3.8 CD\_CONFIGURATION registers description**

**BASIC\_COMMAND :**

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|

Address : 0x40 (64)

Type : RW - AEC

Software Reset : 0

Description :

Used for giving to dsp basic cd-player commands.

| Value | Command            |
|-------|--------------------|
| 1     | stop playing music |
| 2     | pause              |

| Value | Command                               |
|-------|---------------------------------------|
| 3     | fast forward                          |
| 4     | fast rewind                           |
| 5     | track up                              |
| 6     | track down                            |
| 9     | directory down                        |
| 10    | directory up                          |
| 11    | play specified track                  |
| 12    | set a play-list index                 |
| 13    | edit play list                        |
| 14    | play current dir                      |
| 15    | play cd from beginning                |
| 112   | start playing music                   |
| 113   | start searching bytes/mute navigation |
| 124   | ID3 name of song required             |
| 125   | ID3 name of author required           |
| 126   | ID3 name of album required            |
| 127   | name of file required                 |
| 128   | name of directory required            |

**FAST\_FUNCTIONAL\_VAL :**

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|

Address : 0x41 (65)

Type : RW - ABO

Software Reset : 0

Description :

This register specifies the volume of fast function. For the "fast forward function" it is a number between 1 and 20.

For the "fast rewind function" it is a number of second

**REQUIRED\_TRACK :**

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|

Address : 0x42 (66)

Type : RW - ABO

Software Reset : 0

## STA016T

Description :

This specifies the number of track to play.

### REQUIRED\_DIR :

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x43 (67)

Type : RW - ABO

Software Reset : 0

Description :

This register specifies the number of directory to play.

### PLAY\_MODE :

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x44 (68)

Type : RW - ABO

Software Reset : 0

Description :

This register specifies the playing mode.

| Bit   | Mode   |
|-------|--|
| [1:0] | end of directory:<br>0: play next directory<br>1: replay same directory<br>2: make pause.<br>other: reserved |
| [3:2] | end of track:<br>0: play next track.<br>1: replay same track.<br>2: make pause.<br>other: reserved           |
| 4     | next track choice:<br>0: linear mode.<br>1: random mode.   |
| 5     | playing time for track:<br>0: until end of track.<br>1: scanning mode.                                       |
| 6     | end of CD:<br>0: stop.<br>1: replay same CD..  |

### TYPE\_CD\_EXT\_REQ:

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x46 (70)

Type : RO - AEC

Software Reset : 0

Description :

This register specifies the type of request sent to the cd module.

| Value | Signification                            |
|-------|--|
| 10    | application is in pause after EOT or EOD |
| 18    | request for a sector                     |
| 20    | begin of track reached                   |
| 30    | ready to receive a new command           |
| 35    | dsp ready to run                         |
| 40    | cd application stopped.                  |
| 66    | time spent on track available            |
| 112   | request for root                         |
| 120   | song information available               |

### MINUTE\_REQ :

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x47 (71)

Type : RO - AEC

Software Reset : 0

Description :

This register specifies to the CD module the minute location requested.

### SECOND\_REQ :

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x48 (72)

Type : RO - AEC

Software Reset : 0

Description :

This register specifies to the CD module the second location requested.

**SECTOR\_REQ :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x49 (73)

Type : RO - AEC

Software Reset : 0

Description :

This register specifies to the CD module the sector location requested.

**MINUTE\_SPENT :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x4A (74)

Type : RO - AEC

Software Reset : 0

Description :

This register specifies the number of minute spent from the beginning of the track. It is reset at the beginning of a new track.

**SECOND\_SPENT :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x4B (75)

Type : RO - AEC

Software Reset : 0

Description :

This register specifies the number of second spent from the beginning of the track. It is reset at the beginning of a new track.

**SCANNING\_TIME :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x4C (76)

Type : RW - ABO

Software Reset : 0

Description :

This register specifies in second (<60) the playing time for each track in scanning mode.

**PLAY\_LIST\_INDEX:**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x4D (77)

Type : RW - ABO

Software Reset : 0

Description :

This register specifies the index in the play list of the song to enter in the play list, it is also a value between 1 and the maximum number of track in the directory.

**PLAY\_LIST\_VALUE:**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x4E (78)

Type : RW - ABO

Software Reset : 0

Description :

This register specifies the song index in the directory to enter in the play list, it is also a value between 1 and the maximum number of track in the directory.

**CD\_SONG\_INFO\_Cn :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x86 (134) to 0xA5 (165)

Type : RO - AEC

Software Reset : 0

## STA016T

### Description :

This register contains the n<sup>th</sup> character of the song info required (ASCII code).

### CD\_SONG\_TYPE\_INFO :

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xA6 (166)

Type : RO - AEC

Software Reset : 0

### Description :

This register specifies the kind of current information contained in the

| Value | Signification               |
|-------|-----------------------------|
| 0     | information not valid       |
| 1     | ID3 song name information   |
| 2     | ID3 author name information |
| 3     | ID3 album name information  |
| 4     | file name information       |
| 5     | directory name information  |
| 6     | bytes requested             |
| 7     | play list content           |

When the track has changed the previous information are declared "not valid". New valid information should be requested by user.

### NB\_OF\_CUR\_TRACK :

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xA7 (167)

Type : RO - AEC

Software Reset : 0

### Description :

This register specifies the number of the current track into his directory (sub-directories included): from 1 to max number of track/subdirectory.

### NB\_OF\_CUR\_DIR :

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xA8 (168)

Type : RO - AEC

Software Reset : 0

### Description :

This register specifies the number of the current directory into the CD: from 1 to max number of directory. This number is negative if going backward to the end of the CD with the command directory-down.

### CD\_CUR\_STATUS :

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xA9 (169)

Type : RO - ABO

Software Reset : 0

### Description :

This register gives the status of the CD application.

| Bit | Mode   |
|-----|--|
| 0   | 0: unknown format.<br>1: recognized format                     |
| 1   | reserved.  |
| 2   | 0: searching track.<br>1: track founded.                       |
| 3   | 0: ID3 present.<br>1: ID3 missing.                             |
| 4   | 0: no error detected.<br>1: error detected.                    |
| 5   | 0: CD application in pause.<br>1: CD application not in pause. |
| 6   | 0: CD not playable.<br>1: CD playable.                         |
| 7   | 0: music mode.<br>1: searching bytes mode                      |

**CD\_TRACK\_FORMAT :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xAA (170)

Type : RO - AEC

Software Reset : 0

Description :

This register specifies the format of the played track considering the extension name. Only 1 bit can be set in the same time:

| Bit | FORMAT                 |
|-----|------------------------|
| 0   | 0 : UNKNOWN<br>1 : MP3 |
| 1   | 1: RESERVED            |
| 2   | MPEG1                  |
| 3   | MPEG2                  |
| 4   | MPG                    |

**NB\_OF\_SUBDIR :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xAB (171)

Type : RO - AEC

Software Reset : 0

Description :

This register specifies the number of sub-directory in the current directory.

**NB\_OF\_SUB\_TRACK :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xAC (172)

Type : RO - AEC

Software Reset : 0

Description :

This register specifies the number of file in the current directory.

**DIRECTORY\_LEVEL :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xAD (173)

Type : RO - AEC

Software Reset : 0

Description :

This register specifies the current directory level.

**DIR\_IDENTIFIER\_Bn :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xAE (174) to 0xB1 (177)

Type : RO - AEC

Software Reset : 0

Description :

This register specifies the nth byte of the number of byte of the current directory. Considering that two directories have very few chance to have exactly the same number of byte, this number allows to identify the directory. The first byte (174) is the MSB and the last one (177) is the LSB.

**VOL\_IDENTIFIER\_Bn:**

Address : 0xB2 (178) to 0xB5 (181)

Type : RO - AEC

Software Reset : 0

Description :

This register specifies the nth byte of the number of byte of the CD. Considering that two CD have very few chance to have exactly the same number of byte, this number allows to identify the CD. The first byte (178) is the MSB and the last one (181) is the LSB.

## STA016T

### EXTRACT\_BYTE\_IDX\_Bn:

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xB6 (182) to 0xB8 (185)

Type : RW - ABO

Software Reset : 0

Description :

This register specifies the  $n^{\text{th}}$  byte of the index of the byte block to extract from the CD. This number should be relative to the beginning of the track containing these bytes.

### EXTRACT\_ADR\_MODE :

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xBA (186)

Type : RW - ABO

Software Reset : 0

Description :

This register specifies addressing mode type for byte extraction: if set to 0, it is a relative (to the beginning of the current file) addressing mode, if set to 1 it is an absolute addressing mode (relative to the beginning of the CD).

### CD\_CONFIG\_MODULE :

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xBC (188)

Type : RO - ABO

Software Reset : 0xA

Description :

This register set some parameters describing the way the module transmit the data to the DSP.

| Bit | FORMAT   |
|-----|--|
| 0   | 0: valid data byte swapped.<br>1: valid data not byte swapped. |

| Bit   | FORMAT                                       |
|-------|--|
| 1     | 0: ID3 tag not checked<br>1: ID3 tag checked |
| other | reference for counting sector in minute.     |

## 3.9 COMMAND registers description

### SOFT\_RESET :

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x10 (16)

Type : WO - DWT

Software Reset : 0

Description :

When user write 1 in this register, a soft reset occurs. The core command register and the interrupt register are cleared. The decoder goes into idle mode.

### CK\_CMD :

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x3A (58)

Type : WO - DBO

Software Reset : 1

Hardware Reset : 1

Description :

After a soft reset, user must write 0 in CK\_CMD to run the core clock of the chip. This will begin the boot of the chip, and so get it out of its idle state.

### DEC\_SEL :

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x55 (85)

Type : RW - DEC

Software Reset : 0

**Description :**

This register select the decoding data flux according the mode written in following table.

| Bit(7:0) | Mode                        |
|----------|-----------------------------|
| 0        | CD_MP3                      |
| 1        | CD_BYPASSA                  |
| 2        | RESERVED                    |
| 3        | BSB_MP3                     |
| 4        | BSB_ADPCM_DECODER           |
| 5        | RESERVED                    |
| 6        | BSA_ADPCM_ENCODER           |
| 7        | BSA_BYPASSA                 |
| 8        | I2Sin_ADPCM_ENC             |
| 9        | I2Sin_BYPASSA               |
| 10       | SINE (test mode chip alive) |

**RUN :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x56 (86)

Type : RW - DEC

Software Reset : 0

**Description :**

- When a software reset occurs, register RUN is reset (value 0) by the dsp (see I).
- When boot routines are finished, the dsp write inside RUN register the value 2 : this is the start of the external configuration period (start of DEC : see I).
- When the external device wants to end the external configuration period, it must write the value 1 inside the register RUN: this is the run command that starts the decoding process (see I).

**CRC\_IGNORE :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x52 (82)

Type : RW - ABO

Software Reset : 0

**Description :**

For decoders having CRC abilities (see each decoder configuration), if set to 0 enable the check of CRC, if set to 1 disable the check of the CRC.

**MUTE :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x53 (83)

Type : RW - ABO

Software Reset : 0

**Description :**

For decoders having MUTE abilities (see each decoder configuration), if set to 0 disable the mute of the decoder, if set to 1 enable the mute of the decoder. Note that during a MUTE the input stream keeps on entering.

**SKIP :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x57 (87)

Type : RW - ABO

Software Reset : 0

**Description :**

For data flux using USSB Input, if SKIP == n>2, decoder skip (n-1) out of n frames. Note that maximum value for n is 8, and if n==0 or n==1, no frames is skipped.

**PAUSE :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x58 (88)

Type : RW - ABO

Software Reset : 0

Description :

For decoders having PAUSE abilities (see each decoder configuration), if set to 0 disable the pause of the decoder, if set to 1 enable the pause of the decoder. Note that during a PAUSE the input stream is stopped.

3.10 STATUS registers description

STATUS\_MODE :

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xCC (204)

Type : RO - EDF

Software Reset : 0

Description :

This register give the type of the currently decoded bitstream according following table.

| Value | Mode     |
|-------|----------|
| 0     | MP3      |
| 1     | MP3_25   |
| 2     | RESERVED |
| 3     | RESERVED |
| 4     | RESERVED |
| 5     | ADPCM    |
| 6     | RESERVED |
| 7     | BYPASS   |
| 8     | RESERVED |
| 9     | RESERVED |
| 10    | RESERVED |
| 11    | MPG2     |
| 12    | RESERVED |
| 13    | RESERVED |
| 14    | RESERVED |
| 15    | RESERVED |
| 16    | RESERVED |
| 17    | RESERVED |
| 18    | UNKNOWN  |

STATUS\_CHANS\_NB :

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xCD (205)

Type : RO - EDF

Software Reset : 0

Description :

This register gives the number of channel currently decoded.

STATUS\_SF :

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xCE (206)

Type : RO - EDF

Software Reset : 0

Description :

This register gives the index of the sampling frequency of the stream currently decoded. Note that sampling frequency indexes are given by table 5

STATUS\_FE :

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x6F (111)

Type : RO - AEC

Software Reset : 0

Description :

This register give the status of the synchronization process according following table.

| Value | Level                 |
|-------|-----------------------|
| 0     | Syncrho not started   |
| 1     | Syncword found        |
| 2     | Syncword search       |
| 3     | Syncword hard to find |



**HEADER\_n:**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xD4 (212) to 0xD9 (217)

Type : RO - EDF

Software Reset : 0

Description :

This register give the nth byte of the header of the frame currently decoded

**3.11 BYPASSA\_CONFIGURATION registers description**

**CHAN\_NB :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x70 (112)

Type : RW - DEC

Software Reset : 0

Description :

User must specify the number of channel for bypassa decoder to decode.

**SAMPLING\_FREQ: :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x71 (113)

Type : RW - DEC

Software Reset : 0

Description :

User must specify the sampling frequency of the stream to decode if clocks direction of the input interface is input. Sampling frequency index is given by table 4.

**PCMCLK\_INPUT :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0xCB (203)

Type : RW - DEC

Software Reset : 0

Description :

If set to 1, the PCMCLK pad is configure as input in order to receive an external reference clock.

**3.12 MP3\_CONFIGURATION registers description**

**ERR\_DEC\_LEVEL :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x6B (107)

Type : RO - EDF

Software Reset : 0

Description :

This register give the status of the mp3 decoding process according the error level written in following table.

| Value | Level                      |
|-------|----------------------------|
| 0     | No error                   |
| 1     | Warning while decoding     |
| 2     | Error while decoding       |
| 3     | Fatal error while decoding |

**ERR\_DEC\_NB\_1 :**

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| b7  | b6  | b5  | b4  | b3  | b2  | b1  | b0  |
| ER7 | ER6 | ER5 | ER4 | ER3 | ER2 | ER1 | ER0 |

Address : 0x6C (108)

Type : RO - EDF

Software Reset : 0

Description :

See ERR\_DEC\_NB\_2 register description.

**ERR\_DEC\_NB\_2 :**

|           |           |           |           |           |           |           |           |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| <b>b7</b> | <b>b6</b> | <b>b5</b> | <b>b4</b> | <b>b3</b> | <b>b2</b> | <b>b1</b> | <b>b0</b> |
| ER15      | ER14      | ER13      | ER12      | ER11      | ER10      | ER9       | ER8       |

Address : 0x6D (109)  
 Type : RO - EDF  
 Software Reset : 0

Description :  
 This register give the status of the mp3 decoding process according the error number written in following table.

| Event     | Comment                   |
|-----------|---------------------------|
| ER0 == 1  | crc_error                 |
| ER1 == 1  | cutoff_error              |
| ER2 == 1  | big_value_error           |
| ER3 == 1  | hufftable_error           |
| ER4 == 1  | mod_buf_size_error        |
| ER5 == 1  | huffman_decode_error      |
| ER6 == 1  | dynpart_exchange_error    |
| ER7 == 1  | gr_length_error           |
| ER8 == 1  | input_bit_available_error |
| ER9 == 1  | ch_length_error           |
| ER10 == 1 | head_framelength_error    |
| ER11 == 1 | dynpart_length_error      |
| ER12 == 1 | block_type_error          |
| ER13 == 1 | head_emphasis_error       |
| ER14 == 1 | head_samp_freq_error      |
| ER15 == 1 | head_layer_error          |

**3.13 ADPCM\_CONFIGURATION registers description**

**CHAN\_NB :**

|           |           |           |           |           |           |           |           |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| <b>b7</b> | <b>b6</b> | <b>b5</b> | <b>b4</b> | <b>b3</b> | <b>b2</b> | <b>b1</b> | <b>b0</b> |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|

Address : 0x70 (112)  
 Type : RW - DEC  
 Software Reset : 0

Description :

It allows the user to specify the number of channel of the stream to encode.

| Value | Codec   |
|-------|---|
| 1     | stream mono encoded as mono                       |
| 2     | stream stereo encoded as stereo                   |
| 5     | stream stereo encoded as mono with left channel.  |
| 9     | stream stereo encoded as mono with right channel. |

stream mono stands for only 1 channel is transmitted, data are also not interleaved.

Encode a stereo stream as mono reduce from an half the encoded data.

**SAMPLING\_FREQ. :**

|           |           |           |           |           |           |           |           |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| <b>b7</b> | <b>b6</b> | <b>b5</b> | <b>b4</b> | <b>b3</b> | <b>b2</b> | <b>b1</b> | <b>b0</b> |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|

Address : 0x71 (113)  
 Type : RW - DEC  
 Software Reset : 0

Description :  
 It allows the user to specify the sampling frequency of the stream to encode. See table 6 of sample frequencies.

**ENC\_STATE\_REPEAT :**

|           |           |           |           |           |           |           |           |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| <b>b7</b> | <b>b6</b> | <b>b5</b> | <b>b4</b> | <b>b3</b> | <b>b2</b> | <b>b1</b> | <b>b0</b> |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|

Address : 0x72 (114)  
 Type : RW - DEC  
 Software Reset : 0

Description :  
 It allows the user to specify at which frequency the state of the encoder should be repeated in the stream : (1/HOST\_ENC\_STATE\_REPEAT) frame.



**ENC\_CODEC :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x73 (115)

Type : RW - DEC

Software Reset : 0

Description :

It allows the user to specify the codec to use for the encoding:

| Value | Codec     |
|-------|-----------|
| 0     | Intel/DVI |
| 1     | G723_24   |
| 2     | G721      |
| 3     | G723_40   |

**ENC\_FRAME\_LEN :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x74 (116)

Type : RW - DEC

Software Reset : 0

Description :

It allows the user to specify the number of words by channel included in 1 frame: value from 1 to 15 (multiplied by 64 inside dsp).

**3.14 MIX\_CONFIGURATION registers description**

**MIX\_MODE:**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x75 (117)

Type : RW - ABO

Software Reset : 2

Description :

This register selectes the mode of mix/volume control

:

| Value | Mode                        |
|-------|-----------------------------|
| 0     | diseable mix/volume control |
| 1     | volume control              |
| 2     | mono to stereo (up-mix)     |
| 3     | stereo to mono (down-mix)   |

**MIX\_DLA:**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x76 (118)

Type : RW - ABO

Software Reset : 0

Description :

This register specifies the direct left attenuation (in dB).

**MIX\_DLB:**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x77 (119)

Type : RW - ABO

Software Reset : 0

Description :

This register specifies the left attenuation (in dB) on righth channel.

**MIX\_DRA:**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x78 (120)

Type : RW - ABO

Software Reset : 0

Description :

This register specifies the direct right attenuation (in dB).

**MIX\_DRB:**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x79(121)

Type : RW - ABO

Software Reset : 0

Description :

This register specifies the right attenuation (in dB) on left channel.

**3.15 TONE\_CONFIGURATION registers description**

**TONE\_ON:**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x7A(122)

Type : RW - ABO

Software Reset : 0

Description :

This register enables/disables (1/0) the tone control.

**TONE\_FCUTH :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x7B(123)

Type : RW - ABO

Software Reset : 20

Description :

This register specifies the high cut frequency:  $f_{cut}(in\ Hz)=(TONE\_FCUTH+1)*50$ .

**TONE\_FCUTL :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x7C(124)

Type : RW - ABO

Software Reset : 10

Description :

This register specifies the low cut frequency:  $f_{cut}(in\ Hz) = (TONE\_FCUTL+1)*10$

**TONE\_GAINH :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x7D(125)

Type : RW - ABO

Software Reset : 12

Description :

This register specifies the gain on high frequencies:  $gain(in\ Db)=(TONE\_GAINH-12)*1.5$

**TONE\_GAINL :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x7E(126)

Type : RW - ABO

Software Reset : 12

Description :

This register specifies the gain on high frequencies:  $gain\ (in\ Db)=(TONE\_GAINL-12)*1.5$ . Value of register from 0 to 24.

**TONE\_GAIN\_ATTEN :**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

Address : 0x7F(127)

Type : RW - ABO

Software Reset : 0

Description :

This register specifies the attenuation on global spectrum:  $gain\ (in\ dB)=-TONE\_GAIN\_ATTEN*1.5$ . Value of register from 0 to 12.

## 3.16 TABLES

**Table 2. values to configure audio PLL for ofact==256.**

This table give values to configure the audio PLL according CRYCK so that to generate a PCMCK == 256\*SF.

| Register           | CRYCK in MHz<br>10 | CRYCK in MHz<br>14.31818 | CRYCK in MHz<br>14.7456 |
|--------------------|--------------------|--------------------------|-------------------------|
| PLL_AUDIO_PEL_192  | 42                 | 58                       | 85                      |
| PLL_AUDIO_PEH_192  | 169                | 187                      | 85                      |
| PLL_AUDIO_NDIV_192 | 0                  | 0                        | 0                       |
| PLL_AUDIO_XDIV_192 | 3                  | 3                        | 0                       |
| PLL_AUDIO_MDIV_192 | 18                 | 12                       | 2                       |
| PLL_AUDIO_PEL_176  | 56                 | 54                       | 0                       |
| PLL_AUDIO_PEH_176  | 16                 | 118                      | 64                      |
| PLL_AUDIO_NDIV_176 | 0                  | 0                        | 0                       |
| PLL_AUDIO_XDIV_176 | 3                  | 2                        | 3                       |
| PLL_AUDIO_MDIV_176 | 17                 | 8                        | 11                      |

**Table 3. values to configure audio PLL for ofact==384**

This table give values to configure the audio PLL according CRYCK so that to generate a PCMCK == 384\*SF.

| Register           | CRYCK in MHz<br>10 | CRYCK in MHz<br>14.31818 | CRYCK in MHz<br>14.7456 |
|--------------------|--------------------|--------------------------|-------------------------|
| PLL_AUDIO_PEL_192  | 224                | 108                      | 0                       |
| PLL_AUDIO_PEH_192  | 190                | 76                       | 0                       |
| PLL_AUDIO_NDIV_192 | 0                  | 0                        | 0                       |
| PLL_AUDIO_XDIV_192 | 1                  | 1                        | 1                       |
| PLL_AUDIO_MDIV_192 | 13                 | 9                        | 9                       |
| PLL_AUDIO_PEL_176  | 42                 | 54                       | 0                       |
| PLL_AUDIO_PEH_176  | 140                | 118                      | 48                      |
| PLL_AUDIO_NDIV_176 | 0                  | 0                        | 0                       |
| PLL_AUDIO_XDIV_176 | 1                  | 1                        | 1                       |
| PLL_AUDIO_MDIV_176 | 12                 | 8                        | 8                       |

**Table 4. values to configure audio PLL for ofact==512.**

This table give values to configure the audio PLL according CRYCK so that to generate a PCMCK == 512\*SF.

| Register           | CRYCK in MHz<br>10 | CRYCK in MHz<br>14.31818 | CRYCK in MHz<br>14.7456 |
|--------------------|--------------------|--------------------------|-------------------------|
| PLL_AUDIO_PEL_192  | 42                 | 58                       | 85                      |
| PLL_AUDIO_PEH_192  | 169                | 187                      | 85                      |
| PLL_AUDIO_NDIV_192 | 0                  | 0                        | 0                       |
| PLL_AUDIO_XDIV_192 | 1                  | 0                        | 1                       |
| PLL_AUDIO_MDIV_192 | 18                 | 5                        | 12                      |
| PLL_AUDIO_PEL_176  | 56                 | 157                      | 0                       |
| PLL_AUDIO_PEH_176  | 16                 | 157                      | 64                      |
| PLL_AUDIO_NDIV_176 | 0                  | 0                        | 0                       |
| PLL_AUDIO_XDIV_176 | 1                  | 1                        | 1                       |
| PLL_AUDIO_MDIV_176 | 17                 | 11                       | 11                      |

**Table 5. values to configure system PLL for SYSCK.**

This table give values to configure the system PLL according CRYCK so that to generate a SYSCK == 50MHz.  
or SYSCK == 42.5MHz.

| Register             | CRYCK in MHz 10 | CRYCK in MHz<br>14.31818 | CRYCK in MHz<br>14.7456 |
|----------------------|-----------------|--------------------------|-------------------------|
| PLL_SYSTEM_PEL_50    | 162             | 0                        | 28                      |
| PLL_SYSTEM_PEH_50    | 11              | 0                        | 152                     |
| PLL_SYSTEM_NDIV_50   | 0               | 0                        | 0                       |
| PLL_SYSTEM_XDIV_50   | 1               | 1                        | 1                       |
| PLL_SYSTEM_MDIV_50   | 19              | 13                       | 12                      |
| PLL_SYSTEM_PEL_42_5  | 0               | 126                      | 100                     |
| PLL_SYSTEM_PEH_42_5  | 0               | 223                      | 135                     |
| PLL_SYSTEM_NDIV_42_5 | 0               | 0                        | 0                       |
| PLL_SYSTEM_XDIV_42_5 | 1               | 1                        | 1                       |
| PLL_SYSTEM_MDIV_42_5 | 16              | 10                       | 10                      |

Table 6. index of the Sampling Frequency.

| Index              | Frequency         |
|--------------------|-------------------|
| 0                  | 48 kHz            |
| 1                  | 44.1 kHz          |
| 2                  | 32 kHz            |
| 4                  | 96 kHz            |
| 5                  | 88.2 kHz          |
| 6                  | 64 kHz            |
| 8                  | 24 kHz            |
| 9                  | 22.05 kHz         |
| 10                 | 16 kHz            |
| 12                 | 12 kHz            |
| 13                 | 11.025 kHz        |
| 14                 | 8 kHz             |
| 16                 | 192 kHz           |
| 17                 | 176.4 kHz         |
| 18                 | 128 kHz           |
| 3, 7, 11, 15 or 19 | illegal frequency |

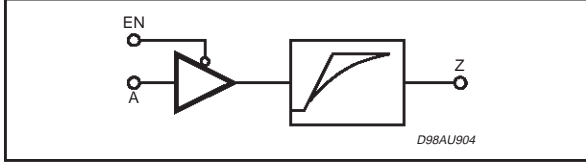
### 3.17 NOTATIONS

|         |   |
|---------|---|
| ABO     | : After B0ot (see I).   |
| AEC     | : After External Config (see I).  |
| BCK     | : Bit Clock   |
| BSA     | : BitStream input interface in Audio mode.                              |
| BSB     | : BitStream input interface in Burst mode.                              |
| BS      | : BitStream input interface.  |
| BYPASSA | : decoder BYPASS an Audio stream.                                       |
| CD      | : input interface for CD.   |
| CK      | : Clock.  |
| CRYCK   | : CRYstal Clock provided to the chip by an external crystal.            |
| DBO     | : During B0ot (see I).  |
| DEC     | : During External Config (see I).                                       |
| DWT     | : During Whole Time (see I).  |
| EDB     | : Every Decoded Block (see I).  |
| EDF     | : Every Decoded Frame (see I).  |
| LRCK    | : Left Right Clock for an I2S interface.                                |
| ofact   | : oversampling factor for PCMCK ( $PCMCK == ofact * SF$ ).              |
| PCMCK   | : PCM Clock (can be generated by the audio PLL).                        |
| SF      | : Sampling Frequency.   |
| SYSCK   | : SYStem Clock (clock of the core, can be generated by the system PLL). |
| X       | : don't care.   |

**I/O CELL DESCRIPTION**

**1) TTL Tristate Output Pad Buffer, 3V capable 4mA, with Slew Rate Control**

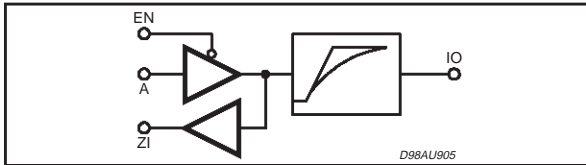
Pin numbers: 4, 18, 20, 21, 22, 25, 54, 56, 59



| INPUT PIN | MAX LOAD |
|-----------|----------|
| Z         | 100pF    |

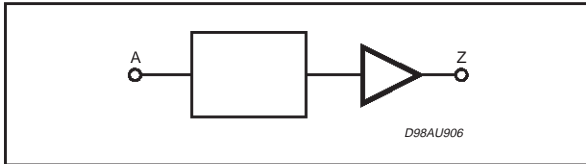
**2) TTL Schmitt Trigger Bidir Pad Buffer, 3V capable, 4mA, with Slew Rate Control**

Pin numbers: 1, 2, 3, 7, 8, 9, 19



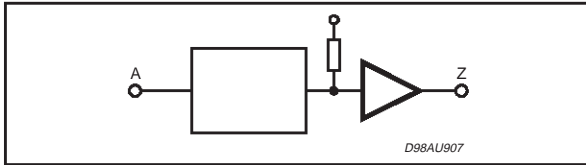
| INPUT PIN | CAPACITANCE | OUTPUT PIN | MAX LOAD |
|-----------|-------------|------------|----------|
| IO        | TBD         | IO         | 100pF    |

**3) TTL Schmitt Trigger Input Pad Buffer, 3V capable / Pin numbers:17, 60, 63**



| INPUT PIN | CAPACITANCE |
|-----------|-------------|
| A         | TBD         |

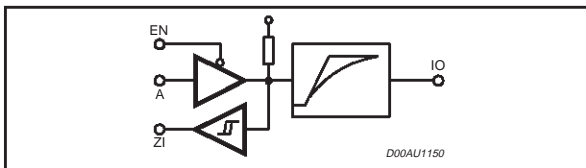
**4) TTL Input Pad Buffer, 3V capable with Pull-Up / Pin numbers:15, 16**



| INPUT PIN | CAPACITANCE |
|-----------|-------------|
| A         | TBD         |

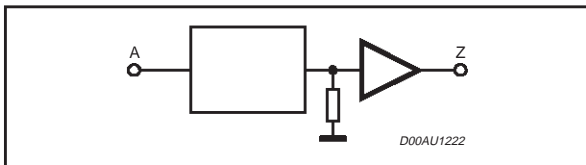
**5) TTL Schmitt Trigger Bidir Pad Buffer, with Pull-up, 4mA, with slew rate control / 3V capable**

Pin numbers: 26, 27, 28, 31, 32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 51, 64



| INPUT PIN | CAPACITANCE | OUTPUT PIN | MAX LOAD |
|-----------|-------------|------------|----------|
| IO        | TBD         | IO         | 100pF    |

**6) TTL Input Pad Buffer, 3V capable, with pull down / Pin numbers: 12, 13, 14, 55**



| INPUT PIN | CAPACITANCE |
|-----------|-------------|
| A         | TBD         |



## 4 COMMAND PROTOCOL CONFIGURATION

### General Information About The Command Protocol

#### I2C protocol :

CD\_module & mmdsp are using an I2C protocol to communicate : CD\_module is master of the I2C protocol, and can access (in read and write mode) host registers of the sta016 to write commands to the mmdsp and to read request from the mmdsp. It must use following I2C syntax :

device\_address, host\_register\_number, host\_register\_value

where :

for a write acces, device\_address is 0x86.

for a read acces, device\_address is 0x87.

#### Writing a command to mmdsp :

CD\_module write its command inside dedicated host registers (mainly H64 to H69), then it must signals the writing of this command to mmdsp by sending the interrupt IT\_CMD to the core of mmdsp.

Note that IT\_CMD is generated by cd\_module threw a falling edge on the input line number 0 of the sta016 (the INTLINE[0]pin).

#### Reading a request from mmdsp :

MMDSP write its request inside dedicated host registers (mainly H70 to H78 and H134 to H169), then it signals to cd\_module that it must read a request by sending the interrupt IT\_REQ.

Note that IT\_REQ interrupt is generated by mmdsp on the IRQB pin of sta016.

Note also that once it has finished to read the message, cd\_module must always acknowledge it by reading H10.

Figure 4. Block diagram for running the CD application.

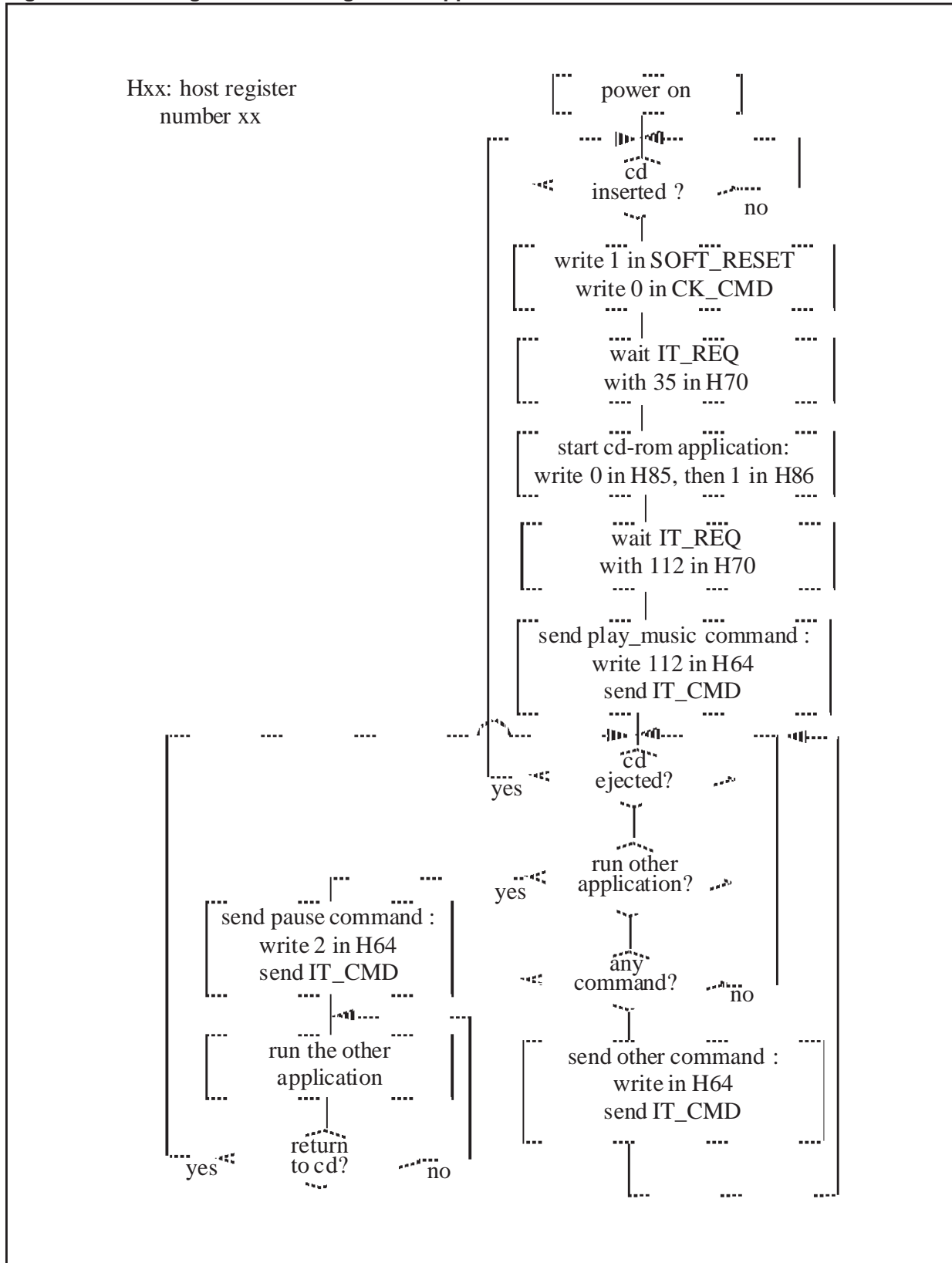
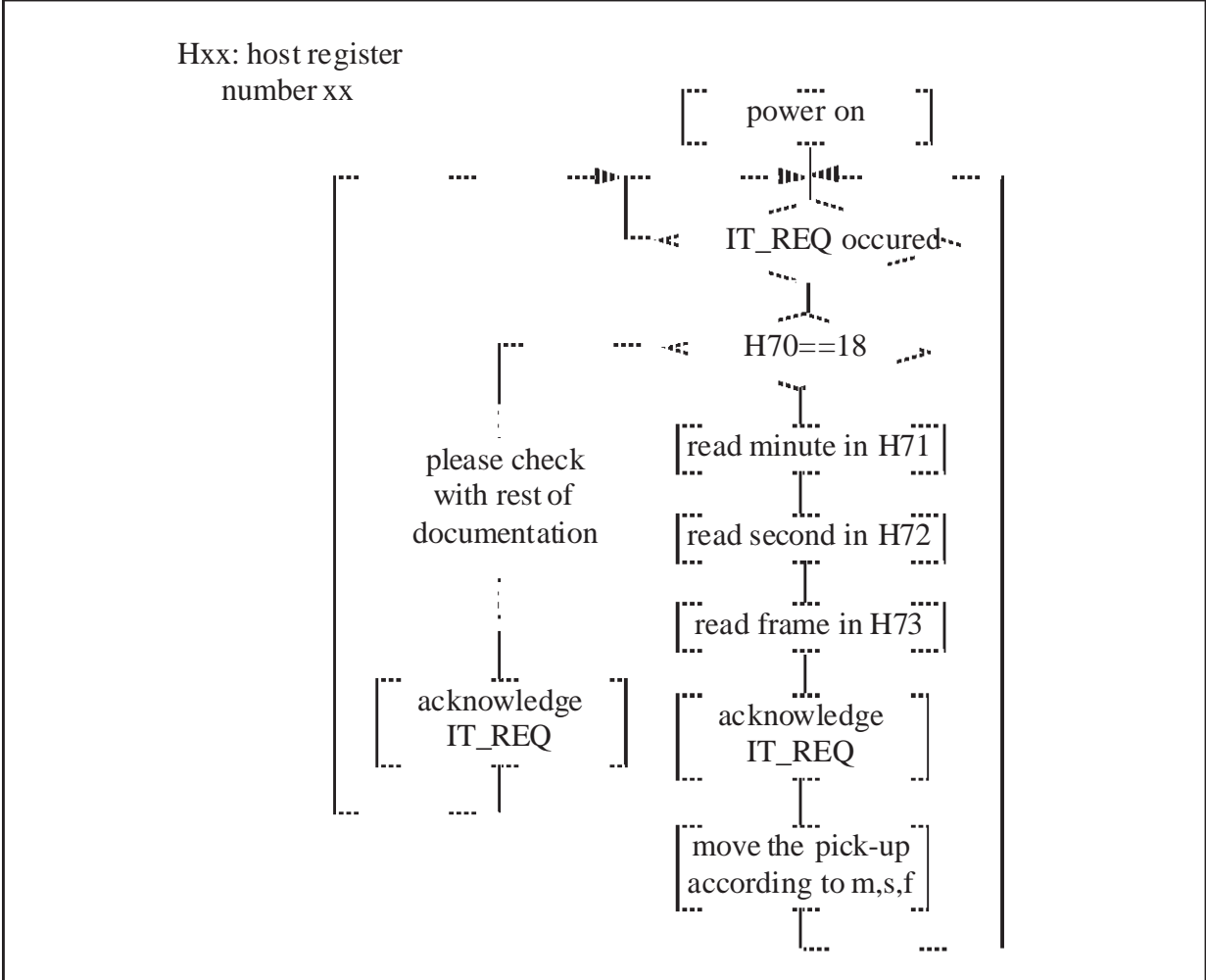
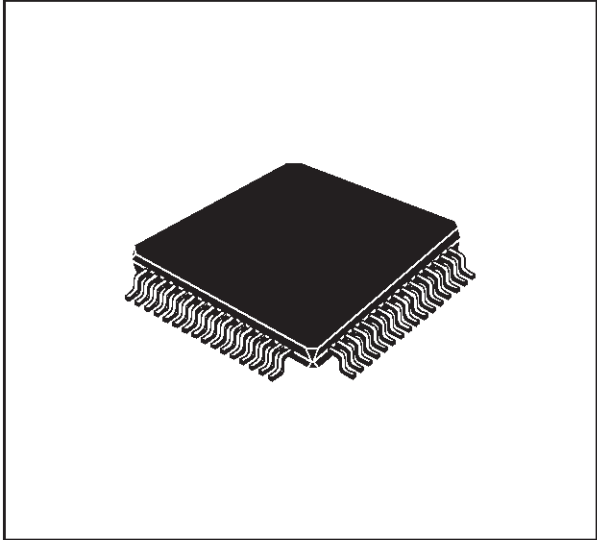


Figure 5. Block diagram for answer to a sector request from dsp.

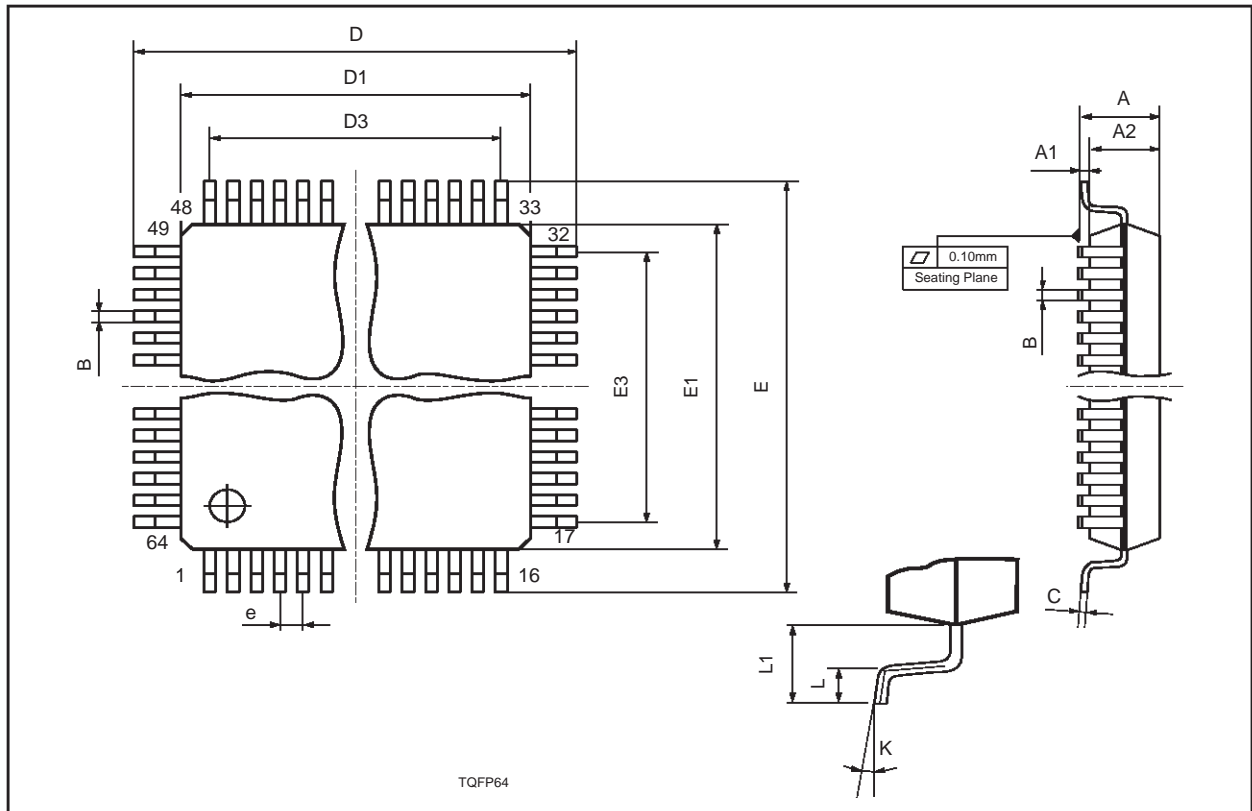


| DIM. | mm                 |       |      | inch   |        |        |
|------|--------------------|-------|------|--------|--------|--------|
|      | MIN.               | TYP.  | MAX. | MIN.   | TYP.   | MAX.   |
| A    |                    |       | 1.60 |        |        | 0.063  |
| A1   | 0.05               |       | 0.15 | 0.002  |        | 0.006  |
| A2   | 1.35               | 1.40  | 1.45 | 0.053  | 0.055  | 0.057  |
| B    | 0.18               | 0.23  | 0.28 | 0.007  | 0.009  | 0.011  |
| C    | 0.12               | 0.16  | 0.20 | 0.0047 | 0.0063 | 0.0079 |
| D    |                    | 12.00 |      |        | 0.472  |        |
| D1   |                    | 10.00 |      |        | 0.394  |        |
| D3   |                    | 7.50  |      |        | 0.295  |        |
| e    |                    | 0.50  |      |        | 0.0197 |        |
| E    |                    | 12.00 |      |        | 0.472  |        |
| E1   |                    | 10.00 |      |        | 0.394  |        |
| E3   |                    | 7.50  |      |        | 0.295  |        |
| L    | 0.40               | 0.60  | 0.75 | 0.0157 | 0.0236 | 0.0295 |
| L1   |                    | 1.00  |      |        | 0.0393 |        |
| K    | 0°(min.), 7°(max.) |       |      |        |        |        |

**OUTLINE AND MECHANICAL DATA**



**TQFP64**



**Note:1**

STA016 is a device based on an integrated DSP core. Some of the I<sup>2</sup>C registers default values are loaded after an internal DSP boot operation. The bootstrap time is 60 micro second. Only after this time length, the data in the register can be considered stable.

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