AVERLOGIC

AL4CA01/02/03/04/05

512/ 1K/ 2K/ 4K/ 8K x 9 Asynchronous FIFOs

Applications

- ATM switches
- Routers
- Cable modems
- Wireless base stations
- SONET(Synchronous Optical Network) multiplexers
- Multimedia systems
- TBC(Time Base Corrector)
- Hard Disk cache memory
- Buffer for Communications

Description

The AL4CA01/02/03/04/05 Asynchronous FIFO (First In First Out) memory provides completely independent 9bit bus width input and output port control that have a maximum data access time as fast as 12ns. The products are available in densities from 4Kbit to 64Kbit with word depths from 512bit to 8Kbit.

Features

- High performance, low-power, FIFO(First-In First-Out) memory
- 512 x9 bit I/O port (AL4CA01)
- 1K x9 bit I/O port (AL4CA02)
- 2K x9 bit I/O port (AL4CA03)
- 4K x9 bit I/O port (AL4CA04)
- 8K x9 bit I/O port (AL4CA05)
- Asynchronous 12ns access time
- Fully independent input/output port access
- Empty, Full, Half Full flags
- Auto Retransmit
- Cascadable expansion in depth and width
- 3.3-volt power tolerant of 5-volt input
- Standard 32-pin PLCC,

Ordering Information

Part number	AL4CA01, AL4CA02, AL4CA03, AL4CA04, AL4CA05
Package	32-pin plastic PLCC
Power Supply	+3.3V±10%

PLCC TOP VIEW
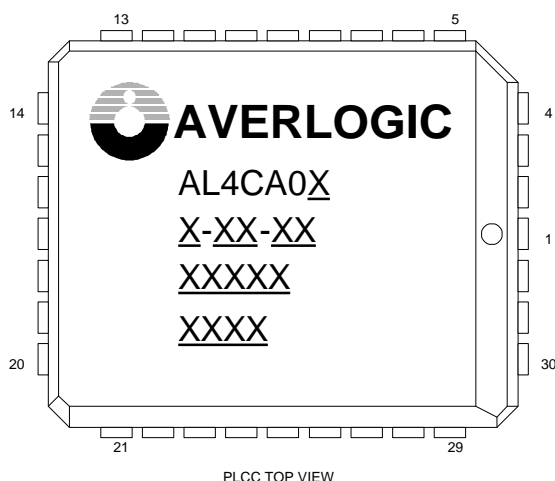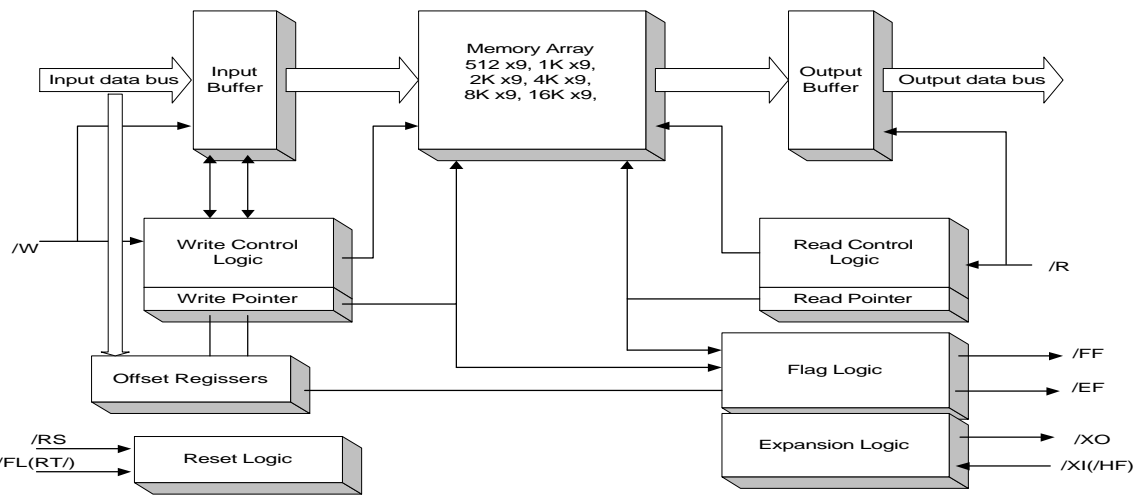
AL4CA0x FIFO Block Diagram

The read and write operations are internally sequential through the managing of address pointers, with no address line control required to store and retrieve data. Data is toggled in and out of the FIFO through the use of the Write and Read enable pins.

Additional features of the AL4CA0x series include: Retransmit(/RT) that allows for reset of the read pointer and do the retransmit operation; Empty, Full and Half-Full flags can indicate the FIFO accessible capacity. AL4CA0x FIFO memory is AverLogic Technologies, latest products that is designed to buffer data for a wide range of application such as optical storage controllers, Networking Switches and various communication applications. The embedded memory array with built-in address decoder, pointer manager and state-of-the-art circuits provide an easy-to-use interface to serial read/write memory and offer a flexible way to manage memory in the system design.

There are 3 flag signals, Empty Flag/Output Ready and Full Flag/Input Ready, and Half Full flags that enable further manipulation of the synchronous control.

Multiple AL4CX0xs can be cascaded to expand the storage depth or can be used in parallel to expand bus width.

The FIFOs are 3.3-volt devices with 5-volt input tolerance. And are available in the 32-pin PLCC Package.

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