

21-26.5GHz Down converter *Preliminary*

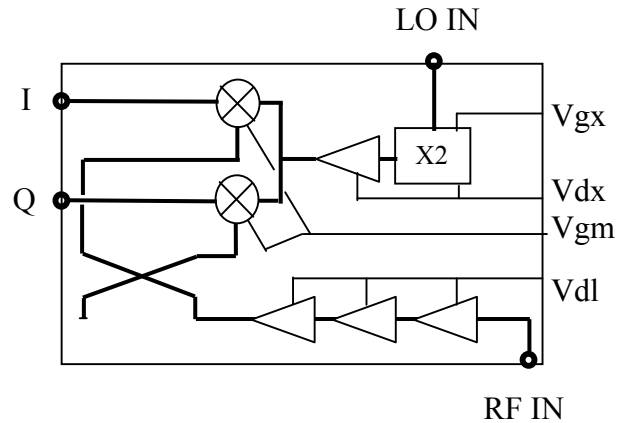
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GaAs Monolithic Microwave IC in SMD package

Description

The CHR3693-QDG is a multifunction part, which integrates a balanced cold FET mixer, a time two multiplier, and a RF LNA. It is designed for a wide range of applications, typically commercial communication systems.

The circuit is manufactured with a PM-HEMT process, 0.25µm gate length, via holes through the substrate and air bridges.

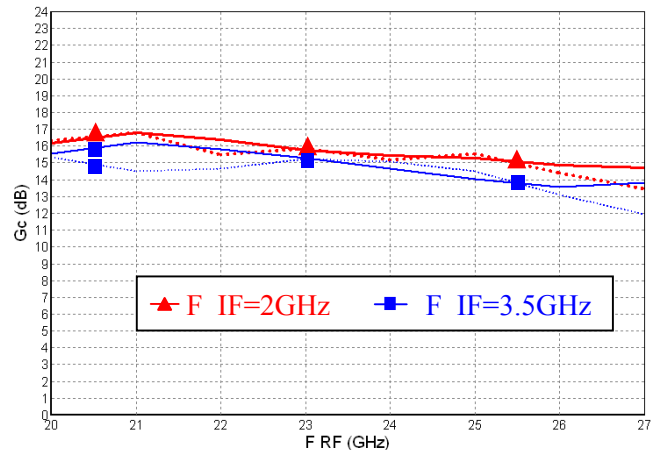


It is supplied in lead-free SMD package.

Main Features

- Broadband performance 21-26.5GHz
- 14dB gain
- -5dBm IIP3
- 18dBc Image rejection
- 24LQFN4x4

Conversion gain (Inf. & Sup. Mode)



Main Characteristics

T_{amb.} = 25°C, V_d = 4V

Symbol	Parameter	Min	Typ	Max	Unit
F _{RF}	RF frequency range	21		26.5	GHz
F _{LO}	LO frequency range	9		14	GHz
F _{IF}	IF frequency range	DC		3.5	GHz
G _c	Conversion gain		14		dB

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

Electrical Characteristics

Tamb=25°C, Vdx=Vdl = 4V, Typical Vgx = -0.9V & Vgm= -0.7V

These values are representative of onboard measurements (on connector access planes) as defined on the drawing 96401

Preliminary

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Symbol	Parameter	Min	Typ	Max	Unit
F _{RF}	RF frequency range	21		26.5	GHz
F _{LO}	LO frequency range	9		14	GHz
F _{IF}	IF frequency range	DC		3.5	GHz
G _c	Conversion gain		14		dB
NF	Noise Figure		3		dB
P _{LO}	LO Input power		2		dBm
Img Sup	Image Suppression (1)		18		dBc
IIP3	Input IP3		-5		dBm
LO VSWR	Input LO VSWR		2.0:1		
RF VSWR	Input RF VSWR (21 to 23.6GHz) Input RF VSWR (24.5 to 26.5GHz)		1.7:1 2.3:1		
LO/RF	Isolation LO → RF		45		dBc
2LO/RF	Isolation 2LO → RF		35		dBc
I _d	Bias current (2)		160		mA

(1) With external I/Q 90° hybrid coupler

(2) Typically, I_{dl}= 90mA, I_{dx}=70mA

Absolute Maximum Ratings (1)

Tamb = +25°C

Symbol	Parameter	Values	Unit
V _d	Maximum drain bias voltage	4.5	V
I _d	Maximum drain bias current	230	mA
V _g	Gate bias voltage	-2.0 to +0.4	V
P _{RF}	Maximum RF input power	10	dBm
P _{LO}	Maximum LO input power	10	dBm
T _{ch}	Maximum channel temperature (2)	175	°C
T _a	Operating temperature range	-40 to +85	°C
T _{stg}	Storage temperature range	-55 to +125	°C

(1) Operation of this device above anyone of these paramaters may cause permanent damage.

(2) Thermal Resistance channel to ground paddle = 63.6°C/W for Tamb. = +85°C

Typical Measured Performance

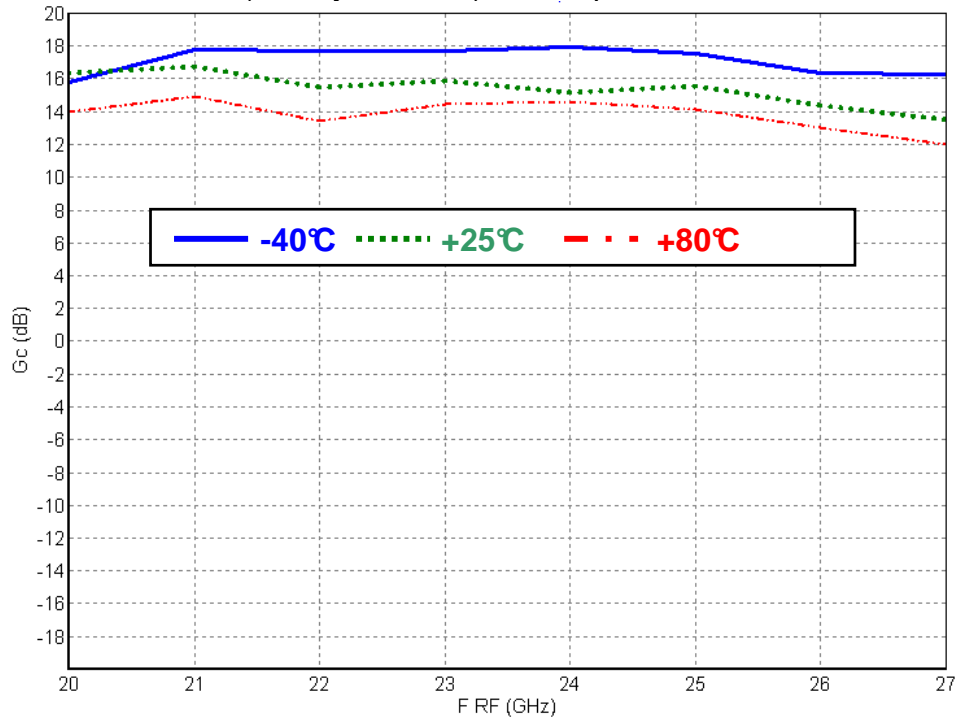
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Tamb. = 25°C, Vdx=Vdl = 4V, Typical Vgx = -0.9V & Vgm= -0.7V

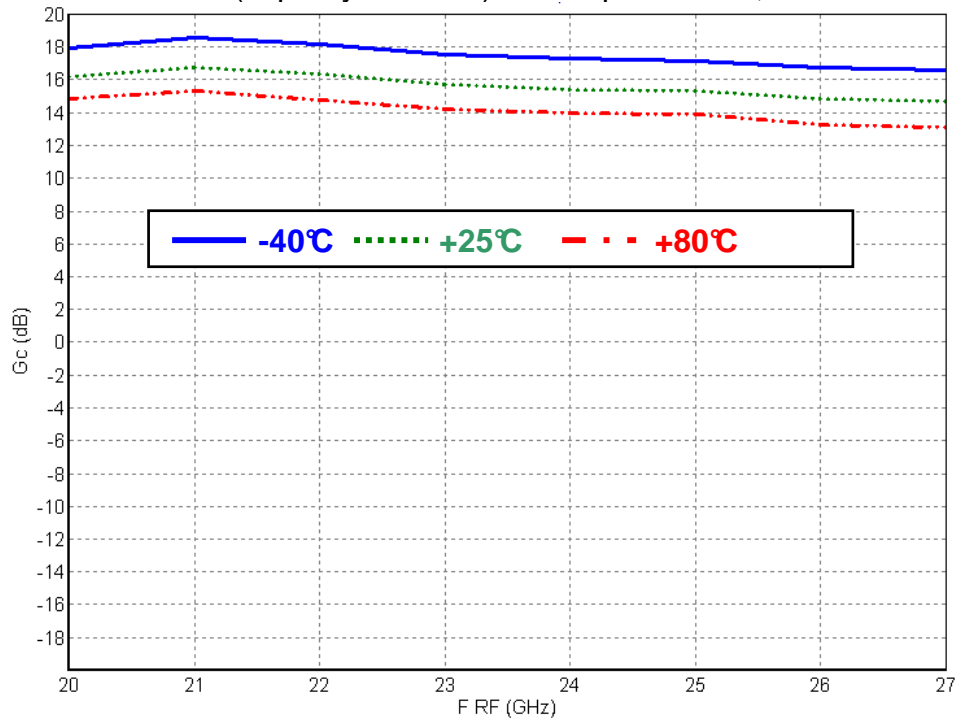
These values are representative of onboard measurements as defined on the drawing 96401 (on connector access planes)

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Conversion Gain (infradyne mode) @ Freq_IF=2GHz, P_LO=2dBm



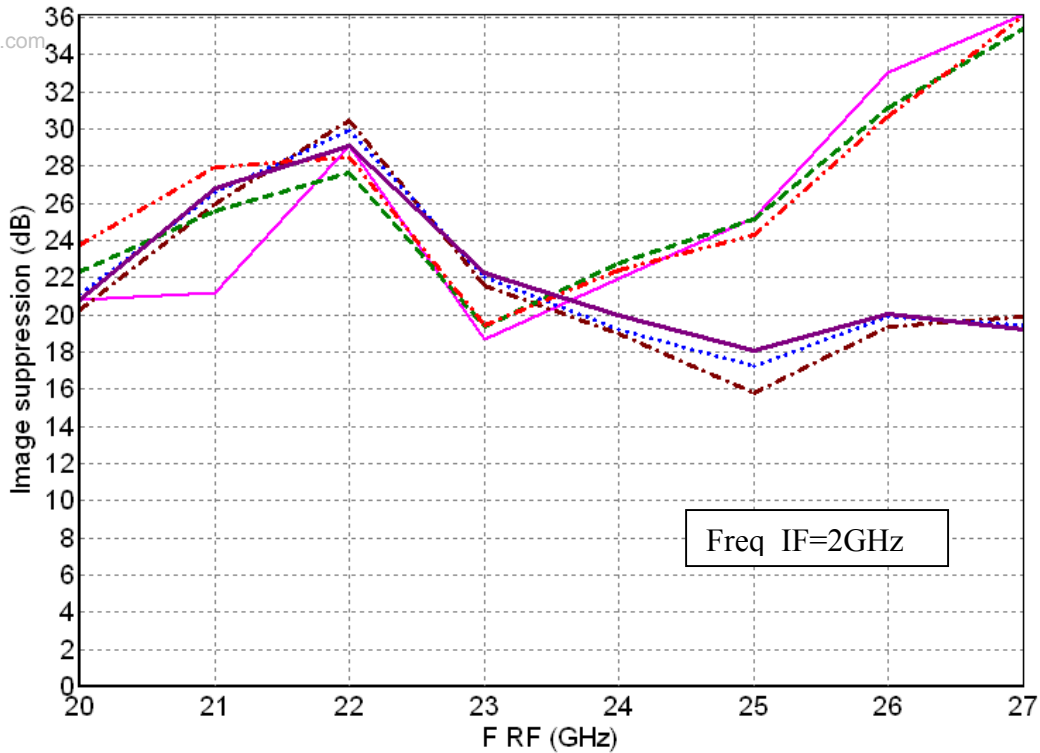
Conversion Gain (supradyne mode) @ Freq_IF=2GHz, P_LO=2dBm



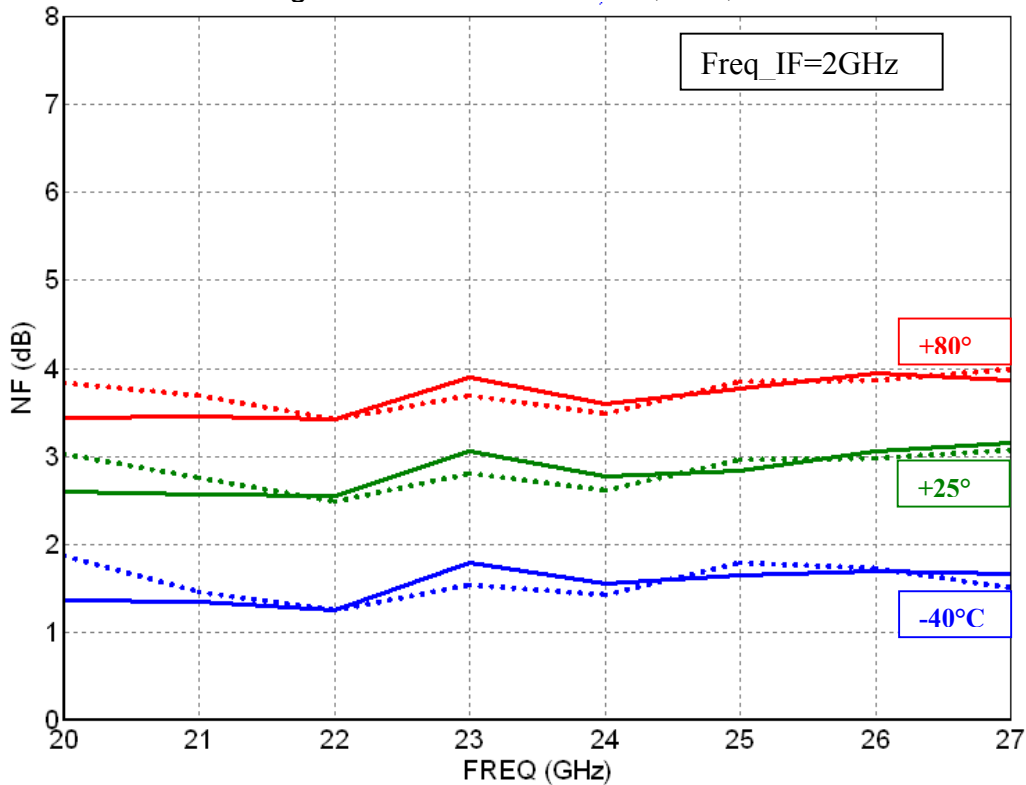
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Image Frequency rejection (inf. & sup. Mode) @ -40, +25, +80°C

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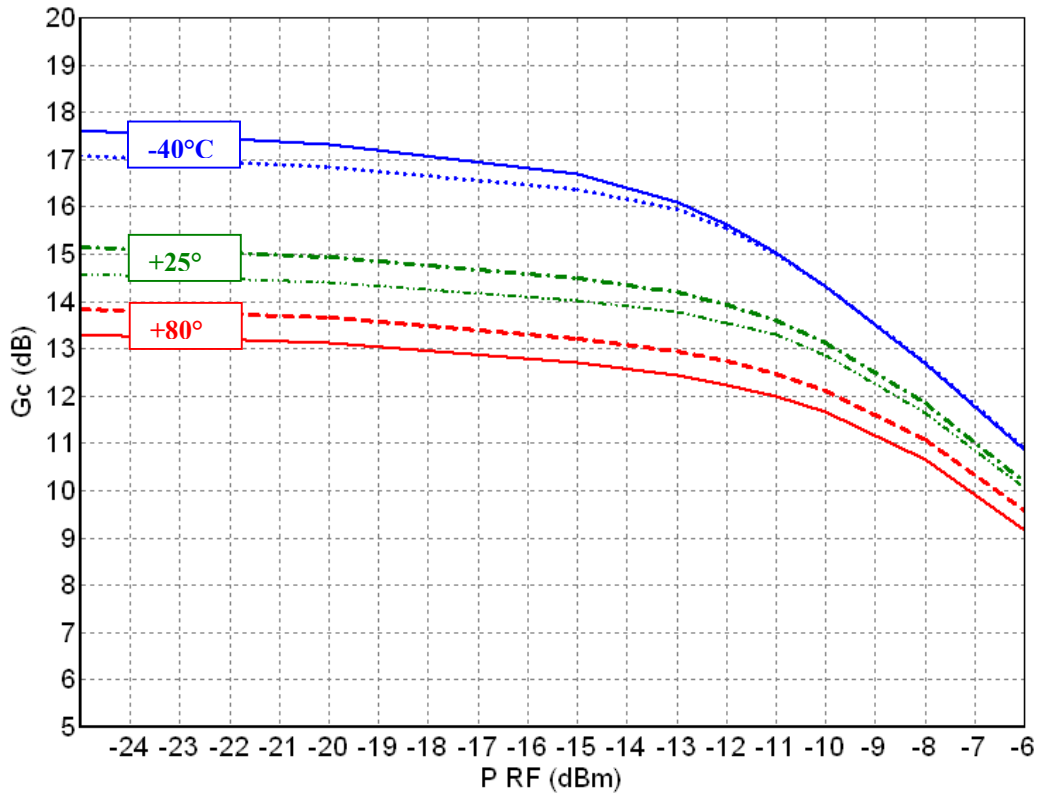
Noise figure channel I & Q @ -40, +25, +80°C



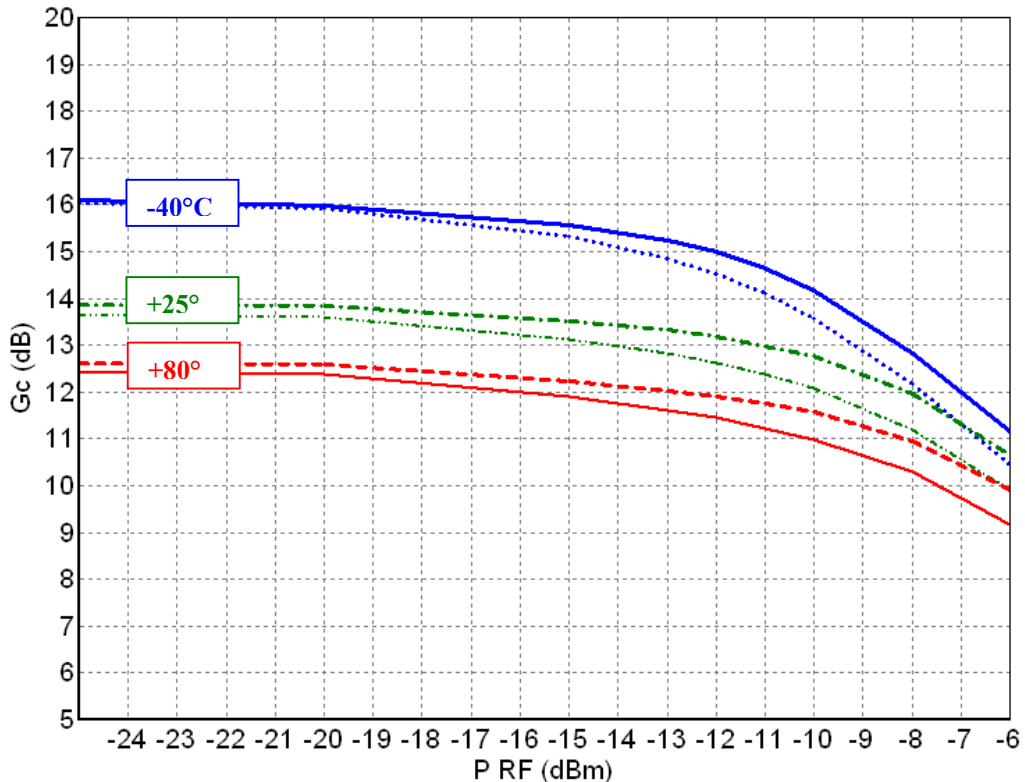
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Compression vs P_{RF} (inf. & sup. Mode) @ F_{RF}=21GHz & F_{IF}=3GHz
P_{LO}=2dBm

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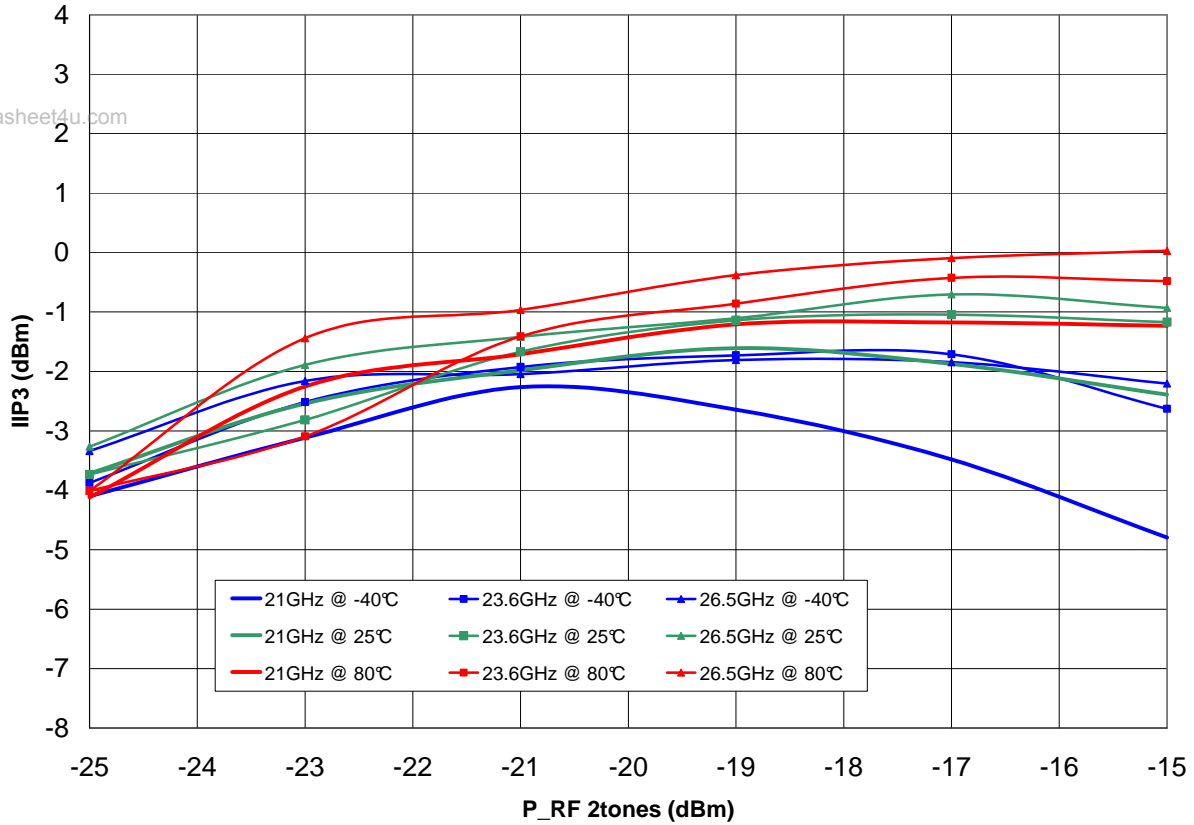
Compression vs P_{RF} (inf. & sup. Mode) @ F_{RF}=26GHz & F_{IF}=2GHz
P_{LO}=2dBm



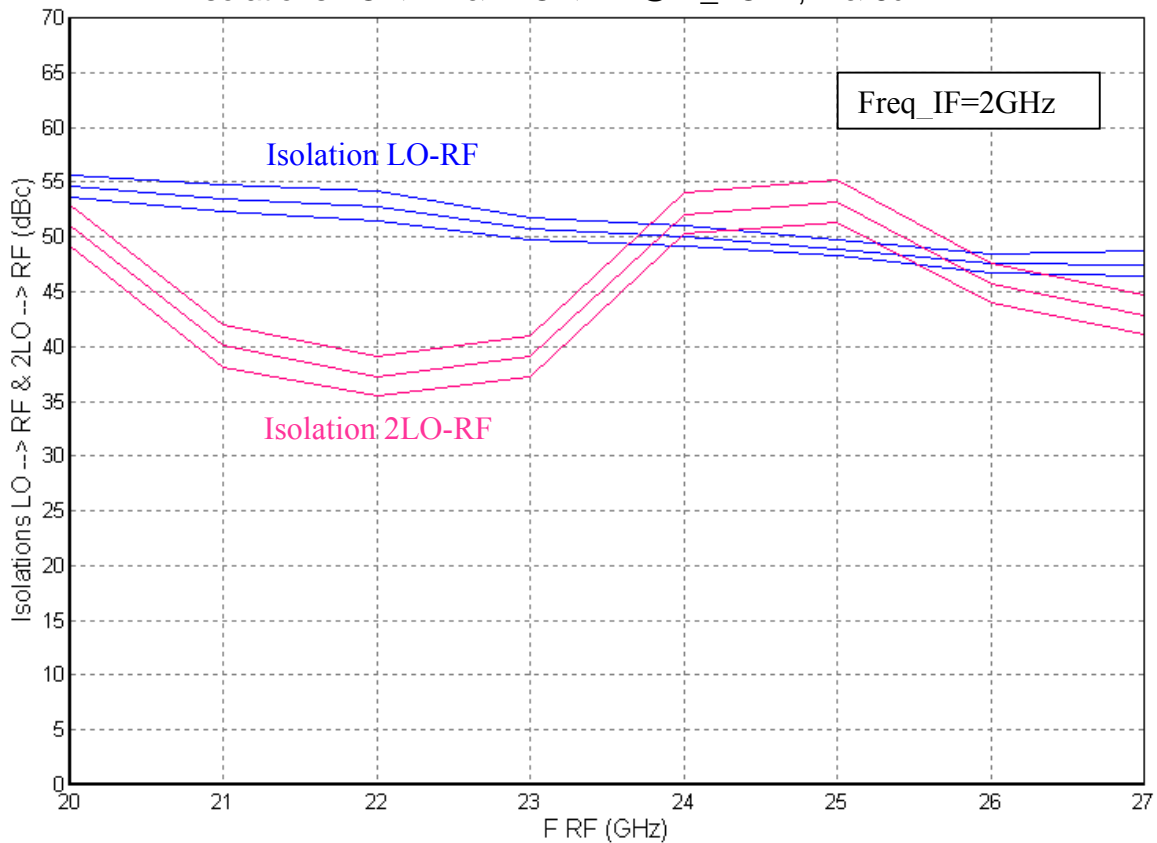
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Input IP3 versus RF power

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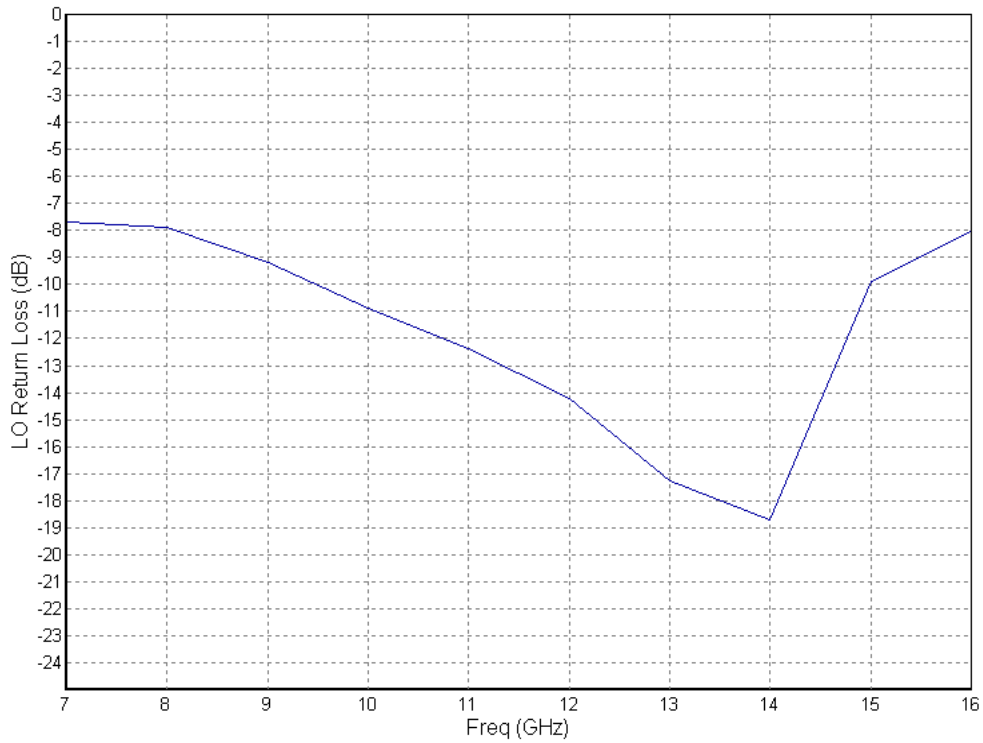


Isolations LO→RF & 2LO→RF @ P_LO=2, 4 & 6dBm

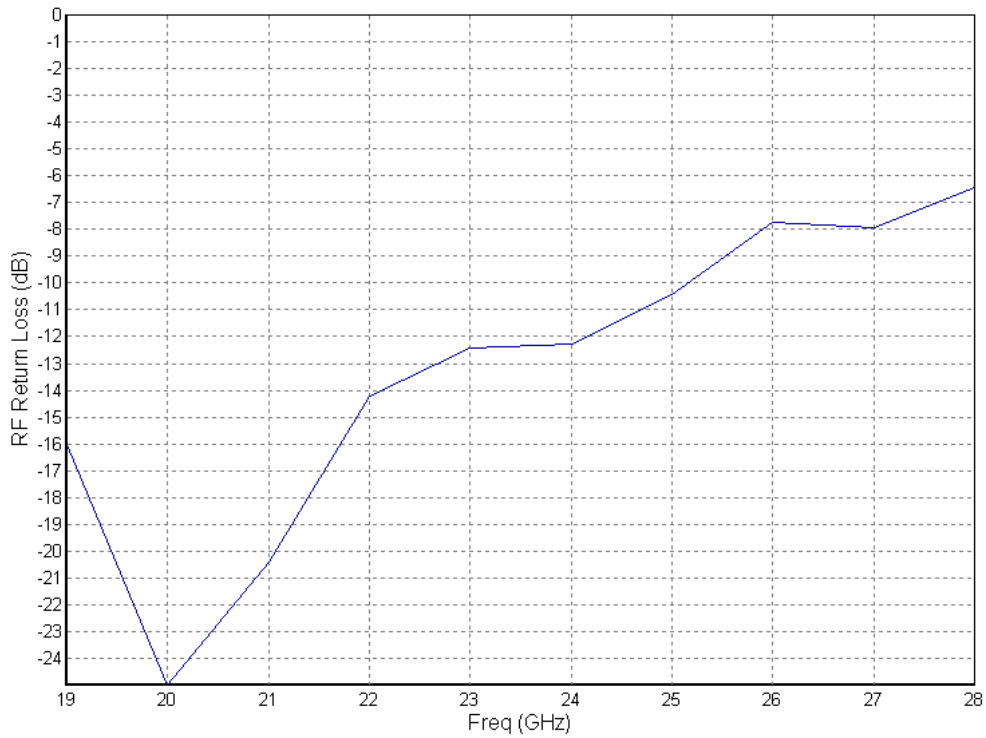


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LO Return Loss



RF Return Loss

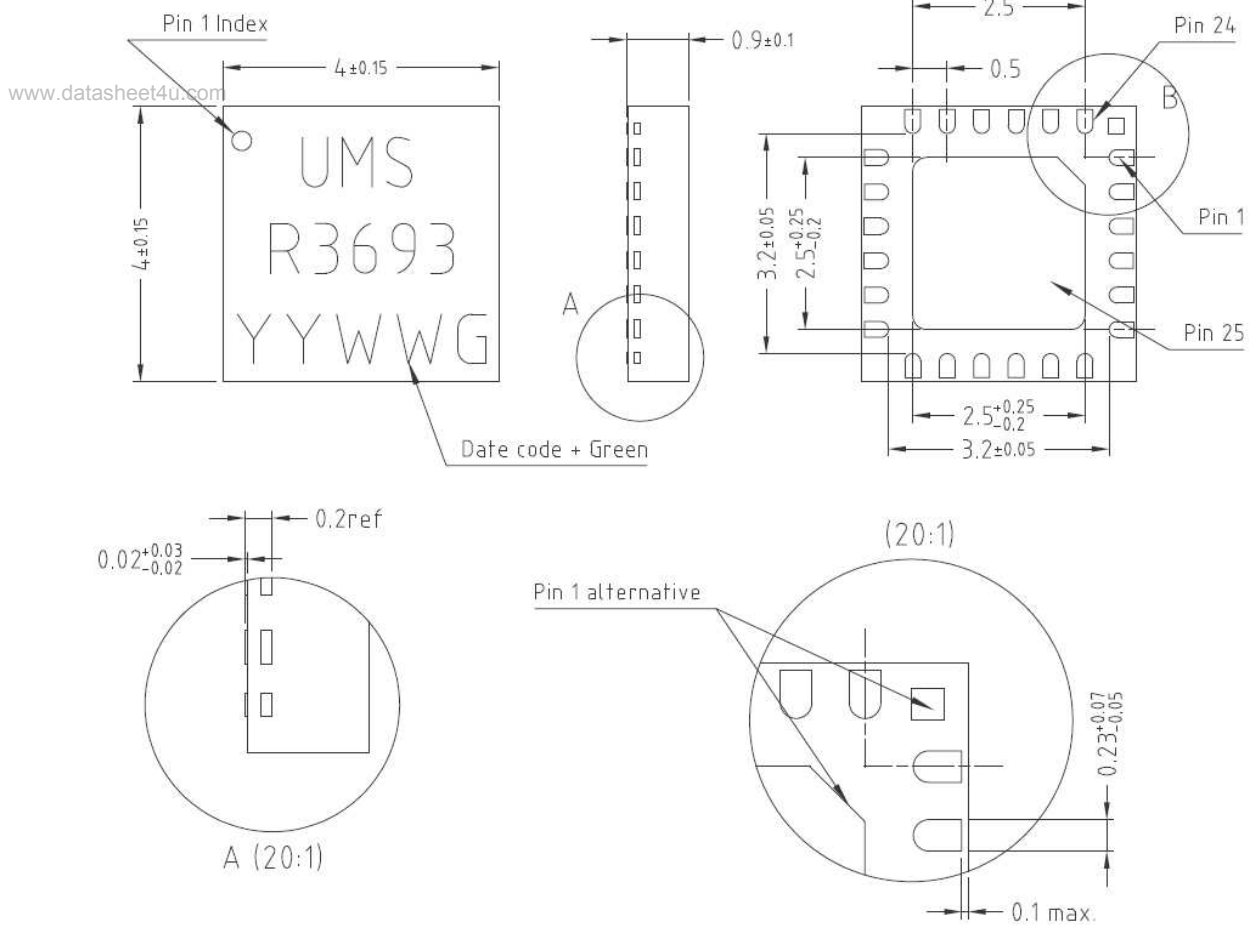


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Package outline:



Matt tin, Lead Free
Units
From the standard
Pin 25 (paddle): GND

(Green)
mm
JEDEC MO-220

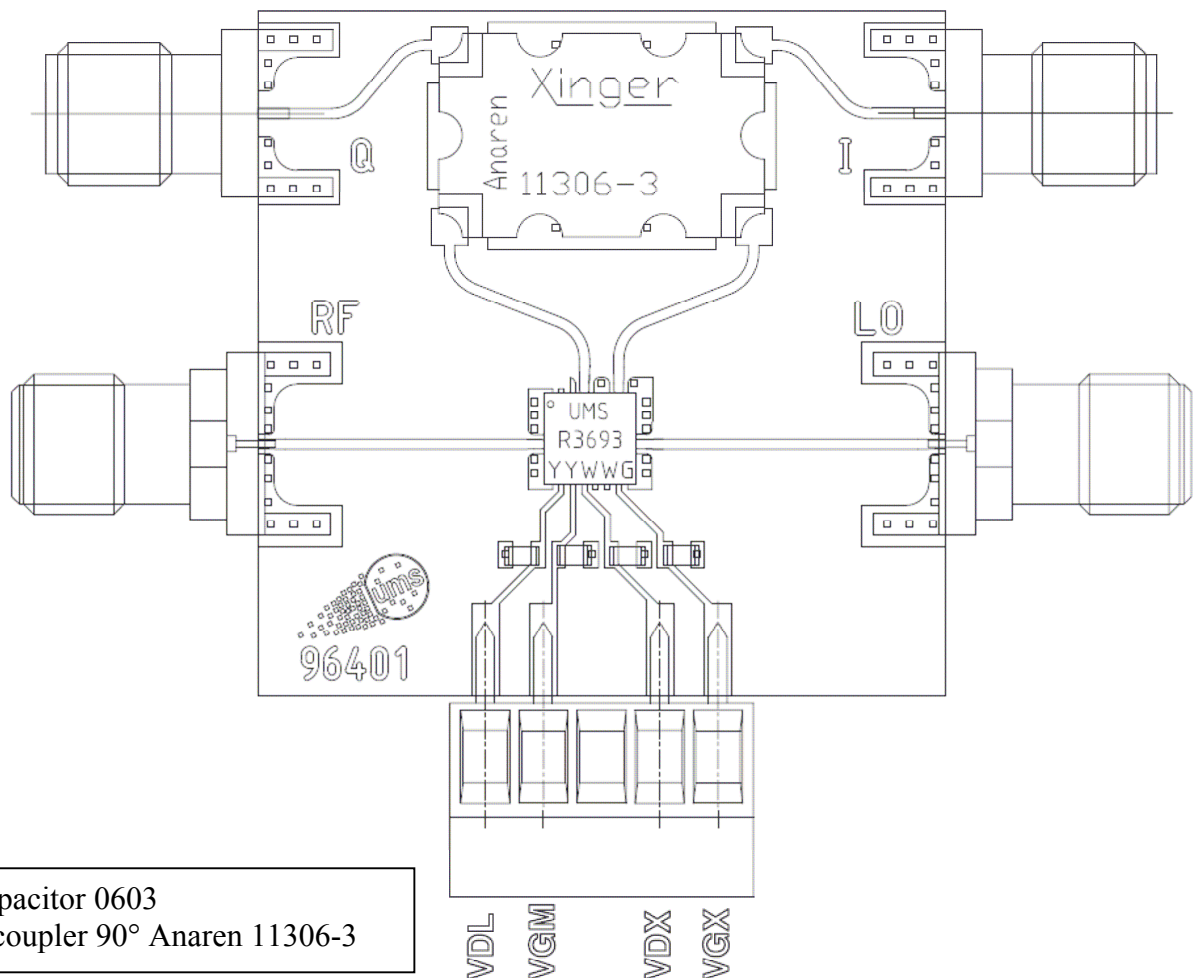
- | | |
|----------|--------------|
| 1- NC | 13- GND |
| 2- GND | 14- GND |
| 3- GND | 15- LO IN |
| 4- RF IN | 16- GND |
| 5- GND | 17- GND |
| 6- GND | 18- NC |
| 7- Vdl | 19- I-IF OUT |
| 8- Vgm | 20- GND |
| 9- Vdx | 21- GND |
| 10- NC | 22- Q-IF OUT |
| 11- NC | 23- NC |
| 12- Vgx | 24- NC |

Preliminary

Proposed Assembly board "96401" for the 24L-QFN4x4 product characterization.

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- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.



10nF capacitor 0603
Hybrid coupler 90° Anaren 11306-3

The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

The SMD leadless package has been designed for high volume surface mount PCB assembly process. A typical footprint is proposed for the PCB (motherboard) in the previous drawing. For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

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Ordering Information

QFN 4x4 RoHS compliant package: CHR3693-QDG/XY
Stick: XY = 20 Tape & reel: XY = 21

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