37-40GHz Integrated Down converter

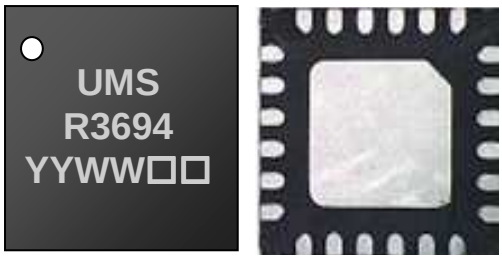
GaAs Monolithic Microwave IC in SMD package

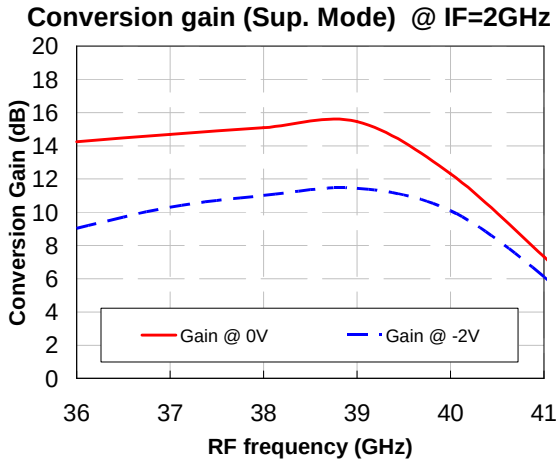
Description

The CHR3694-QDG is a multifunction chip, which integrates a balanced cold FET mixer, a time two multiplier, and a RF LNA including gain control.
It is designed for a wide range of applications, typically commercial communication systems.

The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate and air bridges.

It is available in lead-free SMD package.
A mirror version versus RF & LO access is available as CHR3794-QDG.





Main Features

- Broadband performance 37-40GHz
- 12dB Gain
- 15dBc Image Frequency Rejection
- -5dBm IIP3
- 4dB Gain control
- DC power consumption: 4V, 150mA
- 24L-QFN4x4
- ESD protected
- MSL Level 1

Main Characteristics

Tamb = +25°C, VDL= VDX= 4V

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	37		40	GHz
F_{LO}	LO frequency range	17.5		21	GHz
F_{IF}	IF frequency range	DC		3.5	GHz
G	Conversion gain @ VGC=-2V	8	10		dB
	Conversion gain @ VGC=0V	11	14		dB

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

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Electrical Characteristics

Tamb= +25℃, VDL= VDX= 4V, Typical VGX = -0.9V & VG M= -0.7V

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	37		40	GHz
F_{LO}	LO frequency range	17.5		21	GHz
F_{IF}	IF frequency range	DC		3.5	GHz
G	Conversion gain @ VGC = -2V	8	10		dB
	Conversion gain @ VGC = 0V	11	14		dB
PLO	LO Input power		1		dBm
IFR	Image Frequency Rejection (1)	13	15		dBc
NF	Noise Figure @ VGC = -2V		5	6.5	dB
	Noise Figure @ VGC = 0V		4.5	6	dB
IIP3	Input IP3		-5		dBm
LO RL	Input LO Return Loss		-10	-8	dB
RF RL	Input RF Return Loss		-4	-3	dB
Gc	Gain control range		4		dB
VDL,VDX	Drain bias voltage		4		V
VGC	Gain control voltage (2)	-2		0	V
Idl + Idx	Bias current @ VGC = -2V (3)	100	140	180	mA
	Bias current @ VGC = 0V (3)	110	150	190	mA

(1) With external I/Q 90° hybrid coupler

(2) Idl=50mA@VGC=-2V, Idl= 60mA@VGC=0V

(3) Typically, Idl=60mA@VGC=0V, Idx=90mA

These values are representative of onboard measurements as defined on the drawing at page 16 for CHR3694-QDG and page 17 for CHR3794-QDG.

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Absolute Maximum Ratings (1)

Tamb = +25℃

Symbol	Parameter	Values	Unit
VDL,VDX	Maximum drain bias voltage	4.5	V
Idl + Idx	Maximum drain bias current	200	mA
VGM,VGX	Gate bias voltage	-2.0 to +0	V
VGC	Control gain voltage	-3.0 to +4	V
P_RF	Maximum RF input power	10	dBm
P_LO	Maximum LO input power	10	dBm
Tch	Maximum channel temperature	175	℃
Ta	Operating temperature range	-40 to +85	℃
Tstg	Storage temperature range	-55 to +125	℃

(1) Operation of this device above anyone of these paramaters may cause permanent damage.

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).

The temperature is monitored at the package back-side interface (Tcase) as shown below. The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

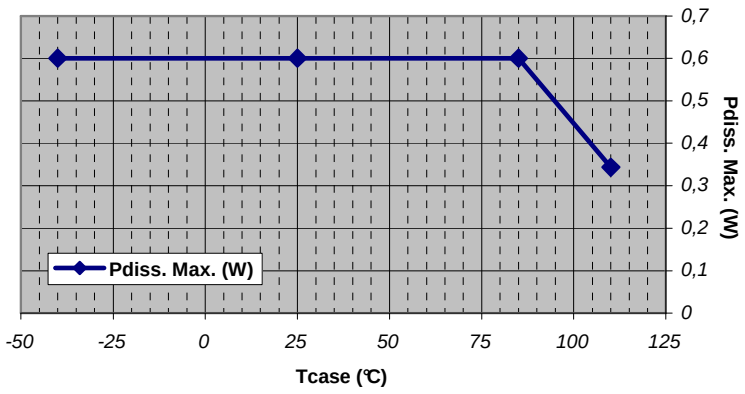
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below than the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

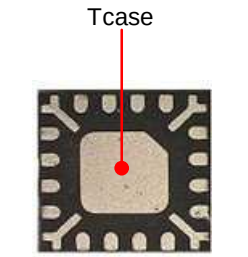
DEVICE THERMAL SPECIFICATION : CHR3694-QDG			
Max. junction temperature (Tj max)		:	144 ℃
Max. continuous dissipated power @ Tcase=	85 ℃	:	0,6 W
=> Pdiss derating above Tcase(1)=	85 ℃	:	10 mW/℃
Junction-Case thermal resistance (Rth J-C)(2)		:	<97 ℃/W
Min. package back side operating temperature(3)		:	-40 ℃
Max. package back side operating temperature(3)		:	85 ℃
Min. storage temperature		:	-55 ℃
Max. storage temperature		:	125 ℃

(1) Derating at junction temperature constant = Tj max.

*(2) Rth J-C is calculated for a worst case where the **hotter junction** of the MMIC is considered.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example of QFN 16L 3x3 back-side view, temperature reference point (Tcase) location.

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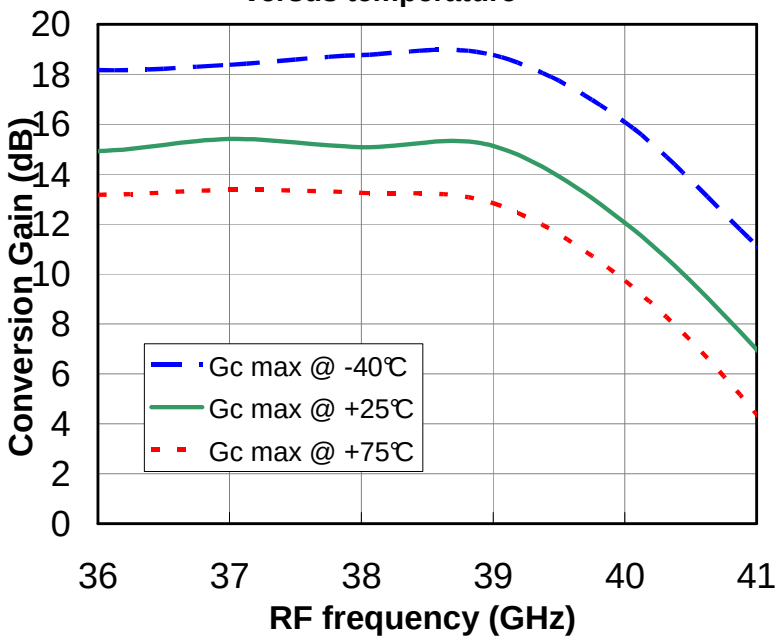
Typical Measured Performances

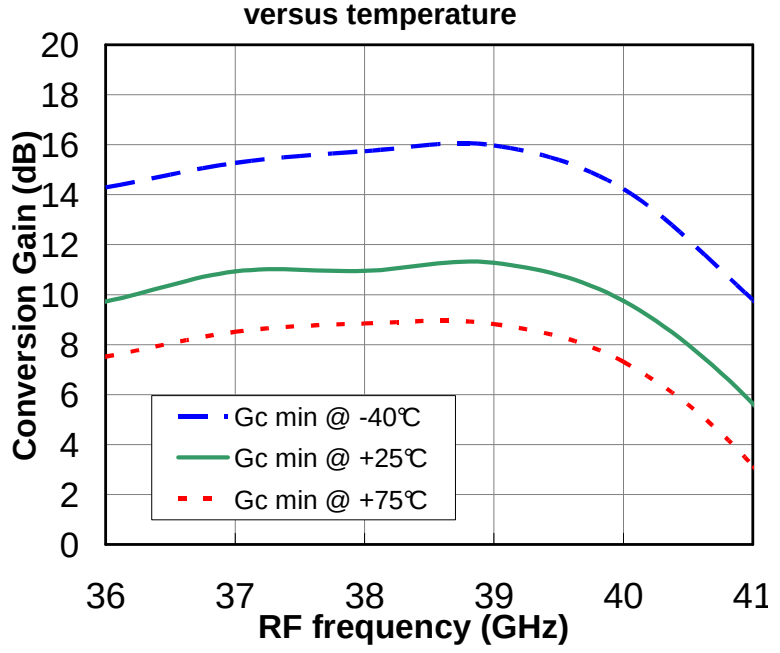
Tamb = +25℃, VDX=VDL = 4V, Typical VGX = -0.9V & V GM= -0.7V, P_LO=1dBm

These values are representative of onboard measurements (on connector access planes) as defined on the drawing 97445 page 16 for CHR3694-QDG and drawing 97342 page 17 for CHR3794-QDG. The board loss is estimated to 2 to 3dB in the frequency range.

Conversion Gain @ Freq_IF= 2GHz, F_RF= 2xF_LO - F_IF, VGC=0V versus temperature



Conversion Gain @ Freq_IF= 2GHz, F_RF= 2xF_LO - F_IF, VGC=-2V versus temperature



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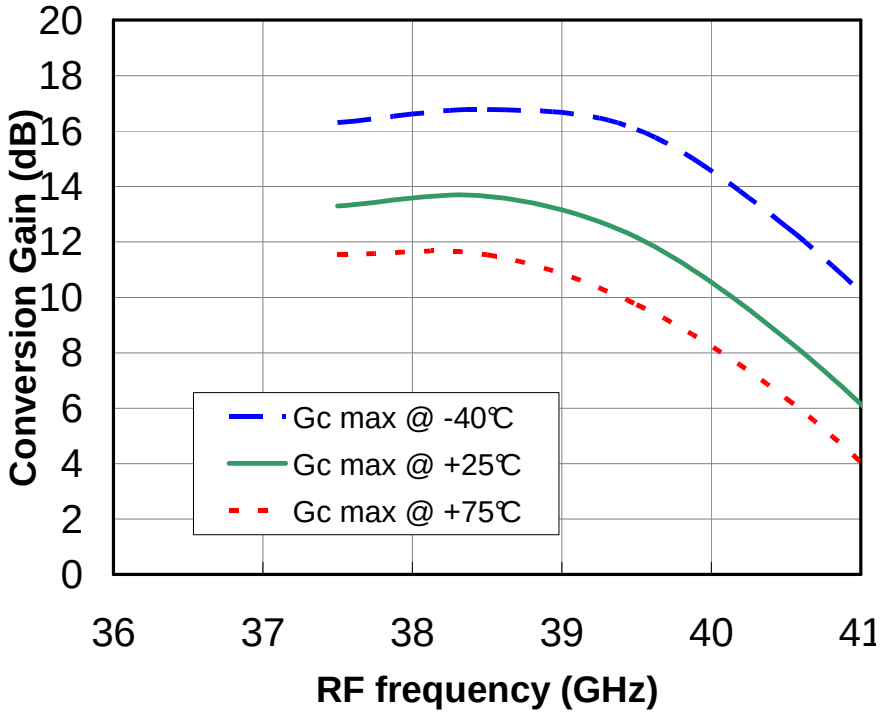
Conversion Gain @ Freq_IF= 3.5GHz, F_RF= 2xF_LO + F_IF, VGC=0V versus temperature



Conversion Gain @ Freq_IF= 3.5GHz, F_RF= 2xF_LO + F_IF, VGC=-2V versus temperature

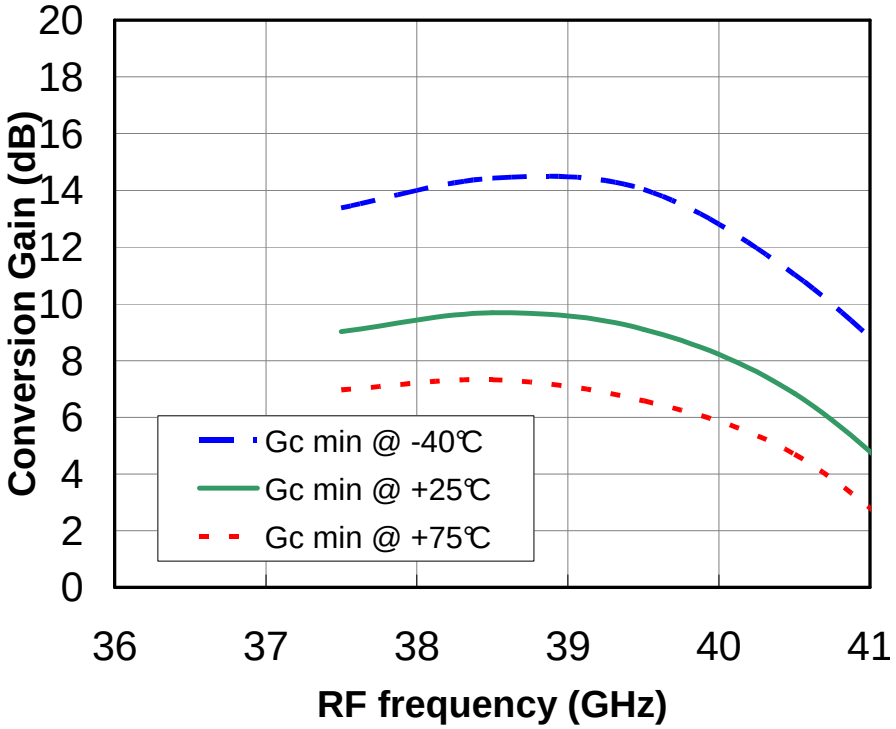


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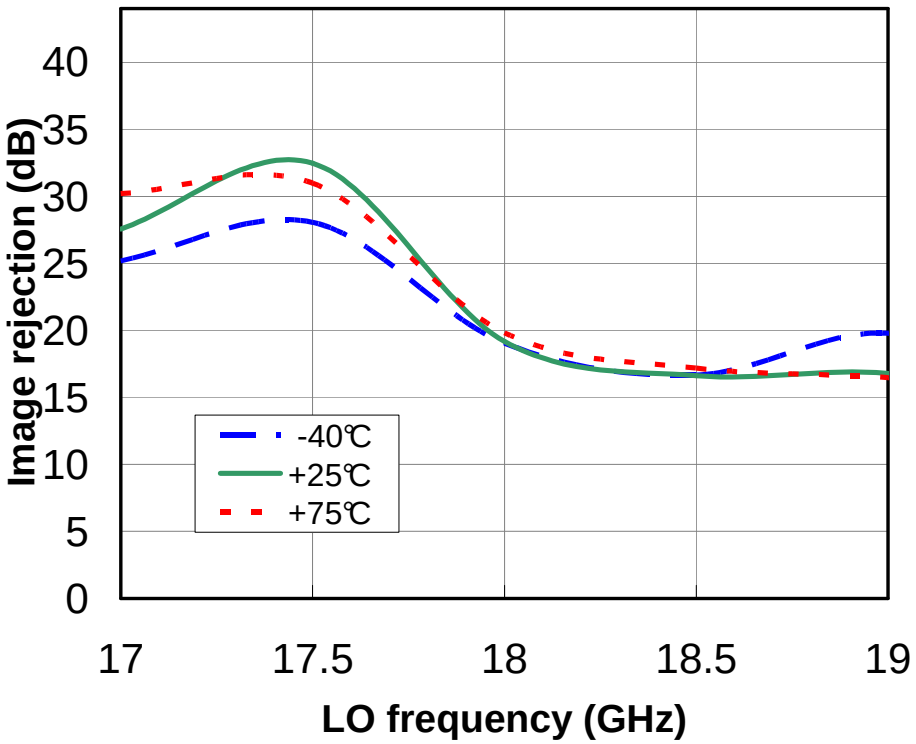
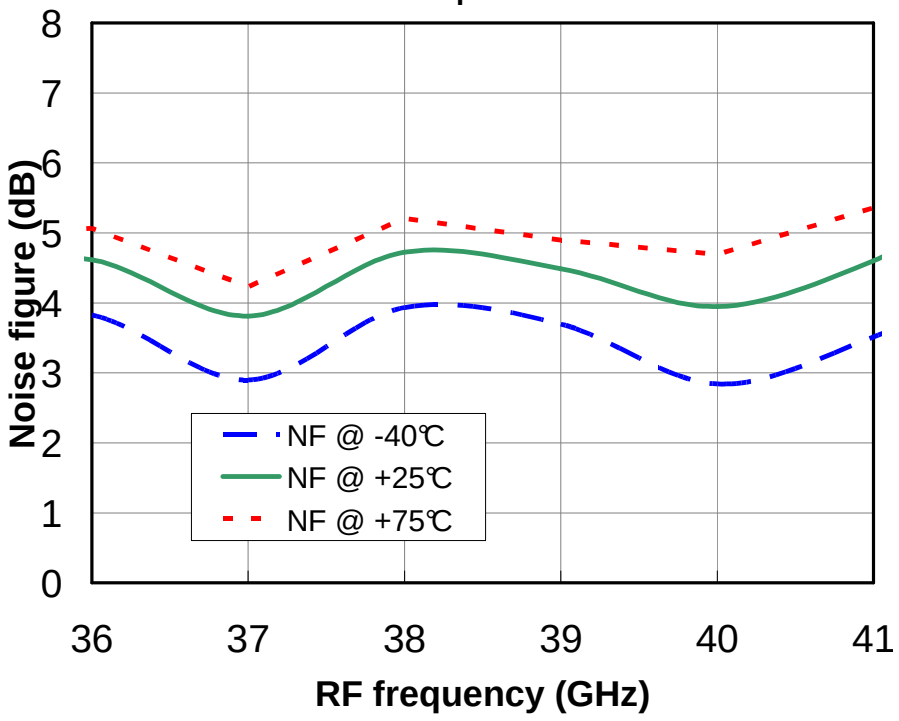
Image rejection @ Freq_IF= 2GHz, VGC=0V versus temperature



Noise figure @ Freq_IF= 3GHz, VGC=0V versus temperature



Rem: The losses due to board are removed for noise measurements.

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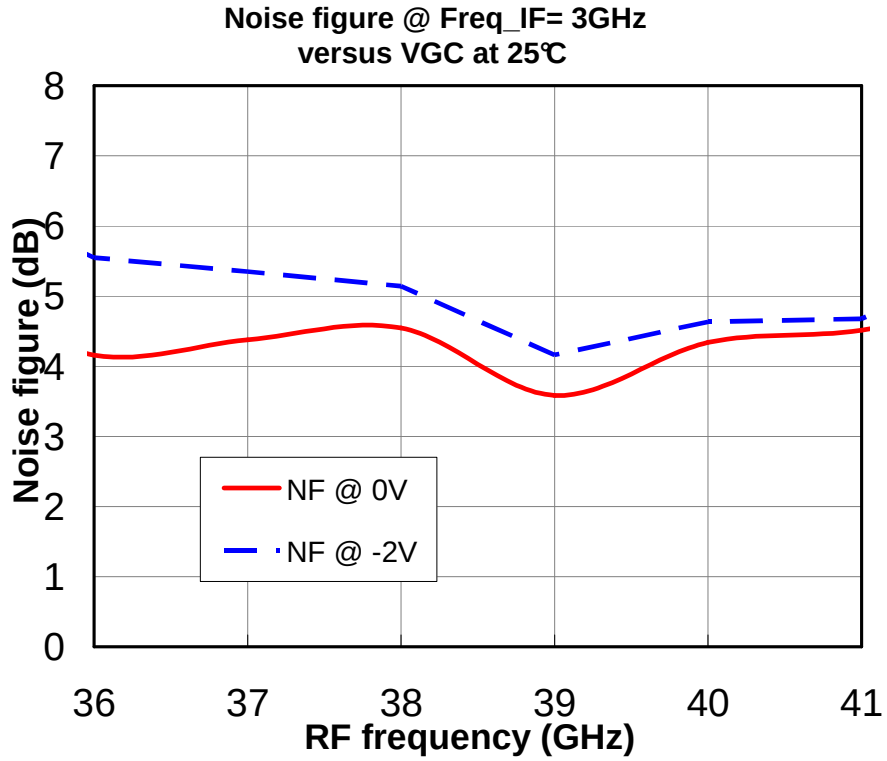
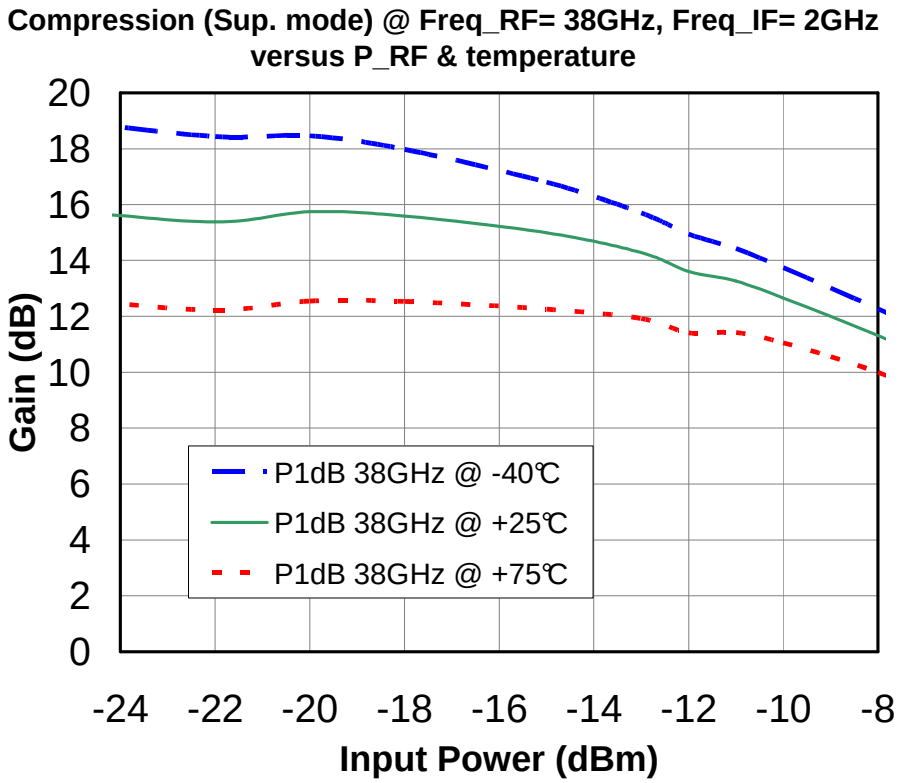


Rem: The losses due to board are removed for noise measurements.



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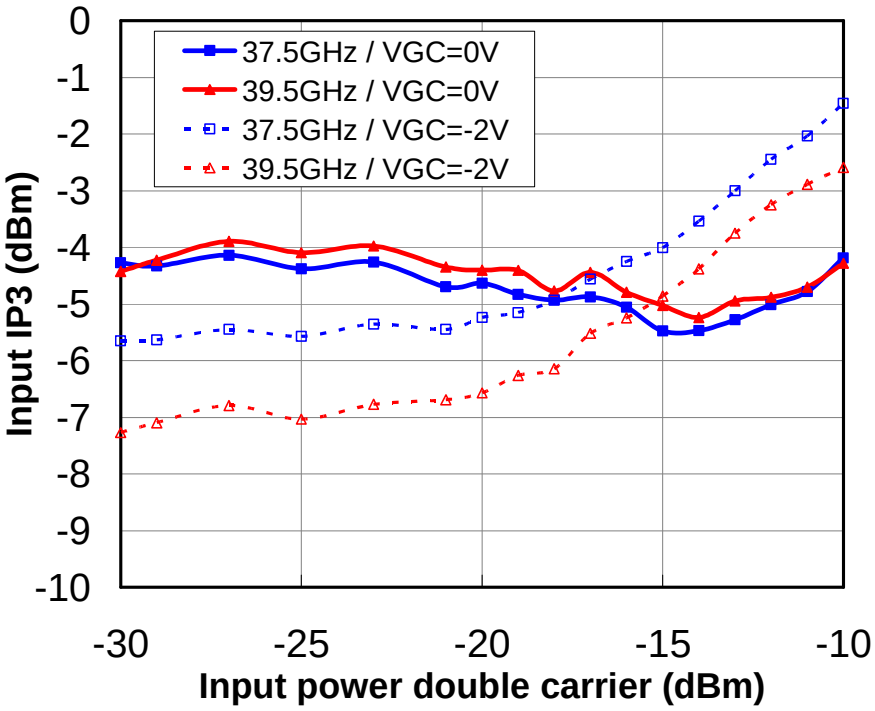
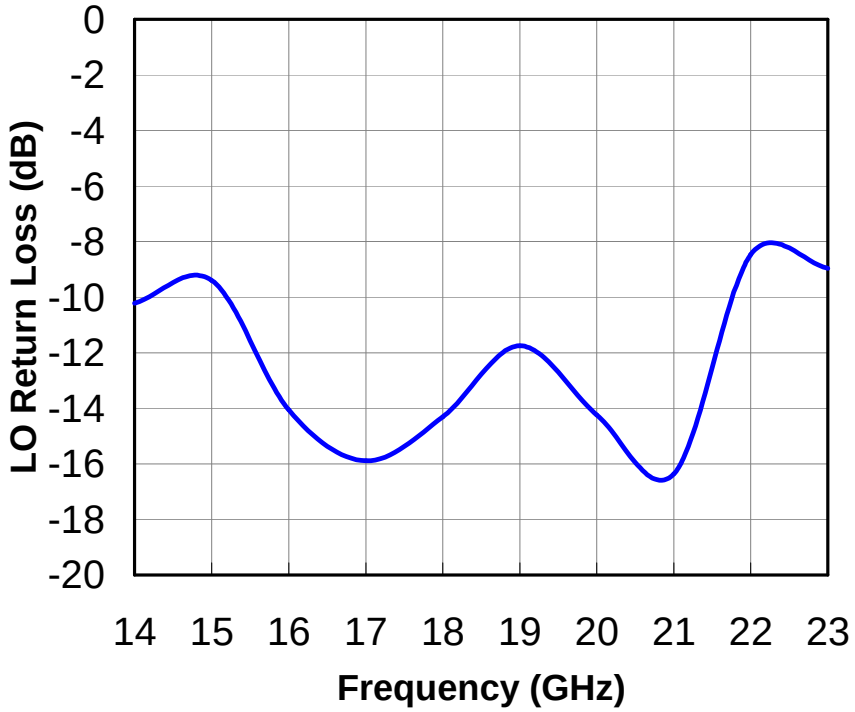
Input IP3 @ Freq_RF= 37.5GHz & 39.5GHz, Freq_IF= 3.5GHz versus VGC at 25°C



LO Return Loss versus frequency



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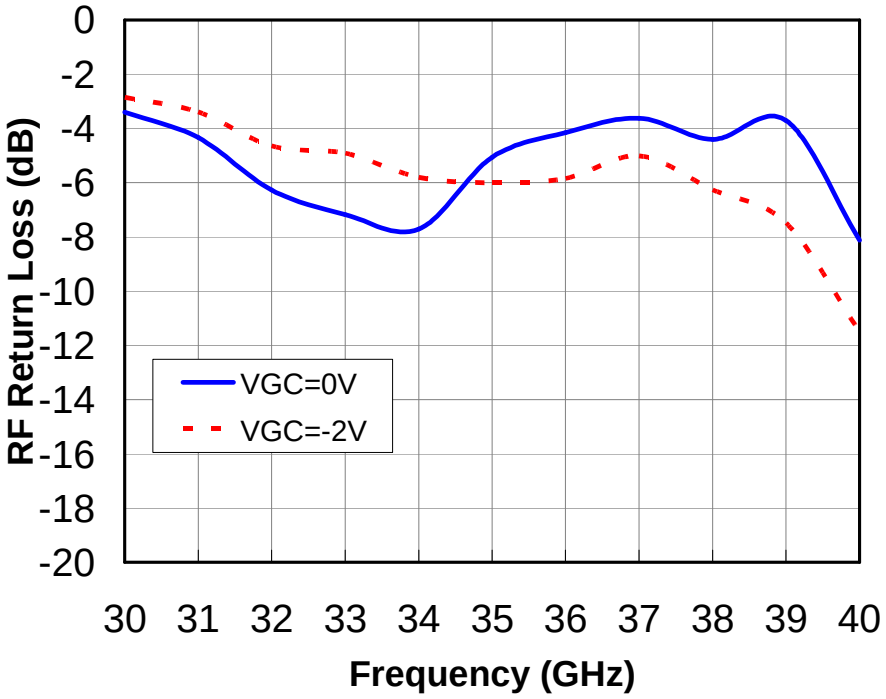
RF Return Loss versus frequency & VGC



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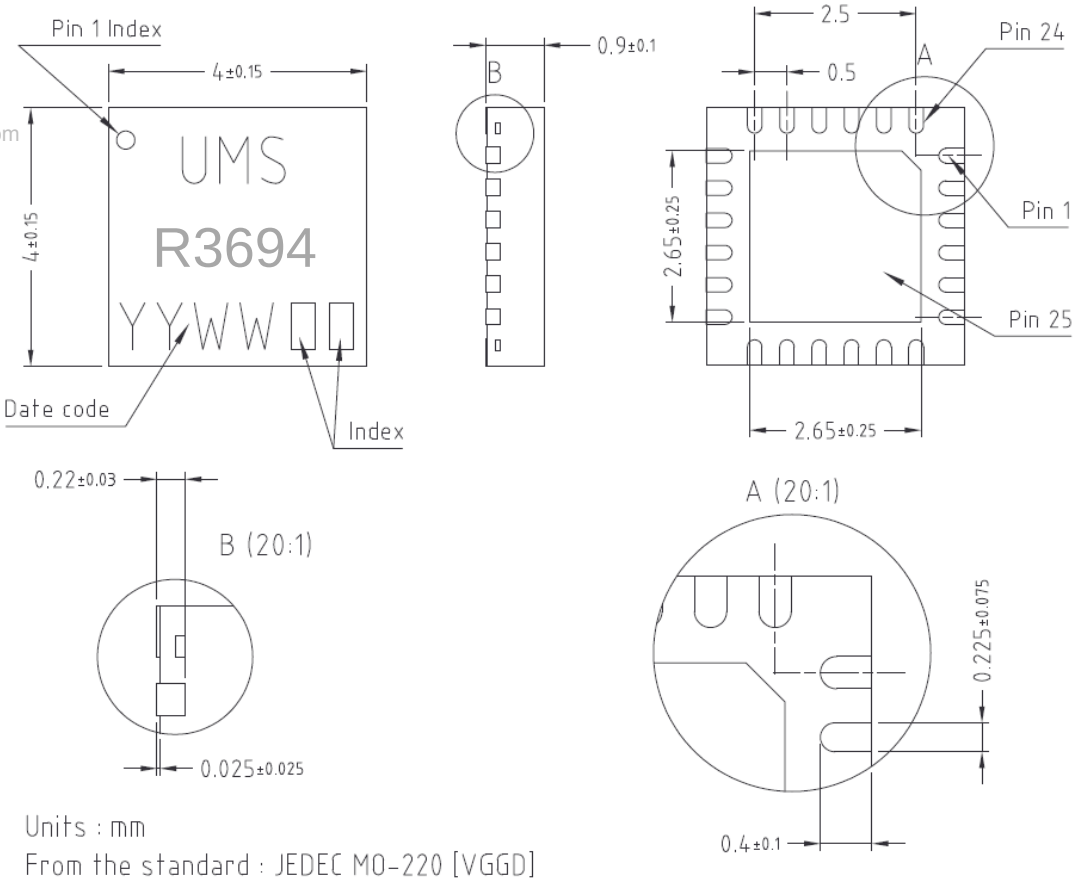
Package outline CHR3694-QDG (1)



Units : mm
From the standard : JEDEC MO-220 [VGGD]
Matt tin, Lead free (Green)

Matt tin, Lead Free	(Green)	1-	Nc	13-	Gnd
Units	mm	2-	Gnd	14-	Gnd
From the standard	JEDEC MO-220	3-	Gnd	15-	RF
	(VGGD)	4-	LO	16-	Gnd
25- GND		5-	Gnd	17-	Gnd
		6-	Gnd	18-	Nc
		7-	Nc	19-	Nc
		8-	VGX	20-	Nc
		9-	VDX	21-	Q
		10-	VGM	22-	Gnd
		11-	VGC	23-	Gnd
		12-	VDL	24-	I

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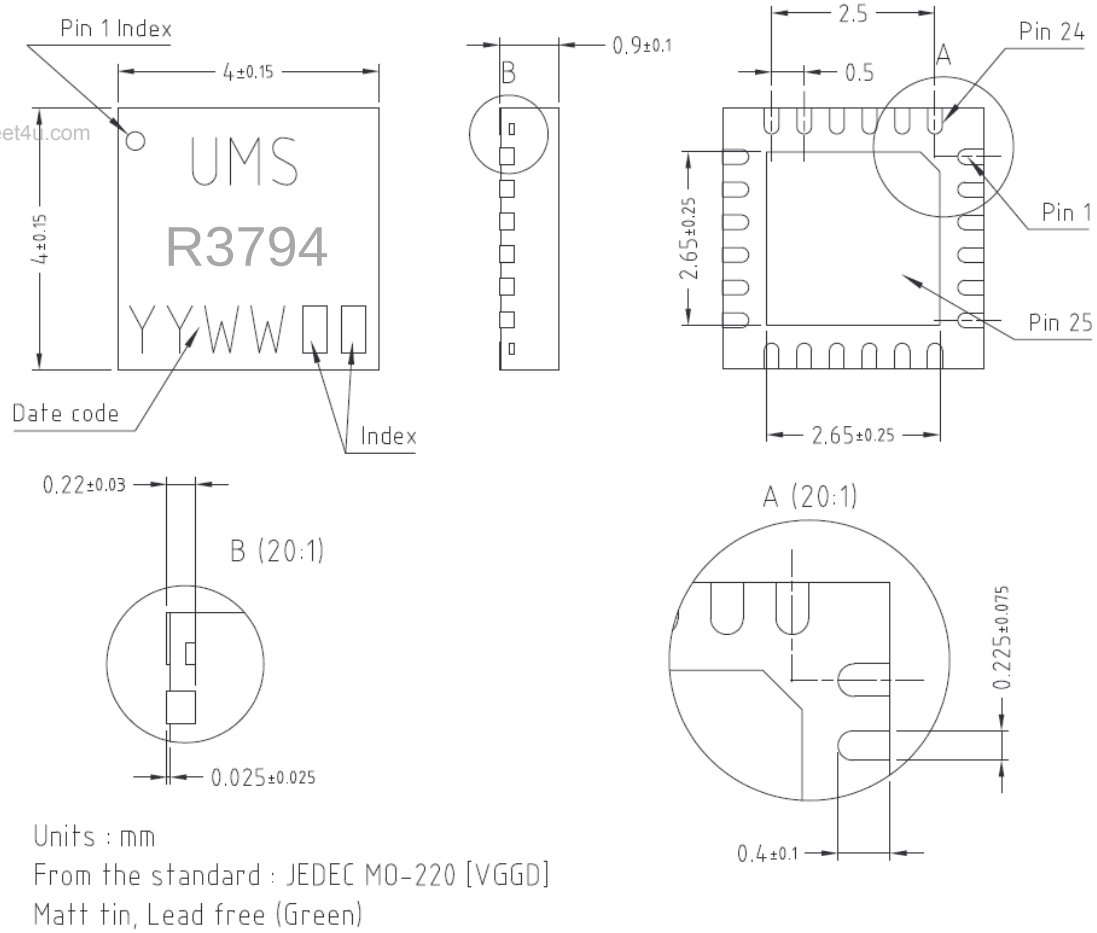
Package outline CHR3794-QDG (1)



Matt tin, Lead Free	(Green)	1-	Nc	13-	Gnd
Units	mm	2-	Gnd	14-	Gnd
From the standard	JEDEC MO-220	3-	Gnd	15-	LO
	(VGGD)	4-	RF	16-	Gnd
25-	GND	5-	Gnd	17-	Gnd
		6-	Gnd	18-	Nc
		7-	VDL	19-	I
		8-	VGC	20-	Gnd
		9-	VGM	21-	Gnd
		10-	VDX	22-	Q
		11-	VGX	23-	Nc
		12-	Nc	24-	Nc

(1)The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 available at http://www.ums-gaas.com for exact package dimensions.

It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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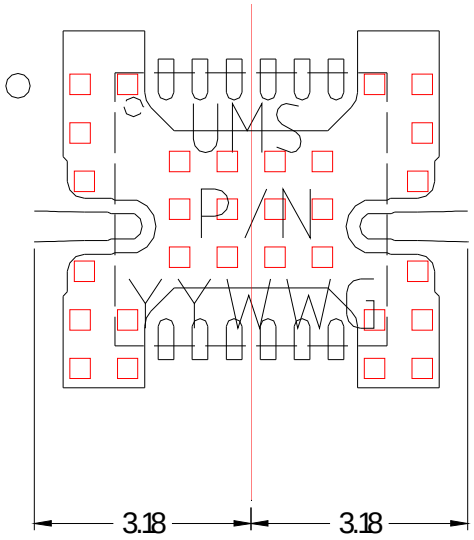
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended at the page 16.



Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

The SMD leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB (motherboard) are given in the drawings above.

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

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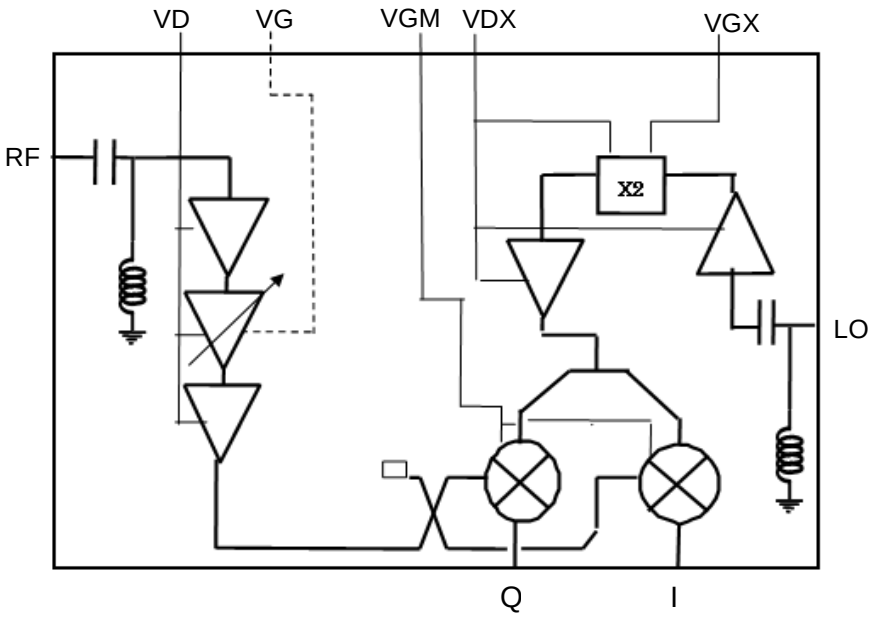
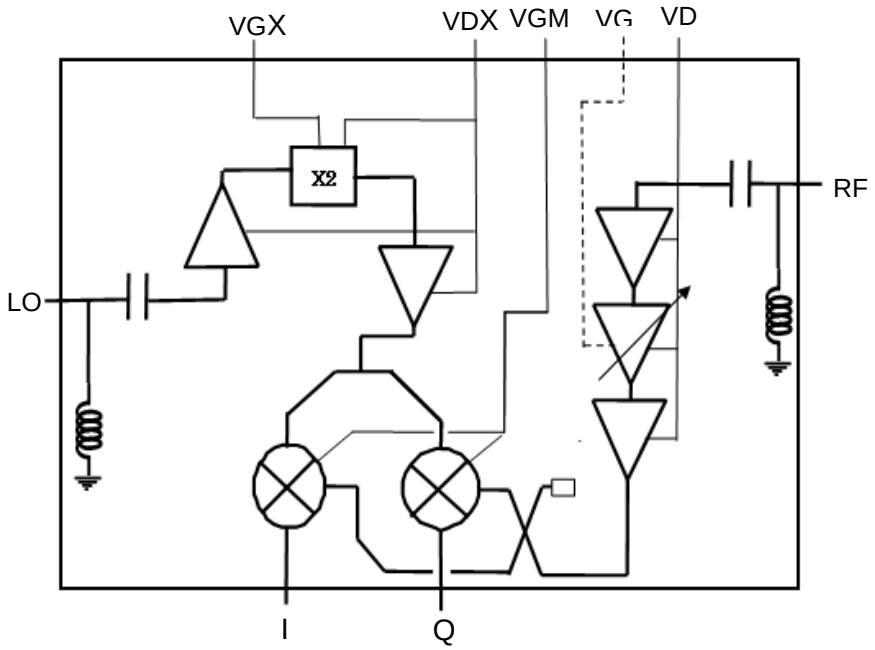
Notes

Due to ESD protection, LO and RF access are DC grounded, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF access. ESD protections are also implemented on each gate access: VGX, VGM and VGC.
Refer to the application note AN0020 available at http://www.ums-gaas.com for general ESD recommendations.

CHR3694-QDG



CHR3794-QDG



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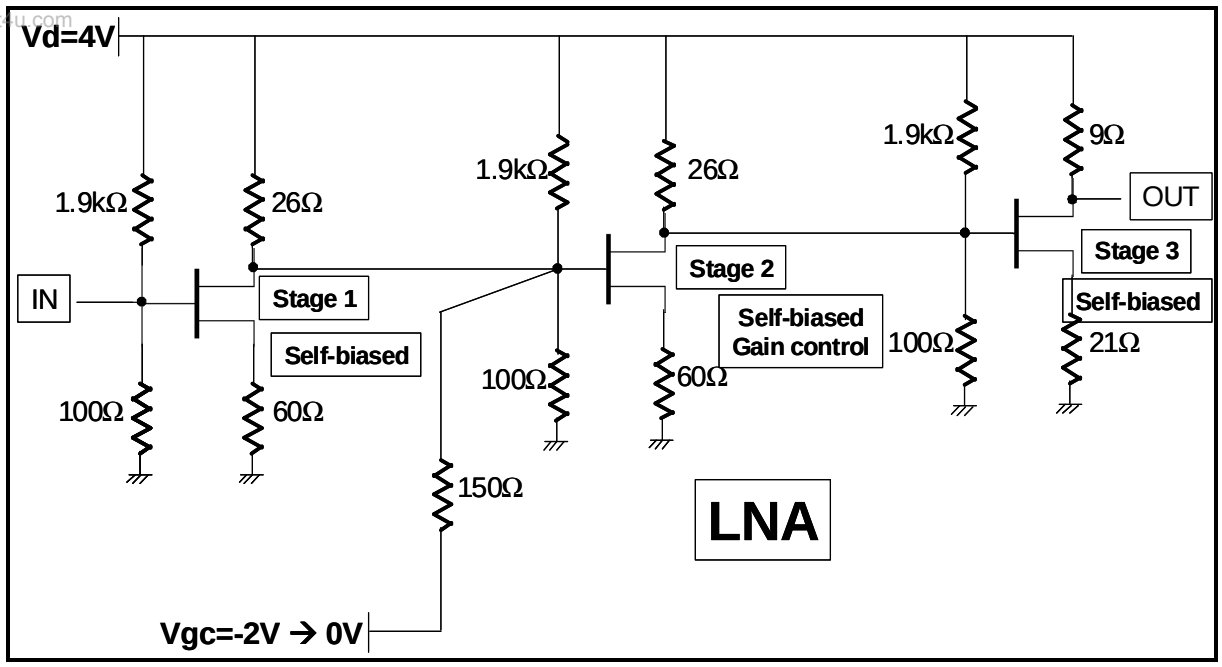
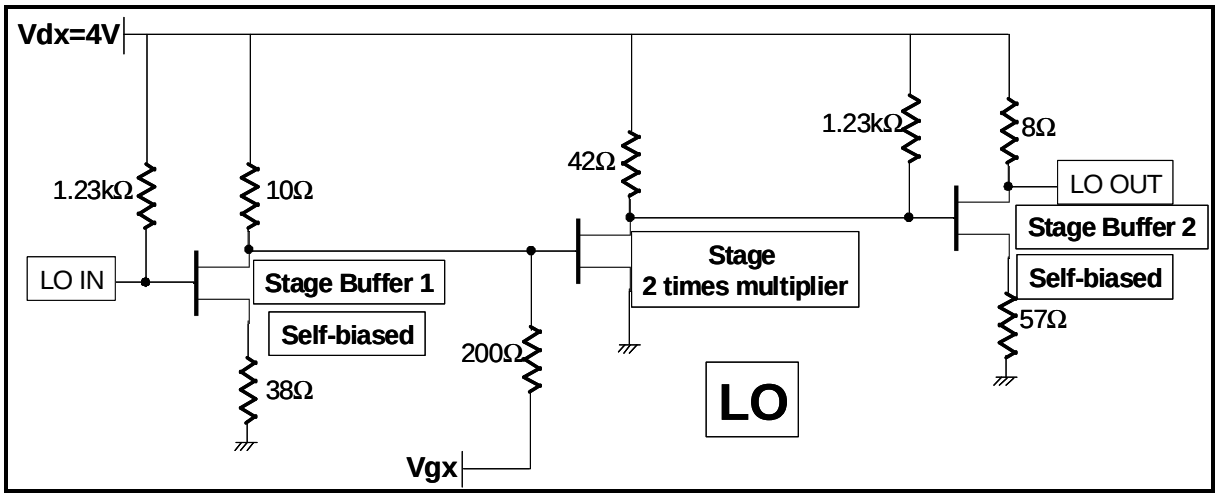
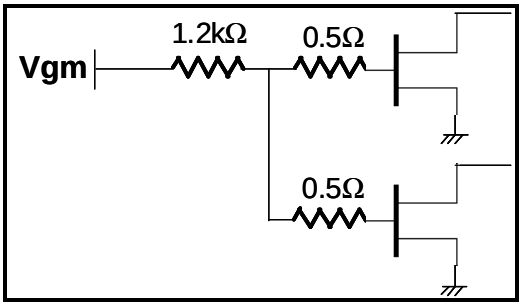
Notes

The biasing circuits of the stages of the circuit are given in the schemes below.







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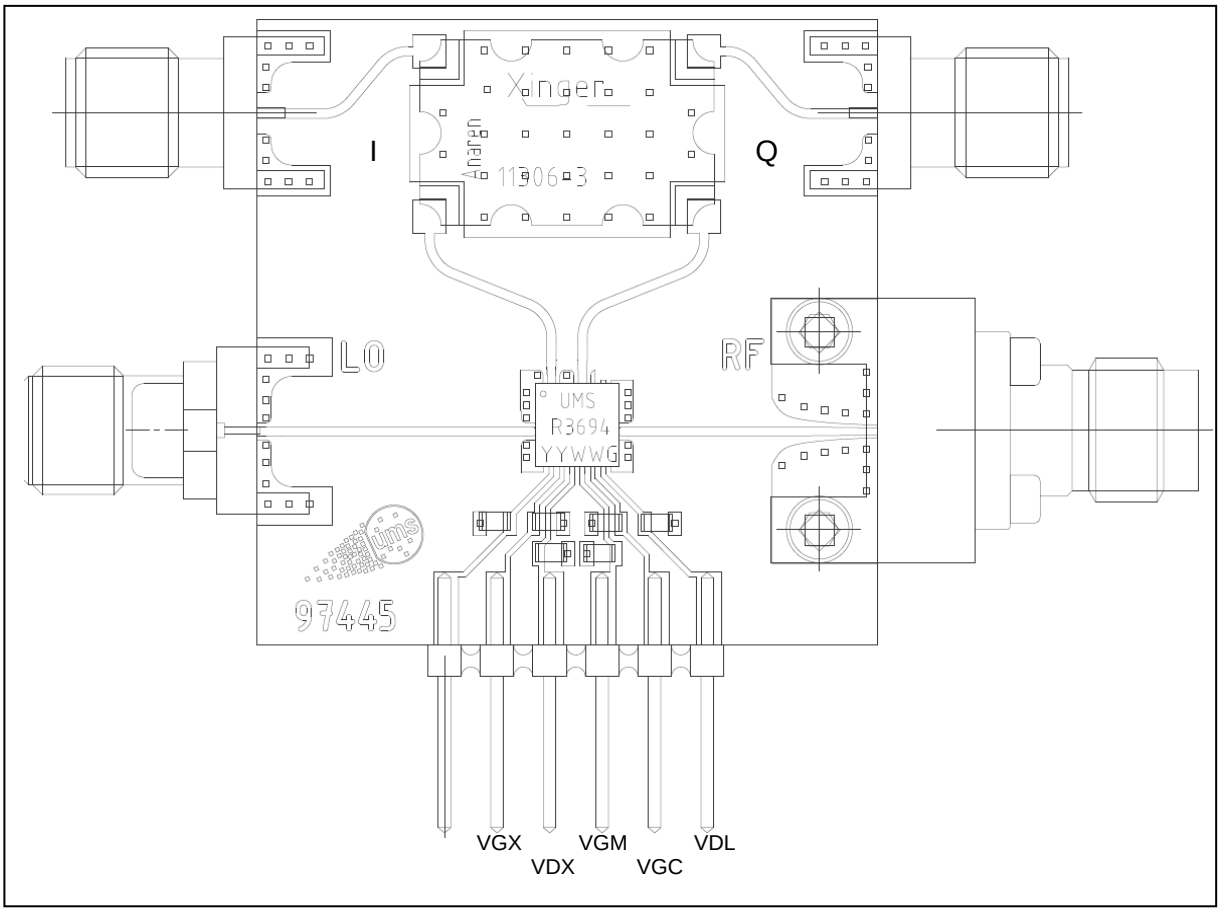
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- Coupleur Anaren 2-4GHz
- (See application note AN0017 for details).

Proposed Assembly board “97445” for CHR3694-QDG 24L-QFN4x4 products characterization



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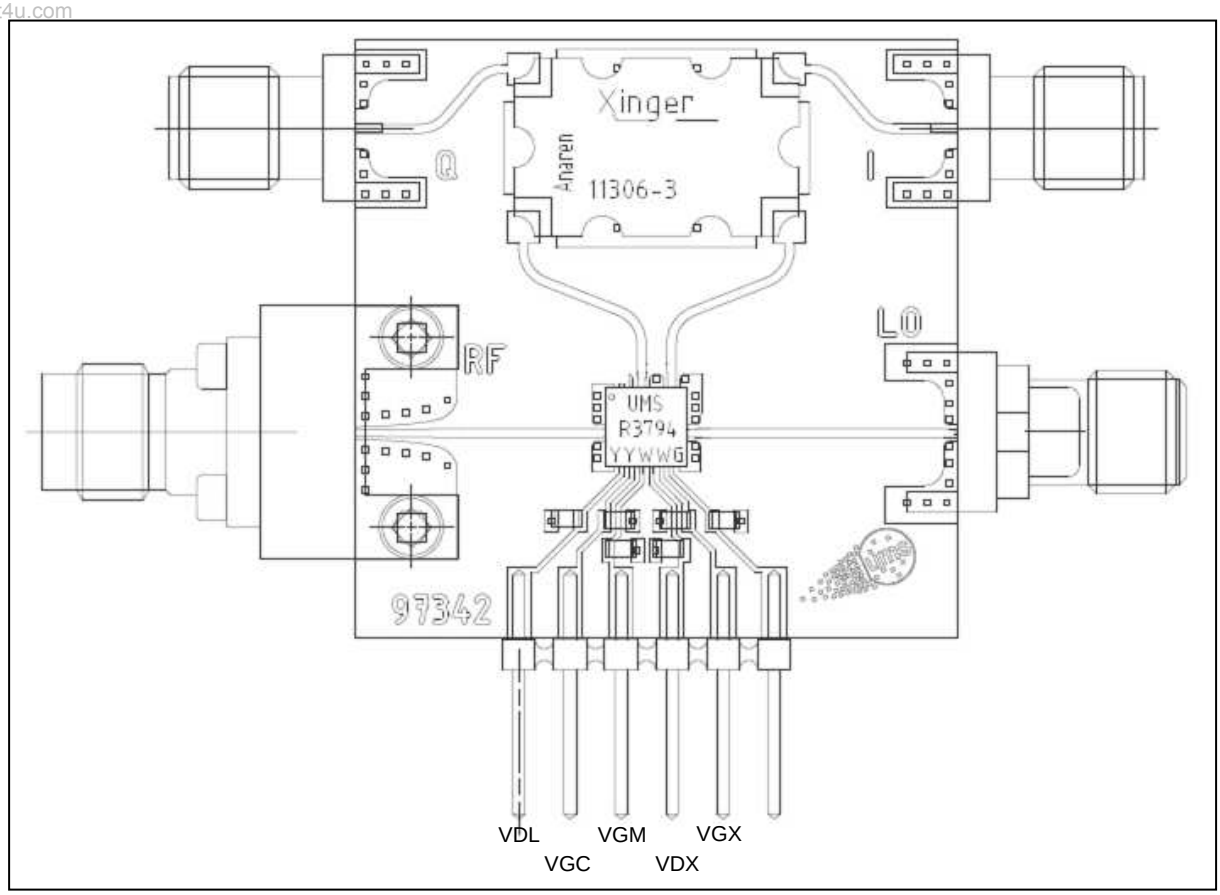
Proposed Assembly board “97342” for CHR3794-QDG 24L-QFN4x4 products characterization



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Ordering Information

QFN 4x4 RoHS compliant package : CHR3694-QDG/XY
Stick: XY = 20 Tape & reel: XY = 21

QFN 4x4 RoHS compliant package : CHR3794-QDG/XY
Stick: XY = 20 Tape & reel: XY = 21

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