Multi-Gigabit Multi-Mode Quad HOTLink-III™ Transceiver

Features

- **Third-generation HOTLink® technology**
- **2488- to 3125-Mbps signaling rate per serial link**
- **XAUI/10G Ethernet compatible mode**
- **InfiniBand™ compatible**
- **Programmable 8-bit or 10-bit SERDES**
- **Selectable 8B/10B encoding/decoding**
- **Ethernet PCS functions using the IEEE802.3z ordered set state machine**
- **Programmable receive framer provides alignment to**
  - **A1/A2: SONET/SDH**
  - **8B/10B COMMA: Ethernet, InfiniBand, XAUI**
- **Synchronous SSTL_2 parallel input/output interface**
- **Internal PLLs with *no* external PLL components**
- **Differential CML serial inputs per channel**
- **Differential CML serial outputs per channel**
  - **Source matched for 50Ω transmission lines**
  - **No external bias resistors required**
- **Compatible with**
  - **Fiber-optic modules**
  - **Copper cables**
  - **Circuit board traces**
- **Diagnostic loop back and line loop back**
- **Signal detect input**
- **Low Power (2.5W typical)**
  - **Single +2.5V V_{DD} supply**
- **256-ball Thermally Enhanced BGA**
- **Commercial temperature range 0°C to +70°C**
- **Industrial temperature range –40°C to +85°C**

Functional Description

The CYP32G0401DX Quad HOTLink-III™ Transceiver is a point-to-point communications building block allowing the transfer of data over high-speed serial links (optical fiber, balanced, and unbalanced copper transmission lines) at signaling speeds ranging from 2488 to 3125 Mbps per serial link.

Each transmit channel accepts parallel characters in an Input Register, encodes each character for transport, and converts it to serial data. Each receive channel accepts serial data and converts it to parallel data, decodes the data into characters, and presents these characters to an output register. *Figure 1* illustrates typical connections between independent host systems and corresponding CYP32G0401DX parts. As a third-generation HOTLink transceiver, the CYP32G0401DX extends the HOTLink family with enhanced levels of integration, multi-gigabit data rates, and multi-mode versatility.

The transmit section of the CYP32G0401DX Quad HOTLink-III shown in *Figure 2* consists of four channels. Each channel can accept either 8-bit data characters or pre-encoded 10-bit transmission characters. Data characters are passed from the Transmit Input Register to an embedded bypassable 8B/10B Encoder to improve their serial transmission characteristics. These encoded characters are then serialized and output from Current Mode Logic (CML) differential transmission-line drivers at a bit-rate which is a multiple of the input reference clock.

The receive section of the CYP32G0401DX Quad HOTLink-III consists of four channels. Each channel accepts a serial bit-stream from a CML differential line receiver and, using a completely integrated PLL Clock Synchronizer, recovers the timing information necessary for data reconstruction. Each recovered bit-stream is deserialized and framed into characters, 8B/10B decoded, and checked for transmission errors. Recovered decoded characters are then written to an internal Elasticity Buffer, and presented to the destination host system. The integrated 8B/10B encoder/decoder may be bypassed for systems that present externally encoded or scrambled data at the parallel interface.

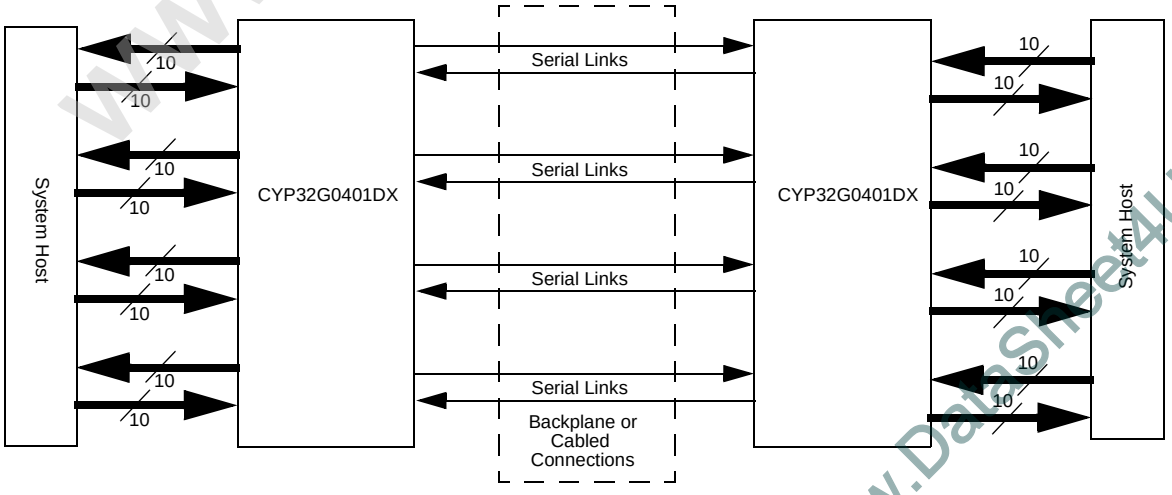


Figure 1. HOTLink-III™ System Connections

The parallel I/O interface may be configured for numerous forms of clocking to provide the highest flexibility in system architecture. The receive interface may be configured to present data relative to a recovered clock (output) or to a local reference clock (input). The CYP32G0401DX is illustrated in greater detail in *Figure 3*.

HOTLink-III devices are ideal for a variety of applications where parallel interfaces can be replaced with high-speed, point-to-point serial links. Some applications include interconnecting workstations, backplanes, servers, mass storage, and video transmission equipment.

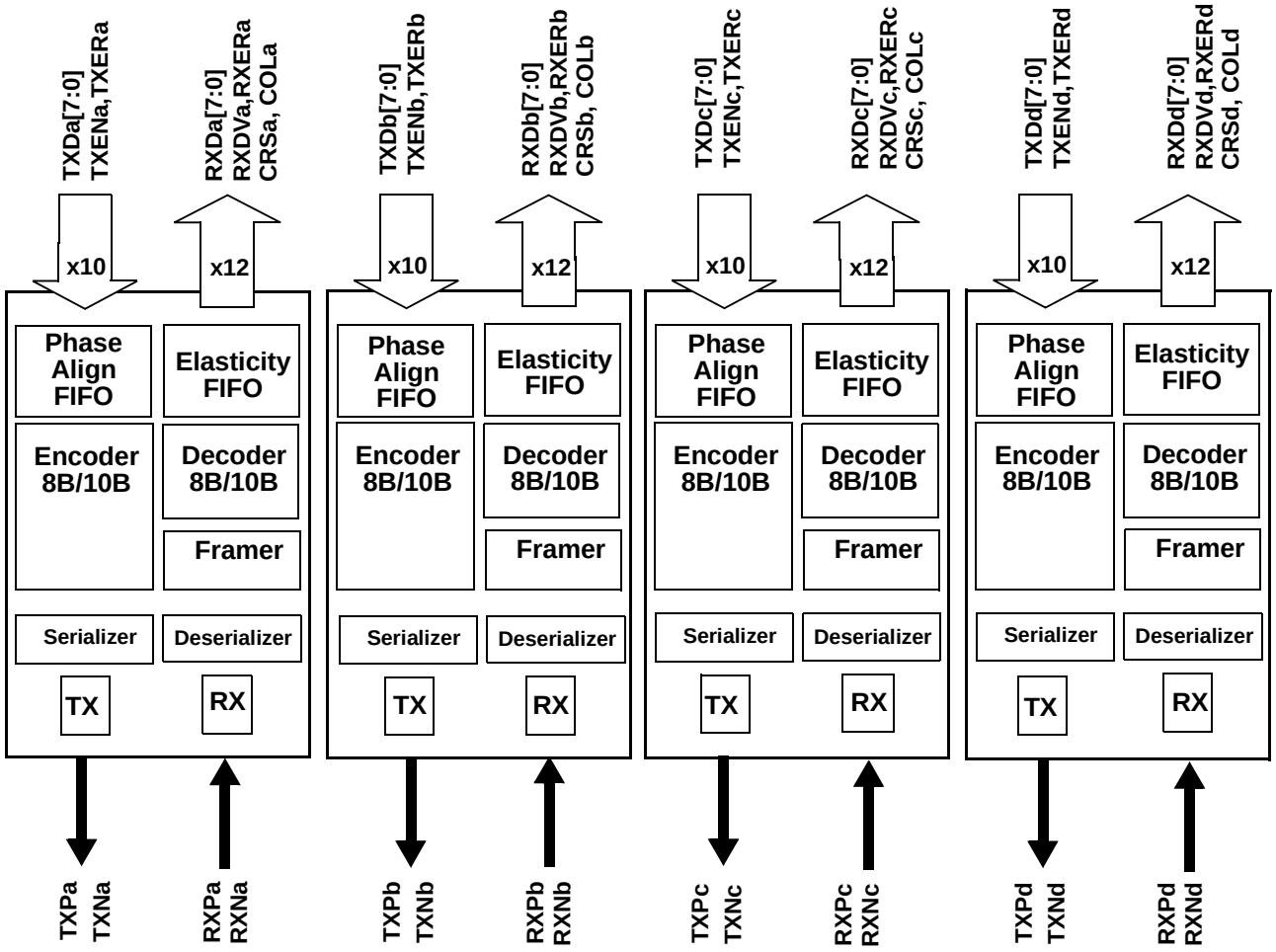


Figure 2. CYP32G0401DX Transceiver Logic Block Diagram

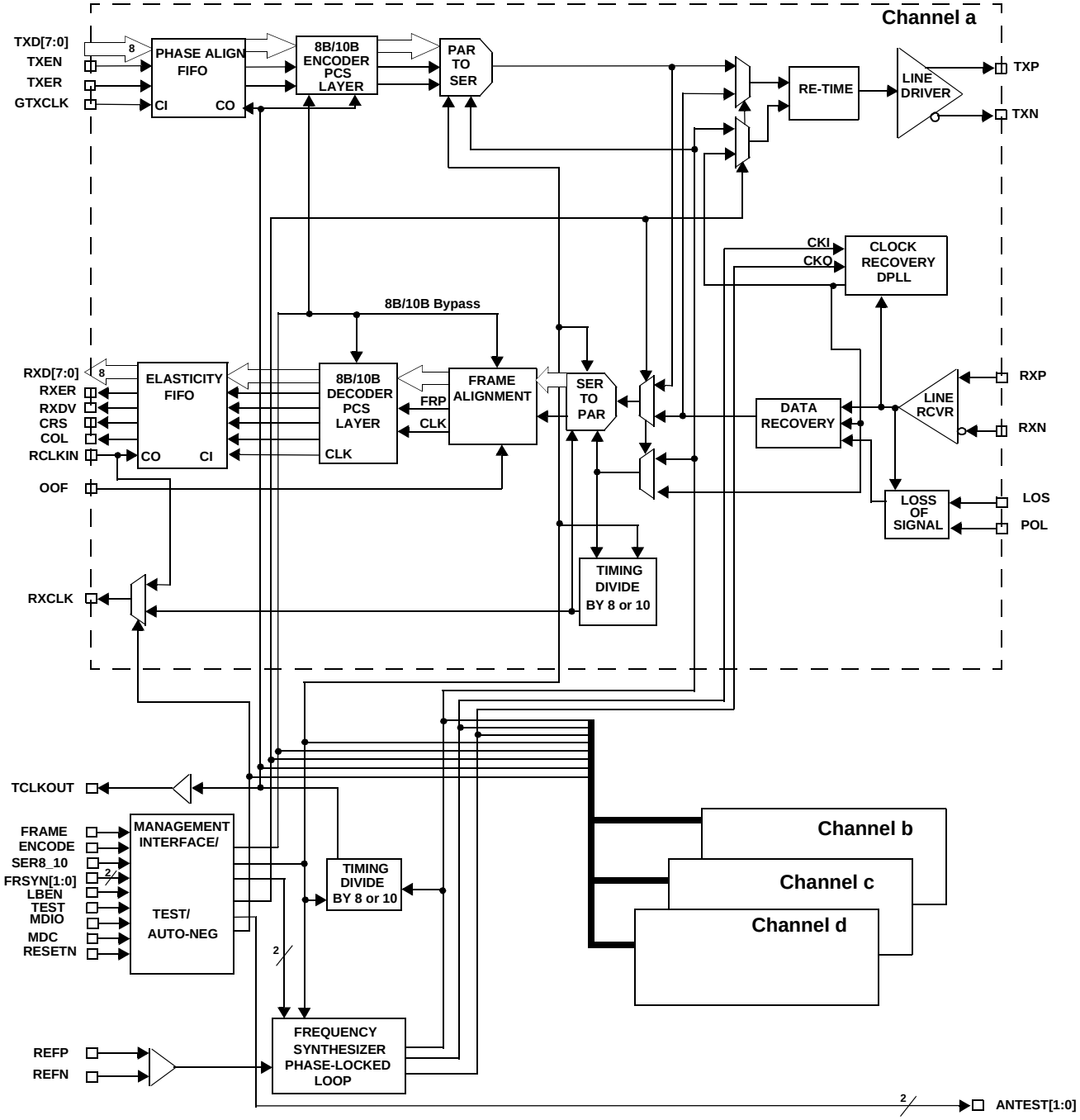


Figure 3. CYP32G0401DX Transceiver Block Diagram

Pin Configuration (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	DGND	DGND	DGND	RCLKINc	RXD2c	RXCLKc	GTXCLKc	TXD5c	DGND	DGND	TCLKOUT	GTXCLKb	DGND	TXD4b	RCLKINb	RXD7b	RXCLKb	DGND	DGND	DGND
B	DGND	DVDD	DVDD	RXD5c	RXD3c	RXD0c	TXD1c	TXD3c	TXD7c	TXENc	VDIGCc	TXD0b	TXD2b	TXD5b	RXDVb	RXD6b	RXD4b	DVDD	DVDD	DGND
C	DGND	DVDD	DVDD	RXD7c	RXD4c	RXD1c	COLc	TXD2c	TXD6c	TXERc	TSYNC	TXD1b	TXD3b	TXD7b	TXENb	RXD5b	RXD3b	DVDD	DVDD	DGND
D	OOFd	RXDVc	RXERc	DVDD	RXD6c	CRSc	DVDD	TXD0c	TXD4c	DVDD	GDIGCc	GDIGCb	TXD6b	DVDD	TXERb	RXERb	DVDD	RXD2b	RXD1b	RXD0b
E	RXCLKd	RXD7d	RXDVd	OOFc													COLb	CRSb	OOFa	RXCLKa
F	RXD4d	RXD5d	RXD6d	RXERd													OOFb	RXDVa	RXERa	RXD7a
G	RCLKINd	RXD2d	RXD3d	GDIGCd													GDIGCa	RXD6a	RXD4a	RXD3a
H	DGND	RXD0d	RXD1d	COLd													RXD5a	RXD2a	CRSa	RCLKINa
J	GTXCLKd	TXD1d	TXD0d	CRSd													RXD1a	RXD0a	COLa	DGND
K	TXD5d	TXD4d	TXD3d	TXD2d													DVDD	TXD0a	GTXCLKa	DGND
L	DGND	TXD7d	TXD6d	VDIGCd													TXD4a	TXD3a	TXD2a	TXD1a
M	DGND	TXENd	DVDD	TXERd													TXENa	TXD7a	TXD6a	TXD5a
N	RESETN	TEST	FRSYN1	FRSYN0													MDIO	TXERa	VDIGCa	DGND
P	ANTEST0	ANTEST1	GTXMc	AVDD													AVDD	VRXMb	MDC	VDIGCb
R	REFP	VTXMc	VRXMc	GTXMd													VTXMb	TRS	TCK	TMS
T	REFN	GRXMc	VTXMd	VRXMd													GRXMa	GTXMb	TDI	TDO
U	GRXMd	ENCODE	FRAME	AVDD	LOSd	GRXDd	AVDD	TXNd	TXPd	GTXDc	VTXDb	TXNa	TXPa	AVDD	GRXDa	GTXMa	AVDD	VRXMa	LBEN	GRXMb
V	AGND	AVDD	AVDD	SER8_10	LOSc	POLd	GRXDc	GTXDd	TXNc	TXPc	TXPb	TXNb	GTXDa	GRXDb	VRXDa	LOSb	POLa	AVDD	AVDD	AGND
W	AGND	AVDD	AVDD	VRXDd	RXNd	RXPd	VTXDd	GFS3	VTXDc	GFS1	VFS2	GTXDb	VTXDa	VRXDb	RXNa	RXPa	VTXMa	AVDD	AVDD	AGND
Y	AGND	AGND	AGND	POLc	VRXDc	RXNc	RXPc	AGND	VFS3	VFS1	AGND	AGND	GFS2	RXNb	RXPb	POLb	LOSa	AGND	AGND	AGND

Pin Configuration (Bottom View)

20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
DGND	DGND	DGND	RXCLKb	RXD7b	RCLKINb	TXD4b	DGND	GTXCLKb	TCLKOUT	DGND	DGND	TXD5c	GTXCLKc	RXCLKc	RXD2c	RCLKINc	DGND	DGND	DGND	A
DGND	DVDD	DVDD	RXD4b	RXD6b	RXDVb	TXD5b	TXD2b	TXD0b	VDIGCc	TXENc	TXD7c	TXD3c	TXD1c	RXD0c	RXD3c	RXD5c	DVDD	DVDD	DGND	B
DGND	DVDD	DVDD	RXD3b	RXD5b	TXENb	TXD7b	TXD3b	TXD1b	TSYNC	TXERc	TXD6c	TXD2c	COLc	RXD1c	RXD4c	RXD7c	DVDD	DVDD	DGND	C
RXD0b	RXD1b	RXD2b	DVDD	RXERb	TXERb	DVDD	TXD6b	GDIGCb	GDIGCc	DVDD	TXD4c	TXD0c	DVDD	CRSc	RXD6c	DVDD	RXERc	RXDVc	OOFd	D
RXCLKa	OOFa	CRSb	COLb													OOFc	RXDVd	RXD7d	RXCLKd	E
RXD7a	RXERa	RXDVa	OOFb													RXERd	RXD6d	RXD5d	RXD4d	F
RXD3a	RXD4a	RXD6a	GDIGCa													GDIGCd	RXD3d	RXD2d	RCLKINd	G
RCLKINa	CRSa	RXD2a	RXD5a													COLd	RXD1d	RXD0d	DGND	H
DGND	COLa	RXD0a	RXD1a													CRSd	TXD0d	TXD1d	GTXCLKd	J
DGND	GTXCLKa	TXD0a	DVDD													TXD2d	TXD3d	TXD4d	TXD5d	K
TXD1a	TXD2a	TXD3a	TXD4a													VDIGCd	TXD6d	TXD7d	DGND	L
TXD5a	TXD6a	TXD7a	TXENa													TXERd	DVDD	TXENd	DGND	M
DGND	VDIGCa	TXERa	MDIO													FRSYN0	FRSYN1	TEST	RESETN	N
VDIGCb	MDC	VRXMb	AVDD													AVDD	GTXMc	ANTEST1	ANTEST0	P
TMS	TCK	TRS	VTXMb													GTXMd	VRXMc	VTXMc	REFP	R
TDO	TDI	GTXMb	GRXMa													VRXMd	VTXMd	GRXMc	REFN	T
GRXMb	LBEN	VRXMa	AVDD	GTXMa	GRXDa	AVDD	TXPa	TXNa	VTXDb	GTXDc	TXPd	TXNd	AVDD	GRXDd	LOSd	AVDD	FRAME	ENCODE	GRXMd	U
AGND	AVDD	AVDD	POLa	LOSb	VRXDa	GRXDb	GTXDa	TXNb	TXPb	TXPc	TXNc	GTXDd	GRXDc	POLd	LOSc	SER8_10	AVDD	AVDD	AGND	V
AGND	AVDD	AVDD	VTXMa	RXPa	RXNa	VRXDb	VTXDa	GTXDb	VFS2	GFS1	VTXDc	GFS3	VTXDd	RXPd	RXNd	VRXDd	AVDD	AVDD	AGND	W
AGND	AGND	AGND	LOSa	POLb	RXPb	RXNb	GFS2	AGND	AGND	VFS1	VFS3	AGND	RXPc	RXNc	VRXDc	POLc	AGND	AGND	AGND	Y

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +100°C

Supply Voltage to Ground Potential..... –0.5V to +3.0V

DC Voltage Applied on Any Pin with Respect to Ground (with V_{DD} in Normal Operating Range)....–0.5V to V_{DD}+0.5V

Static Discharge Voltage.....> 500 V (per JEDEC)

Latch-Up Current.....> 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}
Commercial	0°C to +70°C	+2.5V ±5%
Industrial	–40°C to +85°C	+2.5V ±5%

Pin Descriptions

CYP32G0401DX Transmitter Pins (53)[1]

Pin	Name	Level	I/O	Description
K18, L20 L19, L18 L17, M20 M19, M18	TXD0a, TXD1a TXD2a, TXD3a TXD4a, TXD5a TXD6a, TXD7a	SSTL_2	inputs	Channel a transmit data in. The transmit data TXDa[7:0] are clocked into the Phase Align FIFO on the rising edge of the GTXCLKa signal. The data are read out of the Phase Align FIFO with TCLKOUT. The phase of GTXCLKa may differ from that of TCLKOUT by any amount. In ***MODE 1***[1] the frequency of GTXCLKa may differ from that of TCLKOUT by up to 200 ppm.
M17	TXENa	SSTL_2	input	Channel a transmit enable (TXENa) in ***MODE 1*** Channel a transmit data bit 8 (TXD8a) in ***MODE 2*** Not used in ***MODE 3*** (Suggest user drive to zero) Not used in ***MODE 4*** (Suggest user drive to zero)
N18	TXERa	SSTL_2	input	Channel a transmit error (TXERa) in ***MODE 1*** Channel a transmit data bit 9 (TXD9a) in ***MODE 2*** Channel a transmit code-group select (TXKa) in ***MODE 3*** Not used in ***MODE 4*** (Suggest user drive to zero)
K19	GTXCLKa	SSTL_2	input	Channel a transmit clock. The rising edge of GTXCLKa clocks the input data into the Phase Align FIFO.
U13	TXPa	CML	output	Channel a differential serial data transmit. TXPa is the positive differential output pin of the channel a Line Driver. The TXPa and TXNa look like a differential amplifier with each of the output drains connected to V_{DD} through a 50Ω resistor.
U12	TXNa	CML	output	Channel a differential serial data transmit. TXNa is the negative differential output pin of the channel a Line Driver. The TXPa and TXNa look like a differential amplifier with each of the output drains connected to V_{DD} through a 50Ω resistor.
B12, C12 B13, C13 A14, B14 D13, C14	TXD0b, TXD1b TXD2b, TXD3b TXD4b, TXD5b TXD6b, TXD7b	SSTL_2	inputs	Channel b transmit data in. The transmit data TXDb[7:0] are clocked into the Phase Align FIFO on the rising edge of the GTXCLKb signal. The data are read out of the Phase Align FIFO with TCLKOUT. The phase of GTXCLKb may differ from that of TCLKOUT by any amount. In ***MODE 1*** the frequency of GTXCLKb may differ from that of TCLKOUT by up to 200 ppm.
C15	TXENb	SSTL_2	input	Channel b transmit enable (TXENb) in ***MODE 1*** Channel b transmit data bit 8 (TXD8b) in ***MODE 2*** Not used in ***MODE 3*** (Suggest user drive to zero) Not used in ***MODE 4*** (Suggest user drive to zero)
D15	TXERb	SSTL_2	input	Channel b transmit error (TXERb) in ***MODE 1*** Channel b transmit data bit 9 (TXD9b) in ***MODE 2*** Channel b transmit code-group Select (TXKb) in ***MODE 3*** Not used in ***MODE 4*** (Suggest user drive to zero)
A12	GTXCLKb	SSTL_2	input	Channel b transmit clock. The rising edge of GTXCLKb clocks the input data into the Phase Align FIFO.

Note:
1. Transmitter pins are ***MODE***-dependent where indicated. See *Table 1* for defined ***MODES*** of operation.

Pin Descriptions

CYP32G0401DX Transmitter Pins (53)[1] (continued)

Pin	Name	Level	I/O	Description
V11	TXPb	CML	output	Channel b differential Serial Data Transmit. TXPb is the positive differential output pin of the channel b Line Driver. The TXPb and TXNb look like a differential amplifier with each of the output drains connected to V_{DD} through a 50Ω resistor.
V12	TXNb	CML	output	Channel b differential serial data transmit. TXNb is the negative differential output pin of the channel b Line Driver. The TXPb and TXNb look like a differential amplifier with each of the output drains connected to V_{DD} through a 50Ω resistor.
D8, B7 C8, B8 D9, A8 C9, B9	TXD0c, TXD1c TXD2c, TXD3c TXD4c, TXD5c TXD6c, TXD7c	SSTL_2	inputs	Channel c transmit data in. The transmit data TXDc[7:0] are clocked into the Phase Align FIFO on the rising edge of the GTX-CLKc signal. The data are read out of the Phase Align FIFO with TCLKOUT. The phase of GTXCLKc may differ from that of TCLK-OUT by any amount. In ***MODE 1*** the frequency of GTXCLKc may differ from that of TCLKOUT by up to 200 ppm.
B10	TXENc	SSTL_2	input	Channel c transmit enable (TXENc) in ***MODE 1*** Channel c transmit data bit 8 (TXD8c) in ***MODE 2*** Not used in ***MODE 3*** (Suggest user drive to zero) Not used in ***MODE 4*** (Suggest user drive to zero)
C10	TXERc	SSTL_2	input	Channel c transmit error (TXERc) in ***MODE 1*** Channel c transmit data bit 9 (TXD9c) in ***MODE 2*** Channel c transmit code-group select (TXKc) in ***MODE 3*** Not used in ***MODE 4*** (Suggest user drive to zero)
A7	GTXCLKc	SSTL_2	input	Channel c transmit clock.The rising edge of GTXCLKc clocks the input data into the Phase Align FIFO.
V10	TXPc	CML	output	Channel c differential serial data transmit. TXPc is the positive differential output pin of the channel c Line Driver. The TXPc and TXNc look like a differential amplifier with each of the output drains connected to V_{DD} through a 50Ω resistor.
V9	TXNc	CML	output	Channel c differential serial data transmit. TXNc is the negative differential output pin of the channel c Line Driver. The TXPc and TXNc look like a differential amplifier with each of the output drains connected to V_{DD} through a 50Ω resistor.
J3, J2 K4, K3 K2, K1 L3, L2	TXD0d, TXD1d TXD2d, TXD3d TXD4d, TXD5d TXD6d, TXD7d	SSTL_2	inputs	Channel d transmit data in. The transmit data TXDd[7:0] are clocked into the Phase Align FIFO on the rising edge of the GTX-CLKd signal. The data are read out of the Phase Align FIFO with TCLKOUT. The phase of GTXCLKd may differ from that of TCLKOUT by any amount. In ***MODE 1*** the frequency of GTXCLKd may differ from that of TCLKOUT by up to 200 ppm.
M2	TXENd	SSTL_2	input	Channel d transmit enable (TXENd) in ***MODE 1*** Channel d transmit data bit 8 (TXD8d) in ***MODE 2*** Not used in ***MODE 3*** (Suggest user drive to zero) Not used in ***MODE 4*** (Suggest user drive to zero)
M4	TXERd	SSTL_2	input	Channel d transmit error (TXERd) in ***MODE 1*** Channel d transmit data bit 9 (TXD9d) in ***MODE 2*** Channel d transmit code-group select (TXKd) in ***MODE 3*** Not used in ***MODE 4*** (Suggest user drive to zero)
J1	GTXCLKd	SSTL_2	input	Channel d transmit clock. The rising edge of GTXCLKd clocks the input data into the Phase Align FIFO.
U9	TXPd	CML	output	Channel d differential serial data transmit. TXPd is the positive differential output pin of the channel d Line Driver. The TXPd and TXNd look like a differential amplifier with each of the output drains connected to V_{DD} through a 50Ω resistor.

Pin Descriptions

CYP32G0401DX Transmitter Pins (53)[1] (continued)

Pin	Name	Level	I/O	Description
U8	TXNd	CML	output	Channel d differential serial data transmit. TXNd is the negative differential output pin of the channel d Line Driver. The TXPd and TXNd look like a differential amplifier with each of the output drains connected to V_{DD} through a 50Ω resistor.
A11	TCLKOUT	SSTL_2	output	Reference transmit clock output. TCLKOUT is the word clock signal used to clock data out of the Transmit Phase Align FIFOs of all four channels. TCLKOUT is derived directly from the Frequency Synthesizer output.

CYP32G0401DX Receiver Pins (76)[2]

Pin	Name	Level	I/O	Description
J18, J17 H18, G20 G19, H17 G18, F20	RXD0a, RXD1a RXD2a, RXD3a RXD4a, RXD5a RXD6a, RXD7a	SSTL_2	outputs	Channel a receive data. The receive data RXDa[7:0] are clocked out of the Elasticity FIFO by RCLKINa.
F19	RXERa	SSTL_2	output	Channel a receive error (RXERa) in ***MODE 1***[2] Channel a receive data bit9 (RXD9a) in ***MODE 2*** Channel a receive invalid character flag (ERRa) in ***MODE 3*** Not used in ***MODE 4***
F18	RXDVa	SSTL_2	output	Channel a receive data valid (RXDVa) in ***MODE 1*** Channel a receive data bit8 (RXD8a) in ***MODE 2*** Channel a receive code-group select (RXKa) in ***MODE 3*** Not used in ***MODE 4***
H19	CRSa	SSTL_2	output	Channel a receive carrier sense indicate (CRSa) in ***MODE 1*** Not used in ***MODE 2*** Channel a receive idle code (IDLEa) in ***MODE 3*** Channel a receive frame pulse flag (FRPa) in ***MODE 4***
J19	COLa	SSTL_2	output	Channel a receive collision indicate (COLa) in ***MODE 1*** Not used in ***MODE 2*** Channel a receive invalid character flag (ERRa) in ***MODE 3*** Not used in ***MODE 4***
E20	RXCLKa	SSTL_2	output	Channel a receive clock output reference. The RXCLKa pin outputs either a buffered RCLKINa, or the recovered clock. This is determined by the status of LBEN on the rising edge of RESETN as follows: LBEN = 0 selects the buffered RCLKINa; LBEN = 1 selects the recovered clock.
E19	OOFa	SSTL_2	input	Not used in ***MODE 1*** Not used in ***MODE 2*** Not used in ***MODE 3*** Channel a OOF indicate in ***MODE 4***
H20	RCLKINa	SSTL_2	input	Channel a receive Elasticity FIFO output clock. RCLKINa clocks the receive data RXDa[7:0], RXDVa, and RXERa out of the channel a Elasticity FIFO.
W16	RXPa	CML	input	Channel a serial receive data, ext. ac coupled, int. bias. RXPa is the positive differential input pin of the channel a Line Receiver. The RXPa and RXNa look like a differential amplifier with each of the input pins connected to $V_{DD}/2$ through a 150Ω resistor. When inputs are differentially terminated with a 150Ω resistor, the line termination is nominally 100Ω. See *Figure 6*.

Note:
2. Receiver pins are ***MODE***-dependent where indicated. See *Table 1* for defined ***MODES*** of operation.

CYP32G0401DX Receiver Pins (76)[2] (continued)

Pin	Name	Level	I/O	Description
W15	RXNa	CML	input	Channel a serial receive data, ext. ac coupled, int. bias. RXNa is the negative differential input pin of the channel a Line Receiver. The RXPa and RXNa look like a differential amplifier with each of the input pins connected to V_{DD}/2 through a 150Ω resistor. When inputs are differentially terminated with a 150Ω resistor, the line termination is nominally 100Ω. See *Figure 6*.
Y17	LOSa	LVPECL	input	Channel a receive loss of signal indicate. The signal input on the LOSa pin may come from a fiber module and indicates if there is a Loss of Signal (LOS) condition. If a LOS condition occurs, the data input is squelched and no data is sent to the data recovery block. When no data edges are present at the inputs to the clock recovery Digital Phase-Locked Loop (DPLL), its output frequency will be locked to the frequency of the transmit Frequency Synthesizer. The polarity of the LOSa signal is controlled by the POLa pin as shown in *Table 4*.
V17	POLa	SSTL_2	input	Channel a receive loss of signal polarity. The POLa pin controls the polarity of the LOSa signal as shown in *Table 4*.
D20, D19 D18, C17 B17, C16 B16, A16	RXD0b, RXD1b RXD2b, RXD3b RXD4b, RXD5b RXD6b, RXD7b	SSTL_2	outputs	Channel b receive data. The receive data RXDb[7:0] are clocked out of the Elasticity FIFO by RCLKINb.
D16	RXERb	SSTL_2	output	Channel b receive error (RXERb) in ***MODE 1*** Channel b receive data bit9 (RXD9b) in ***MODE 2*** Channel b receive invalid character flag (ERRb) in ***MODE 3*** Not used in ***MODE 4***
B15	RXDVb	SSTL_2	output	Channel b receive data valid (RXDVb) in ***MODE 1*** Channel b receive data bit8 (RXD8b) in ***MODE 2*** Channel B receive code-group select (RXKb) in ***MODE 3*** Not used in ***MODE 4***
E18	CRSb	SSTL_2	output	Channel b receive carrier sense indicate (CRSb) in ***MODE 1*** Not used in ***MODE 2*** Channel b receive idle code (IDLEb) in ***MODE 3*** Channel b receive frame pulse flag (FRPb) in ***MODE 4***
E17	COLb	SSTL_2	output	Channel b receive collision indicate (COLb) in ***MODE 1*** Not used in ***MODE 2*** Channel b receive invalid character flag (ERRb) in ***MODE 3*** Not used in ***MODE 4***
A17	RXCLKb	SSTL_2	output	Channel b receive clock output reference. The RXCLKb pin outputs either a buffered RCLKINb, or the recovered clock. This is determined by the status of LBEN on the rising edge of RESETN as follows: LBEN = 0 selects the buffered RCLKINb; LBEN = 1 selects the recovered clock.
F17	OOFb	SSTL_2	input	Not used in ***MODE 1*** Not used in ***MODE 2*** Not used in ***MODE 3*** Channel b OOF indicate in ***MODE 4***
A15	RCLKINb	SSTL_2	input	Channel b receive Elasticity FIFO output clock. RCLKINb clocks the receive data RXDb[7:0], RXDVb, and RXERb out of the channel b Elasticity FIFO.
Y15	RXPb	CML	input	Channel b serial receive data, ext. ac coupled, int. bias. RXPb is the positive differential input pin of the channel b Line Receiver. The RXPb and RXNb look like a differential amplifier with each of the input pins connected to V_{DD}/2 through a 150Ω resistor. When inputs are differentially terminated with a 150Ω resistor, the line termination is nominally 100Ω. See *Figure 6*.

CYP32G0401DX Receiver Pins (76)[2] (continued)

Pin	Name	Level	I/O	Description
Y14	RXNb	CML	input	Channel b serial receive data, ext. ac coupled, int. bias. RXNb is the negative differential input pin of the channel b Line Receiver. The RXPb and RXNb look like a differential amplifier with each of the input pins connected to V_{DD}/2 through a 150Ω resistor. When inputs are differentially terminated with a 150Ω resistor, the line termination is nominally 100Ω. See *Figure 6*.
V16	LOSb	LVPECL	input	Channel b receive loss of signal indicate. The signal input on the LOSb pin may come from a fiber module and indicates if there is a Loss of Signal (LOS) condition. If a LOS condition occurs, the data input is squelched and no data is sent to the data recovery block. When no data edges are present at the inputs to the clock recovery Digital Phase-Locked Loop (DPLL), its output frequency will be locked to the frequency of the transmit Frequency Synthesizer. The polarity of the LOSb signal is controlled by the POLb pin as shown in *Table 4*.
Y16	POLb	SSTL_2	input	Channel b receive loss of signal polarity. The POLb pin controls the polarity of the LOSb signal as shown in *Table 4*.
B6, C6 A5, B5 C5, B4 D5, C4	RXD0c, RXD1c RXD2c, RXD3c RXD4c, RXD5c RXD6c, RXD7c	SSTL_2	outputs	Channel c receive data. The receive data RXDc[7:0] are clocked out of the Elasticity FIFO by RCLKINc.
D3	RXERc	SSTL_2	output	Channel c receive error (RXERc) in ***MODE 1*** Channel c receive data bit9 (RXD9c) in ***MODE 2*** Channel c receive invalid character flag (ERRc) in ***MODE 3*** Not used in ***MODE 4***
D2	RXDVc	SSTL_2	output	Channel c receive data valid (RXDVc) in ***MODE 1*** Channel c receive data bit8 (RXD8c) in ***MODE 2*** Channel c receive code-group select (RXKc) in ***MODE 3*** Not used in ***MODE 4***
D6	CRSc	SSTL_2	output	Channel c receive carrier sense indicate (CRSc) in ***MODE 1*** Not used in ***MODE 2*** Channel c receive idle code (IDLEc) in ***MODE 3*** Channel c receive frame pulse flag (FRPc) in ***MODE 4***
C7	COLc	SSTL_2	output	Channel c receive collision indicate (COLc) in ***MODE 1*** Not used in ***MODE 2*** Channel c receive invalid character flag (ERRc) in ***MODE 3*** Not used in ***MODE 4***
A6	RXCLKc	SSTL_2	output	Channel c receive clock output reference. The RXCLKc pin outputs either a buffered RCLKINc, or the recovered clock. This is determined by the status of LBEN on the rising edge of RESETN as follows: LBEN = 0 selects the buffered RCLKINc; LBEN = 1 selects the recovered clock.
E4	OOFc	SSTL_2	input	Not used in ***MODE 1*** Not used in ***MODE 2*** Not used in ***MODE 3*** Channel c OOF indicate in ***MODE 4***
A4	RCLKINc	SSTL_2	input	Channel c receive Elasticity FIFO output clock. RCLKINc clocks the receive data RXDc[7:0], RXDVc, and RXERc out of the channel c Elasticity FIFO.
Y7	RXPc	CML	input	Channel c serial receive data, ext. ac coupled, int. bias. RXPc is the positive differential input pin of the channel c Line Receiver. The RXPc and RXNc look like a differential amplifier with each of the input pins connected to V_{DD}/2 through a 150Ω resistor. When inputs are differentially terminated with a 150Ω resistor, the line termination is nominally 100Ω. See *Figure 6*.

CYP32G0401DX Receiver Pins (76)[2] (continued)

Pin	Name	Level	I/O	Description
Y6	RXNc	CML	input	Channel c serial receive data, ext. ac coupled, int. bias. RXNc is the negative differential input pin of the channel c Line Receiver. The RXPc and RXNc look like a differential amplifier with each of the input pins connected to V_{DD}/2 through a 150Ω resistor. When inputs are differentially terminated with a 150Ω resistor, the line termination is nominally 100Ω. See *Figure 6*.
V5	LOSc	LVPECL	input	Channel c receive loss of signal indicate. The signal input on the LOSc pin may come from a fiber module and indicates if there is a Loss of Signal (LOS) condition. If a LOS condition occurs, the data input is squelched and no data is sent to the data recovery block. When no data edges are present at the inputs to the clock recovery Digital Phase-Locked Loop (DPLL), its output frequency will be locked to the frequency of the transmit Frequency Synthesizer. The polarity of the LOSc signal is controlled by the POLc pin as shown in *Table 4*.
Y4	POLc	SSTL_2	input	Channel c receive loss of signal polarity. The POLc pin controls the polarity of the LOSc signal as shown in *Table 4*.
H2, H3 G2, G3 F1, F2 F3, E2	RXD0d, RXD1d RXD2d, RXD3d RXD4d, RXD5d RXD6d, RXD7d	SSTL_2	outputs	Channel d receive data. The receive data RXDd[7:0] are clocked out of the Elasticity FIFO by RCLKINd.
F4	RXERd	SSTL_2	output	Channel d receive error (RXERd) in ***MODE 1*** Channel d receive data bit9 (RXD9d) in ***MODE 2*** Channel d receive invalid character flag (ERRd) in ***MODE 3*** Not used in ***MODE 4***
E3	RXDVd	SSTL_2	output	Channel d receive data valid (RXDVd) in ***MODE 1*** Channel d receive data bit8 (RXD8d) in ***MODE 2*** Channel d receive code-group select (RXKd) in ***MODE 3*** Not used in ***MODE 4***
J4	CRSd	SSTL_2	output	Channel d receive carrier sense indicate (CRSd) in ***MODE 1*** Not used in ***MODE 2*** Channel d receive idle code (IDLEd) in ***MODE 3*** Channel d receive frame pulse flag (FRPd) in ***MODE 4***
H4	COLd	SSTL_2	output	Channel d receive collision indicate (COLd) in ***MODE 1*** Not used in ***MODE 2*** Channel d receive invalid character flag (ERRd) in ***MODE 3*** Not used in ***MODE 4***
E1	RXCLKd	SSTL_2	output	Channel d receive clock output reference. The RXCLKd pin outputs either a buffered RCLKINd, or the recovered clock. This is determined by the status of LBEN on the rising edge of RESETN as follows: LBEN = 0 selects the buffered RCLKINd; LBEN = 1 selects the recovered clock.
D1	OOFd	SSTL_2	input	Not used in ***MODE 1*** Not used in ***MODE 2*** Not used in ***MODE 3*** Channel d OOF indicate in ***MODE 4***
G1	RCLKINd	SSTL_2	input	Channel d receive Elasticity FIFO output clock. RCLKINd clocks the receive data RXDd[7:0], RXDVd, and RXERd out of the channel d Elasticity FIFO.
W6	RXPd	CML	input	Channel d serial receive data, ext. ac coupled, int. bias. RXPd is the positive differential input pin of the channel d Line Receiver. The RXPd and RXNd look like a differential amplifier with each of the input pins connected to V_{DD}/2 through a 150Ω resistor. When inputs are differentially terminated with a 150Ω resistor, the line termination is nominally 100Ω. See *Figure 6*.

CYP32G0401DX Receiver Pins (76)[2] (continued)

Pin	Name	Level	I/O	Description
W5	RXNd	CML	input	Channel d serial receive data, ext. ac coupled, int. bias. RXNd is the negative differential input pin of the channel d Line Receiver. The RXPd and RXNd look like a differential amplifier with each of the input pins connected to V_{DD}/2 through a 150Ω resistor. When inputs are differentially terminated with a 150Ω resistor, the line termination is nominally 100Ω. See *Figure 6*.
U5	LOSd	LVPECL	input	Channel d receive loss of signal indicate. The signal input on the LOSd pin may come from a fiber module and indicates if there is a Loss of Signal (LOS) condition. If a LOS condition occurs, the data input is squelched and no data is sent to the data recovery block. When no data edges are present at the inputs to the clock recovery Digital Phase-Locked Loop (DPLL), its output frequency will be locked to the frequency of the transmit Frequency Synthesizer. The polarity of the LOSd signal is controlled by the POLd pin as shown in *Table 4*.
V6	POLd	SSTL_2	input	Channel d receive loss of signal polarity. The POLd pin controls the polarity of the LOSd signal as shown in *Table 4*.

CYP32G0401DX Control pins (11)[3]

Pin	Name	Level	I/O	Description
N1	RESETN	SSTL_2	Bidir	Chip global reset (active LOW bidirectional pull down). The RESETN pin reflects the operation of the Power On Reset (POR) circuit. When POR is active, RESETN is driven LOW. When POR is inactive, RESETN is three-stated and an internal pull-up resistor (approximately 50 kΩ) establishes the inactive (HIGH) state. The RESETN pin may also be driven from an external device in order to re-initialize the chip regardless of the internal operating state and regardless of the state of POR. In this case RESETN must be driven LOW for a minimum of two cycles of the reference clock (REFP, REFN), though no other timing relationship between RESETN and the reference clock need exist.
P19	MDC	SSTL_2	input	Management Interface Data Clock
N17	MDIO	SSTL_2	Bidir	Management Interface Data Input/Output
N4 N3	FRSYN0 FRSYN1	SSTL_2	input	Frequency Synthesizer PLL ratio select. The FRSYN0 and FRSYN1 pins, together with the SER8_10 pin, select from the allowable reference clock frequency ranges for input to the frequency synthesizer. See *Table 2*.
V4	SER8_10	SSTL_2	input	8-bit (SER8_10 = 1), 10-bit (SER8_10 = 0) data select.[3] The parallel-to-serial and serial-to-parallel converters operate in two modes, eight-bit and ten-bit, under the control of the SER8_10 pin, as shown in*Table 3*. The 8-bit/10-bit selection made using the SER8_10 pin will also affect the choice of reference clock frequency range made using the FRSYN0 and FRSYN1 pins, as shown in *Table 2*.
U2	ENCODE	SSTL_2	input	Encode select.[3] The 8B/10B encode and decode functions are enabled when ENCODE = 1. The encoder translates the 8-bit input byte to a 10-bit symbol for transmit, and the decoder translates the received 10-bit symbol to the 8-bit byte originally encoded at the other end. Both encode and decode functions are bypassed when ENCODE = 0.

Note:
3. The control pins SER8_10, ENCODE and FRAME together select the operating ***MODE***. See *Table 1* for defined operating ***MODES***.

CYP32G0401DX Control pins (11)[3] (continued)

Pin	Name	Level	I/O	Description
U3	FRAME	SSTL_2	input	Frame select.[3] The Ethernet PCS functions are enabled when FRAME=1. This performs Ethernet PCS functions using the IEEE802.3z ordered set state machine (Section 36.2.5.2.1 and Figures 36-5 and 36-6) during transmit, and the receive and synchronization state machines (Section 36.2.5.2.2 and Figures 36-7a, 36-7b, 36-8, and 36-9) during receive.
U19	LBEN	SSTL_2	input	Loop back enable. When loop back is enabled (LBEN = 1) both the high-speed line side data and the byte input data are looped back. The parallel input data (TXD[7:0], TXEN, TXER) are looped back to the receive side parallel data (RXD[7:0], RXDV, RXER), and the line-received data (RXP and RXN) are looped back and sent to the line driver (TXP and TXN). In ***MODE 1*** the transmit driver (TXP, TXN) is disabled, as required in IEEE802.3 Section 22.2.4.1.2. **Note**: LBEN is logically ORed with bit 0.14 of the control register.
R1	REFP	CML	input	Differential Frequency Synthesizer clock input, externally ac coupled, internally biased. REFP is the positive differential input pin for the reference clock (REFCLK) used by the frequency synthesizer. The REFP and REFN look like a differential amplifier with each of the input pins connected to $0.75xV_{DD}$ through a 150Ω resistor. See *Table 7*.
T1	REFN	CML	input	Differential Frequency Synthesizer clock input, externally ac coupled, internally biased. REFN is the negative differential input pin for the reference clock (REFCLK) used by the frequency synthesizer. The REFP and REFN look like a differential amplifier with each of the input pins connected to $0.75xV_{DD}$ through a 150Ω resistor. See *Table 7*.

CYP32G0401DX Analog Power Pins (65)

Pin	Name	Function	Description
Y10	VFS1	Analog Power	Frequency Synthesizer PLL VDD1
W11	VFS2	Analog Power	Frequency Synthesizer PLL VDD2
Y9	VFS3	Analog Power	Frequency Synthesizer PLL VDD3
W10	GFS1	Analog Power	Frequency Synthesizer PLL GND1
Y13	GFS2	Analog Power	Frequency Synthesizer PLL GND2
W8	GFS3	Analog Power	Frequency Synthesizer PLL GND3
W13	VTXDa	Analog Power	Channel a transmit VDD1
W17	VTXMa	Analog Power	Channel a transmit VDD2
V13	GTXDa	Analog Power	Channel a transmit GND1
U16	GTXMa	Analog Power	Channel a transmit GND2
U11	VTXDb	Analog Power	Channel b transmit VDD1
R17	VTXMb	Analog Power	Channel b transmit VDD2
W12	GTXDb	Analog Power	Channel b transmit GND1
T18	GTXMb	Analog Power	Channel b transmit GND2
W9	VTXDc	Analog Power	Channel c transmit VDD1
R2	VTXMc	Analog Power	Channel c transmit VDD2
U10	GTXDc	Analog Power	Channel c transmit GND1
P3	GTXMc	Analog Power	Channel c transmit GND2
W7	VTXDd	Analog Power	Channel d transmit VDD1
T3	VTXMd	Analog Power	Channel d transmit VDD2
V8	GTXDd	Analog Power	Channel d transmit GND1

CYP32G0401DX Analog Power Pins (65) (continued)

Pin	Name	Function	Description
R4	GTXMd	Analog Power	Channel d transmit GND2
V15	VRXDa	Analog Power	Channel a receive VDD1
U18	VRXMa	Analog Power	Channel a receive VDD2
U15	GRXDa	Analog Power	Channel a receive GND1
T17	GRXMa	Analog Power	Channel a receive GND2
W14	VRXDb	Analog Power	Channel b receive VDD1
P18	VRXMb	Analog Power	Channel b receive VDD2
V14	GRXDb	Analog Power	Channel b receive GND1
U20	GRXMb	Analog Power	Channel b receive GND2
Y5	VRXDc	Analog Power	Channel c receive VDD1
R3	VRXMc	Analog Power	Channel c receive VDD2
V7	GRXDc	Analog Power	Channel c receive GND1
T2	GRXMc	Analog Power	Channel c receive GND2
W4	VRXDd	Analog Power	Channel d receive VDD1
T4	VRXMd	Analog Power	Channel d receive VDD2
U6	GRXDd	Analog Power	Channel d receive GND1
U1	GRXMd	Analog Power	Channel d receive GND2
P4	AVDD	Analog Power	General Analog VDD
P17	AVDD	Analog Power	General Analog VDD
U4	AVDD	Analog Power	General Analog VDD
U7	AVDD	Analog Power	General Analog VDD
U14	AVDD	Analog Power	General Analog VDD
U17	AVDD	Analog Power	General Analog VDD
V2	AVDD	Analog Power	General Analog VDD
V3	AVDD	Analog Power	General Analog VDD
V18	AVDD	Analog Power	General Analog VDD
V19	AVDD	Analog Power	General Analog VDD
W2	AVDD	Analog Power	General Analog VDD
W3	AVDD	Analog Power	General Analog VDD
W18	AVDD	Analog Power	General Analog VDD
W19	AVDD	Analog Power	General Analog VDD
V1	AGND	Analog Power	General Analog GND
V20	AGND	Analog Power	General Analog GND
W1	AGND	Analog Power	General Analog GND
W20	AGND	Analog Power	General Analog GND
Y1	AGND	Analog Power	General Analog GND
Y2	AGND	Analog Power	General Analog GND
Y3	AGND	Analog Power	General Analog GND
Y8	AGND	Analog Power	General Analog GND
Y11	AGND	Analog Power	General Analog GND
Y12	AGND	Analog Power	General Analog GND
Y18	AGND	Analog Power	General Analog GND
Y19	AGND	Analog Power	General Analog GND
Y20	AGND	Analog Power	General Analog GND

CYP32G0401DX Digital Power Pins (42)

Pin	Name	Function	Description
N19	VDIGCa	Digital Power	Channel a Core VDD
P20	VDIGCb	Digital Power	Channel b Core VDD
B11	VDIGCc	Digital Power	Channel c Core VDD
L4	VDIGCd	Digital Power	Channel d Core VDD
G17	GDIGCa	Digital Power	Channel a Core GND
D12	GDIGCb	Digital Power	Channel b Core GND
D11	GDIGCc	Digital Power	Channel c Core GND
G4	GDIGCd	Digital Power	Channel d Core GND
B2	DVDD	Digital Power	Digital IO Ring VDD
B3	DVDD	Digital Power	Digital IO Ring VDD
B18	DVDD	Digital Power	Digital IO Ring VDD
B19	DVDD	Digital Power	Digital IO Ring VDD
C2	DVDD	Digital Power	Digital IO Ring VDD
C3	DVDD	Digital Power	Digital IO Ring VDD
C18	DVDD	Digital Power	Digital IO Ring VDD
C19	DVDD	Digital Power	Digital IO Ring VDD
D4	DVDD	Digital Power	Digital IO Ring VDD
D7	DVDD	Digital Power	Digital IO Ring VDD
D10	DVDD	Digital Power	Digital IO Ring VDD
D14	DVDD	Digital Power	Digital IO Ring VDD
D17	DVDD	Digital Power	Digital IO Ring VDD
K17	DVDD	Digital Power	Digital IO Ring VDD
M3	DVDD	Digital Power	Digital IO Ring VDD
A1	DGND	Digital Power	Digital IO Ring GND
A2	DGND	Digital Power	Digital IO Ring GND
A3	DGND	Digital Power	Digital IO Ring GND
A9	DGND	Digital Power	Digital IO Ring GND
A10	DGND	Digital Power	Digital IO Ring GND
A13	DGND	Digital Power	Digital IO Ring GND
A18	DGND	Digital Power	Digital IO Ring GND
A19	DGND	Digital Power	Digital IO Ring GND
A20	DGND	Digital Power	Digital IO Ring GND
B1	DGND	Digital Power	Digital IO Ring GND
B20	DGND	Digital Power	Digital IO Ring GND
C1	DGND	Digital Power	Digital IO Ring GND
C20	DGND	Digital Power	Digital IO Ring GND
H1	DGND	Digital Power	Digital IO Ring GND
J20	DGND	Digital Power	Digital IO Ring GND
K20	DGND	Digital Power	Digital IO Ring GND
L1	DGND	Digital Power	Digital IO Ring GND
M1	DGND	Digital Power	Digital IO Ring GND
N20	DGND	Digital Power	Digital IO Ring GND

CYP32G0401DX Cypress Test Pins (6) – User Connect to Ground

Pin	Name	Level	I/O	Description
R20	TMS	-	-	User Connect to Ground
R19	TCK	-	-	User Connect to Ground
T19	TDI	-	-	User Connect to Ground
R18	TRS	-	-	User Connect to Ground
N2	TEST	-	-	User Connect to Ground
C11	TSYNC	-	-	User Connect to Ground

CYP32G0401DX Cypress Special Pins (3) – N/C

Pin	Name	Level	I/O	Description
T20	TDO	-	-	No Connection
P1 P2	ANTEST0 ANTEST1	-	-	No Connection

CYP32G0401DX HOTLink-III Operation

The CYP32G0401DX is a highly configurable device designed to support reliable transfer of large quantities of data, using high-speed serial links. This device supports four single-byte or single-character channels.

General Description

The CYP32G0401DX is a fully integrated quad transceiver device capable of operating at serial rates up to 3.125 Gbps per channel. The CYP32G0401DX has four operating modes: ***MODE 1*** **–** 10-bit SERDES (Ethernet PCS functions; 8B/10B encoding/decoding; COMMA framing), ***MODE 2*** **–** 10-bit SERDES (no encoding/decoding; no framing), ***MODE 3*** **–** 10-bit SERDES (8B/10B encoding/decoding; COMMA framing), and ***MODE 4*** **–** 8-bit SERDES (no encoding/decoding; A1/A2 framing). It performs the 8B/10B encode and decode functions compatible with the 10G Ethernet and InfiniBand physical layer, parallel-to-serial conversion, serial-to-parallel conversion, and clock recovery functions for use in LAN and WAN applications. The Multi-Gigabit Multi-Mode versatility of the CYP32G0401DX was designed for backplane applications for WAN, LAN, WIN, and storage networks' switches and routers as well as for InfiniBand and XAUI 10G Ethernet port applications.

Functional Description

Overview

Figure 4 shows a block diagram of a typical four-channel application. The transceiver has four defined modes of operation as shown in *Table 1*.

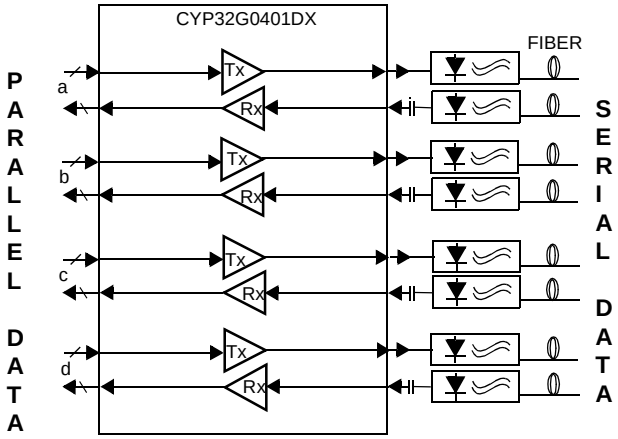


Figure 4. Typical CYP32G0401DX Application Block Diagram

MODE 1 **– 10-bit SERDES (Ethernet PCS functions; 8B/10B encoding/decoding; COMMA framing)**

The transmit side accepts data in the form of 8-bit bytes at up to 312.5 MBps, performs Ethernet PCS functions using the IEEE802.3z ordered set state machine, 8B/10B encoding and serialization of the encoded words into a serial bit stream transmitting at up to 3.125 Gbps. The receive side deserializes the data and performs COMMA framing, 8B/10B decoding, and Ethernet PCS functions. (SER8_10 = 0, ENCODE = 1, FRAME = 1).

MODE 2 **– 10-bit SERDES (no encoding/decoding; no framing)**

The transmit side accepts data in the form of 10-bit words at up to 312.5 Mwps, and serializes them into a bit stream transmitting at up to 3.125 Gbps. The receive side deserializes the data. No encoding/decoding or framing functions are performed. (SER8_10 = 0, ENCODE = 0, FRAME = 0).

MODE 3 **– 10-bit SERDES (8B/10B encoding/decoding; COMMA framing)**

The transmit side accepts data in the form of 8-bit bytes at up to 312.5 MBps, performs 8B/10B encoding, and serializes the encoded words into a bit stream transmitting at up to 3.125 Gbps. The receive side deserializes the data, and performs COMMA framing and 8B/10B decoding. (SER8_10 = 0, ENCODE = 1, FRAME = 0).

MODE 4 **– 8-bit SERDES (no encoding/decoding; A1/A2 framing)**

The transmit side accepts data in the form of 8-bit bytes at up to 350 MBps, and serializes them into a bit stream transmitting at up to 2.8 Gbps. The receive side deserializes the data and performs SONET/SDH A1/A2 framing. (SER8_10 = 1, ENCODE = 0, FRAME = 0).

Table 1. CYP32G0401DX Operating Mode[4]

MODE	SER 8_10	ENCODE	FRAME	APPLICATION
1	0	1	1	10 bit SERDES, 8B/10B encoding/decoding, COMMA framing, and PCS functions
2	0	0	0	10 bit SERDES, no encoding/decoding, and no framing
3	0	1	0	10 bit SERDES, 8B/10B encoding/decoding, and COMMA framing
4	1	0	0	8 bit SERDES, no encoding/decoding, and A1/A2 framing

Note:
4. Choose from four defined operating modes by setting variables SER8_10, ENCODE and FRAME. Selected mode applies to all four channels.

Architecture Overview

Figure 3 is a block diagram showing one of the four multi-gigabit transceiver channels contained within the CYP32G0401DX. Also shown are the internal Management Interface and Frequency Synthesizer blocks, which are common to all channels. Pin names are written in uppercase letters, with lowercase suffixes (a, b, c, d) applied later, as needed, to distinguish among the four channels. In generic cases, the lowercase suffix 'x' will be used to denote channels a, b, c, and d.

Frequency Synthesizer

A Frequency Synthesizer PLL generates the low jitter transmit clock. This clock is derived from a low jitter reference frequency applied differentially at pins REFP and REFN. The output

frequency of the synthesizer is set to provide data output rates between 2.488 Gbps and 3.125 Gbps, and is a multiple of the reference clock frequency. Allowable reference clock frequency ranges are selected by the SER8_10 and FRSYN[1:0] signals, as shown in *Table 2*.

Table 2. Frequency Synthesizer Selectable Input Frequency Range

SER8_10	FRSYN1	FRSYN0	Selected Input Reference Frequency Range (MHz)	TCLKOUT (MHz)	Data Output Rate (Gbps)
0	0	0	125–156.25	250–312.5	2.5–3.125
0	0	1	62.5–78.125	250–312.5	2.5–3.125
0	1	0	31.25–39.0625	250–312.5	2.5–3.125
0	1	1	test mode—do not use		
1	0	0	155.5–175	311-350	2.488–2.8
1	0	1	77.75–87.5	311–350	2.488–2.8
1	1	0	38.875–43.75	311–350	2.488–2.8
1	1	1	test mode—do not use		

The Frequency Synthesizer output is divided to produce a word clock signal that clocks data out of the Transmit Phase Align FIFO. This word clock is available at the TCLKOUT pin. The Frequency Synthesizer output also clocks data out of the parallel-to-serial converter.

Transmit Phase Align FIFO

The input data TXD[7:0], TXEN, and TXER are clocked into the Phase Align FIFO on the rising edge of the GTXCLK signal. The data is read out of the FIFO with TCLKOUT. The phase of GTXCLK can differ from that of TCLKOUT with any difference and relative jitter absorbed by the FIFO. This is a 10-bit wide by 64-word deep FIFO. **Note**: To minimize latency through the FIFO, only two data words need be input before data output from the FIFO begins.

Parallel-to-Serial Converter

The parallel-to-serial converter operates in two modes, eight-bit and ten-bit, under the control of the SER8_10 pin, as shown in *Table 3*.

Table 3. Serial Conversion Modes

SER8_10 Signal	Serializer Function
Logic 1	8 to 1
Logic 0	10 to 1

Note: The serializer **always** outputs data LSB first (Ethernet convention). However in ***MODE 4*** the convention is to transmit MSB first. In order to conform to the desired standard, when the pin SER8_10 is active HIGH, data is presented to the serializer in reverse bit order; i.e., a data word presented at the TXD pins as {D7, D6, D5, D4, D3, D2, D1, D0} is presented to the serializer as {D0, D1, D2, D3, D4, D5, D6, D7}.

Ethernet PCS Functions

The Ethernet PCS functions are enabled (FRAME = 1) whenever the CYP32G0401DX is operated in ***MODE 1***. This performs Ethernet PCS functions using the IEEE802.3z ordered set state machine, Section 36.2.5.2.1 and Figures 36-5 and 36-6.

8B/10B Encoder

The CYP32G0401DX contains an 8B/10B encoder to translate the 8-bit input byte to a 10-bit symbol. This function can be bypassed by setting ENCODE LOW. To facilitate alignment of the 10-bit word by the Receive FRAMER, a COMMA character may be generated. This is automatic when in ***MODE 1***, or under the control of TXER (TXK) in ***MODE 3***. The 8B/10B encoder is standards compliant with ANSI/NCITS ASC X3.230-1994 (Fibre Channel), IEEE 802.3z (Gigabit Ethernet), the IBM® ESCON® and FICON™ channels, and ATM Forum standards for data transport.

Notation Conventions

The 8B/10B transmission code uses letter notation for describing the bits of an unencoded information octet and a single control variable. Each bit of the unencoded information octet contains either a binary zero or a binary one. A control variable, Z, has either the value D or the value K. When the control variable associated with an unencoded information octet contains the value D, the associated encoded code-group is referred to as a data code-group. When the control variable associated with an unencoded information octet contains the value K, the associated encoded code-group is referred to as a special code-group. The bit notation of A,B,C,D,E,F,G,H for an unencoded information octet is used in the description of the 8B/10B transmission code. The bits A,B,C,D,E,F,G,H are translated to bits a,b,c,d,e,i,f,g,h,j of 10-bit transmission code-groups. See *Table 11* at the end of this document for the 8B/10B code-group bit assignments, or refer to Table 36-1 of IEEE802.3. Each valid code-group has been given a name using the following convention: /Dx.y/ for the 256 valid data code-groups, and /Kx.y/ for special control code-groups, where x is the decimal value of bits EDCBA, and y is the decimal value of bits HGF.

Valid special code-groups

See *Table 12* at the end of this document for the valid special code-groups, or refer to Table 36-2 of IEEE802.3.

Loop back

When loop back is enabled (LBEN = 1) both the high-speed line side data and the byte input data are looped back as follows:

- The parallel input data (TXD[7:0], TXEN, TXER) is looped back to the receive side parallel data (RXD[7:0], RXDV, RXER)
- The line-received data (RXP and RXN) is looped back and sent to the line driver (TXP and TXN).
- In ***MODE 1*** the transmit driver (TXP, TXN) is disabled, as required in IEEE802.3 Section 22.2.4.1.2.

Note: LBEN is logically ORed with bit 0.14 of the control register.

Line Driver

The line driver operates at CML levels, with the output pins TXP and TXN. Electrically, the TXP and TXN look like a differential amplifier with each of its output drains connected to V_{DD} through a 50Ω resistor.

Line Receiver

A differential signal input on the input pins (RXP, RXN) will be recovered and converted into a binary stream by the receiver. The line receiver is internally biased, and should be capacitively coupled to the driving stage. The RXP and RXN pins are inputs to a differential amplifier with each of the pins connected to $V_{DD}/2$ through a 150Ω resistor.

Loss of Signal

The signal input on the LOS pin may come from a fiber module and indicates if there is a Loss of Signal (LOS) condition. If a LOS condition occurs, the data input is squelched and no data is sent to the data recovery block. When no data edges are present at the inputs to the clock recovery Digital Phase-Locked Loop (DPLL), its output frequency will be locked to the frequency of the transmit Frequency Synthesizer. The polarity of the LOS signal is controlled by the POL pin as shown in *Table 4*.

Table 4. LOS Signal Polarity Control

POL	LOS	RX Data Path
0	0	Enabled
0	1	Disabled
1	0	Disabled
1	1	Enabled

Clock and Data Recovery

The input data is sent to a DPLL circuit, which recovers the clock. The data edges from the receiver are used to select a phase tapped from the transmit side Frequency Synthesizer. Any difference in frequency between the synthesizer and input data is accommodated by continually adjusting the phase that is tapped. This clock is used to determine the input signal to the deserializer.

Deserializer

The recovered data is converted into an 8-bit or 10-bit parallel word, with arbitrary alignment. The first bit received is assigned to the least significant bit of that parallel word.

Data Framer

Note: The data input to this block from the deserializer is in an "LSB first" format (Ethernet style data). When in ***MODE 4*** (indicated by SER8_10=1) the data alignment block reformats the incoming data word to follow the desired convention of "MSB first" i.e., a data word presented by the deserializer as {0, 0, D7, D6, D5, D4, D3, D2, D1, D0} is reformatted to become {0, 0, D0, D1, D2, D3, D4, D5, D6, D7}.

A1/A2 Framer

In ***MODE 4*** when OOF is active (HIGH), framing is achieved as follows: The alignment state machine will search for the A1/A2 framing sequence and when it is found, will pulse FRP for one cycle. The FRP output will appear on the CRS pin (***MODE 4*** only). Also, the correctly realigned 8-bit word will be output. If OOF is inactive (low), the previous alignment will be used for the 8-bit word. The framing sequence will consist of 3 A1s followed by 3 A2s. The A1 and A2 characters used for framing are as follows:

A1=0xF6 (8'b11110110), A2=0x28 (8'b00101000),

where **0x** indicates hexadecimal, and **8'b** indicates 8-bit binary.

COMMA Framer

In ***MODE 1*** and ***MODE 3*** the framing of the 10-bit symbol at the receive side is achieved by a barrel shifter as follows. Two sequential 10-bit symbols of the data are first loaded into the barrel shifter. When a COMMA character is detected at any alignment, that alignment is used to register the current data.

8B/10B Decoder

The CYP32G0401DX contains an 8B/10B decoder to translate the 10-bit symbol to the 8-bit byte originally input to the encoder at the other end. The data arrives at the decoder with the 10-bit symbol having already been framed by the COMMA Framer as described above. The 8B/10B decode function can be bypassed by setting ENCODE LOW.

Ethernet PCS Functions

The Ethernet PCS functions are enabled (FRAME = 1) whenever the CYP32G0401DX is operated in ***MODE 1***. This performs Ethernet PCS functions using the IEEE802.3z receive and synchronization state machines, Section 36.2.5.2.2 and Figures 36-7a, 36-7b, 36-8, and 36-9.

Serial-to-Parallel Converter

The serial-to-parallel converter operates in two modes, eight-bit and ten-bit, under the control of the SER8_10 pin, as shown in*Table 3*.

Receive Elasticity FIFO

This is a 12-bit wide by 64-word deep FIFO used to absorb line input jitter and allow phase alignment to the selected output clock. The input data word comprises 10-bit data plus CRS and COL.

RXCLK Output

The RXCLK pin outputs either a buffered RCLKIN, or the recovered clock. This is determined by the status of LBEN on the rising edge of RESETN as follows: LBEN=0 selects the buffered RCLKIN; LBEN=1 selects the recovered clock.

Reset

An internal "Power On Reset" function (POR) ensures that following the application of power at all supply pins of the CYP32G0401DX, all circuitry on the device is properly initialized and no external action is required for the device to commence operation. An external RESETN pin reflects the operation of the POR circuit thus:

- When POR is active RESETN is driven LOW.
- When POR is inactive RESETN is three-stated and an internal pull up resistor (approximately 50 kΩ) establishes the inactive (HIGH) state.

The RESETN pin may also be driven from an external device in order to re-initialize the chip regardless of the internal operating state and regardless of the state of POR. In this case RESETN must be driven low for a minimum of two cycles of the reference clock (REFP, REFN), though no other timing relationship between RESETN and the reference clock need exist.

Built-In-Self-Test Mode (BIST)

When operating in ***MODE 1*** and with register 30.8 set, Built-In-Self-Test (BIST) mode is selected. In this mode a pseudo-random data sequence is continuously transmitted instead of the IDLE sequence (or any input data packet). The first character of this sequence is always the Start-of-packet, /S/ character (K27.7) which ensures that a receiver will recognize the data stream as a packet. The pseudo-random sequence is generated by a 16-bit polynomial represented by $X_n = X_{n+15}$ EXOR X_{n+14}.

A self-synchronizing comparator function incorporated within the FRAMER checks the incoming data stream against the expected polynomial sequence and generates an error flag when a mismatch occurs. The error flag is logically ORed into the RXER output. The recovered pseudo-random sequence is also decoded and echoed on the RXD bus.

Management Interface

A management interface on the chip provides serial I/O capabilities as specified in IEEE802.3 Chapter 22. External access to the interface is made through two pins: the management data input/output pin, MDIO, and the management data clock input pin, MDC. Control and status information is serially transferred to and from the CYP32G0401DX on MDIO, with reference timing for the transfer supplied externally on MDC.

Control information must be input on MDIO synchronously relative to MDC, allowing the CYP32G0401DX to sample it synchronously. In turn, status information from the CYP32G0401DX is output on MDIO synchronously relative to MDC, and must be synchronously sampled externally.

MDC is an aperiodic signal with minimum HIGH and LOW times of 160 ns, and a minimum period of 400 ns. There are no maximum HIGH or LOW times for MDC.

Table 5 identifies the available management interface registers, and *Table 6* provides the management frame format. The order of transmission is from left to right.

Referring to *Table 6*:

PRE = Preamble (32 contiguous logic one bits)

ST = Start of frame (01)

OP = Operation code (Read = 10, Write = 01)

PHYAD = PHY Address (Represented below as “vwxyz”)

The PHYSICAL MDIO ADDRESS for the CYP32G0401DX is set at the end of reset. When RESETN goes HIGH the three signals ENCODE, FRAME and SER8_10 are locked in as the first three bits (vwx) of PHYAD (See *Table 7*). The last two bits (yz) identify the channel (See *Table 8*). For example, PHYAD = 11010 is the address for channel c for the case in which ENCODE = 1, FRAME = 1, and SER8_10 = 0 at the end of reset.

REGAD = Register Address

TA = Turnaround (delay for turn on/off of bus drivers)

DATA = Data (16 bits, bit 15 transmitted first)

IDLE = High impedance state on MDIO

.

Table 5. Management Interface Registers

Register	Description	Default
Register 0	PHY control register (c.f. IEEE802.3 Table 22.7)	0x3140
Register 1	PHY status register (c.f. IEEE802.3 Table 22.8)	0x0109
Register 2	PHY identifier register upper bits (c.f. IEEE802.3 Figure 22.12)	0x000a
Register 3	PHY identifier register lower bits (c.f. IEEE802.3 Figure 22.12)	0x3011
Register 4	Autonegotiation advertisement register (c.f. IEEE802.3 Table 37.5)	0x0060
Register 5	Autonegotiation partner ability register (c.f. IEEE802.3 Table 37.6)	0x0000
Register 6	Autonegotiation expansion (c.f. IEEE802.3 Table 37.7)	0x0000
Register 15	Extended status register (c.f. IEEE802.3 Table 22.9)	0x0000
Register 30	Set *BIT 8* = 1 for BIST (***MODE 1*** only). All other bits reserved.	0x0000
Register 31	(RESERVED)	0x0000

Table 6. Management Frame Format[5]

	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ	1…1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1…1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Note:
5. Z = high impedance on PHY’s MDIO. It also occurs during READ TA as well as IDLE.

Table 7. Chip Portion of PHYAD

ENCODE	FRAME	SER8_10	First 3 Bits (vwx) Chip PHYAD
On Rising Edge of RESETN:			
0	0	0	000
0	0	1	001
0	1	0	010
0	1	1	011
1	0	0	100
1	0	1	101
1	1	0	110
1	1	1	111

Table 8. Channel Portion of PHYAD

Last 2 Bits (yz) Channel PHYAD	Channel ID
00	a
01	b
10	c
11	d

MDIO/MDC Timing Relationship

MDIO (Management Data Input/Output) is a bidirectional signal that can be sourced by the Station Management Entity (STA) or the CYP32G0401DX. When the STA sources the MDIO signal, the STA shall provide a minimum of 10 ns of set-up time and a minimum of 10 ns of hold time referenced to the rising edge of MDC. When the MDIO signal is sourced by the CYP32G0401DX, it is sampled by the STA synchronously with respect to the rising edge of MDC. The clock to output delay from the CYP32G0401DX shall be a minimum of 0 ns and a maximum of 300ns. See *Figure 5*.

SSTL_2 Outputs

The SSTL_2 outputs meet the requirements of Section 3 of EIA/JESD8-9 for Class II outputs.

Line Receiver Requirements

The line receiver is compatible with the line driver when capacitively coupled and connected through a backplane of up to 19 inches of properly terminated microstrip or stripline transmission line on FR4. As shown in *Figure 6*, the RXP and RXN look like a differential amplifier with each of the input pins connected to $V_{DD}/2$ through a 150Ω resistor. When inputs are differentially terminated with a 150Ω resistor, the line termination is nominally 100Ω. Similarly the reference clock inputs, REFP and REFN, look like a differential amplifier with each of the input pins connected to $0.75xV_{DD}$ through a 150Ω resistor. This is shown in *Figure 7*.

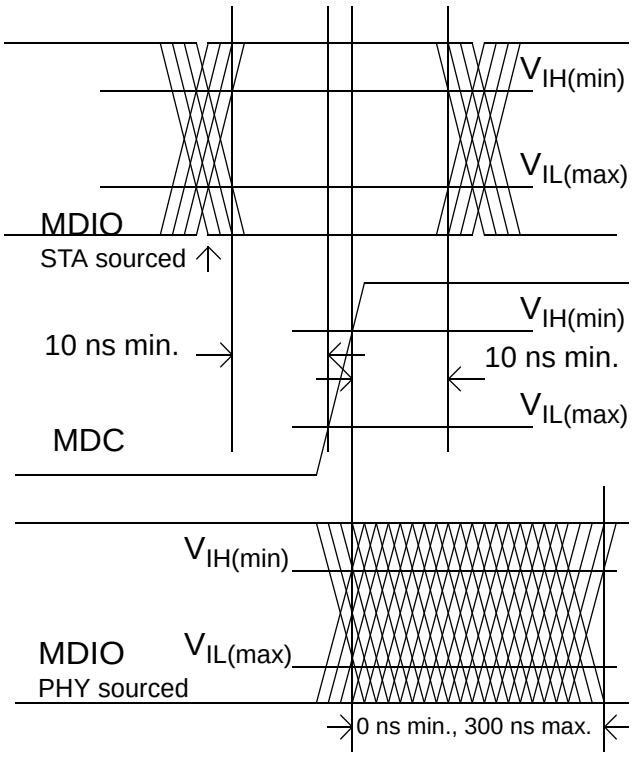


Figure 5. MDIO/MDC Timing Relationship

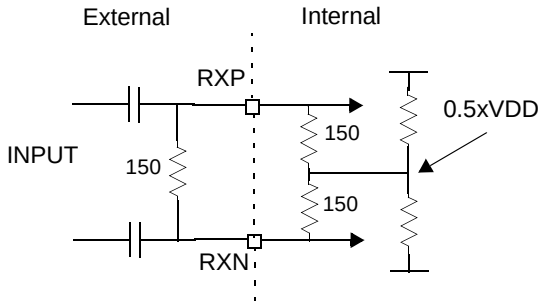


Figure 6. Receiver Input Termination

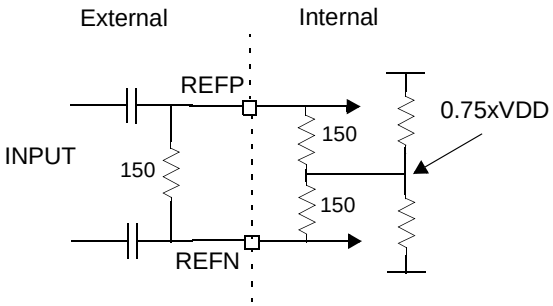


Figure 7. Reference Clock Termination

Line Driver Requirements

The line driver has CML outputs which may be coupled to any fiber module. The TXP and TXN look like a differential amplifier with each of the output drains connected to VDD through a 50Ω resistor.

CYP32G0401DX Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	DC Supply Voltage	2.375	2.5	2.625	V
T_{OP}	Operating Ambient Temperature Range	–40	--	85	°C
P_{DISS}	Power Dissipation	--	2.5	--	W
VDD_{RIPPLE}	Ripple	--	--	50	mV peak-to-peak

CYP32G0401DX SSTL_2 Inputs[6]

Parameter	Description	Min.	Max.	Unit
V_{REF}[7]	Logic Reference Voltage	$0.5xV_{DD}$ – 5%	$0.5xV_{DD}$ + 5%	V
V_{IH}	High Level Input Voltage	1.56	V_{DD} + 0.3	V
V_{IL}	Low Level Input Voltage	–0.3	0.94	V
I_{IH}	High Level Input Current	--	40	µA
I_{IL}	Low Level Input Current	-600	--	µA
C_I	Pin Capacitance to ground	--	4	pF

CYP32G0401DX SSTL_2 Outputs[8]

Parameter	Description	Min.	Max.	Unit
V_{REF}[7]	Logic reference voltage	$0.5xV_{DD}$ – 5%	$0.5xV_{DD}$ + 5%	V
V_{OH}	High Level Output Voltage	0.75 x V_{DD}	V_{DD}	V
V_{OL}	Low Level Output Voltage	0	0.25 x V_{DD}	V
I_{OH}	High level Output Current	–7.6	--	mA
I_{OL}	Low Level Output Current	--	7.6	mA
C_O	Pin Capacitance to ground	--	4	pF

CYP32G0401DX Single Ended LVPECL Inputs

Parameter	Description	Min.	Max.	Unit
V_{IL}	Low Level Input Voltage	V_{DD} – 2.0	V_{DD} – 1.47	V
V_{IH}	High Level Input Voltage	V_{DD} – 1.18	V_{DD} – 0.80	V

CYP32G0401DX Differential Reference Clock Inputs (REFP, REFN) - Differential CML

Parameter	Description	Condition	Min.	Max.	Unit
V_{CM}	Common Mode Input Voltage	--	0.65 x V_{DD}	0.85 x V_{DD}	V
V_{IDIF}[9]	Differential Input Voltage	--	175	2000	mV peak-to-peak
$\|I_{IH}\|$	Input High Current	V_{IDIF} = 0.5V	1.0	2.0	mA
$\|I_{IL}\|$	Input Low Current	V_{IDIF} = 0.5V	1.0	2.0	mA
Duty Cycle	Percent Duty Cycle	--	40	60	%

Notes:

6. The inputs meet the requirements of Section 2.2 of EIA/JESD8-9.
7. VREF is generated internally to the chip.
8. The outputs meet the requirements of Section 3 of EIA/JESD8-9 for Class I outputs.
9. AC coupled, with each input internally biased to $0.75xV_{DD}$ through a 150Ω resistor, as shown in *Figure 7*.

CYP32G0401DX Transmit Data Input Timing

Parameter	Description	Min.	Max.	Unit
t_{TXDS}	Set-up time to GTXCLK rising TXD[7:0]x, TXENx, TXERx	700	--	ps
t_{TXDH}	Hold time from GTXCLK rising TXD[7:0]x, TXENx, TXERx	200	--	ps
$t_{GTXCLKH}$	GTXCLKx high	1.42	--	ns
$t_{GTXCLKL}$	GTXCLKx low	1.42	--	ns
t_{GTXCLK}	GTXCLKx period	2.84	--	ns

CYP32G0401DX Receive Data Output Timing

Parameter	Description	Min.	Max.	Unit
t_{RXDH}	Hold time with respect to RXCLKx rising $RXD[7:0]_X$, RXERx, RXDVx, CRSx, COLx	250	--	ps
$t_{RCLKINH}$	RCLKINx high	1.42	--	ns
$t_{RCLKINL}$	RCLKINx low	1.42	--	ns
t_{RCLKIN}	RCLKINx period	2.84	--	ns

CYP32G0401DX RXPx-RXNx Line Receiver Inputs - Differential CML

Parameter	Description	Condition	Min.	Max.	Unit
V_{CM}	Common Mode Input Voltage	--	0.4 x V_{DD}	0.6 x V_{DD}	V
V_{IDIF}	Differential Input Voltage	--	175	2000	mV peak-to-peak
$\|I_{IH}\|$	Input High Current	V_{IDIF} = 0.5V	1.0	2.0	mA
$\|I_{IL}\|$	Input Low Current	V_{IDIF} = 0.5V	1.0	2.0	mA
$LOSS_{IR}$	Input Return Loss[10]	--	10	--	dB

CYP32G0401DX TXPx-TXNx Line Driver Outputs - Differential CML

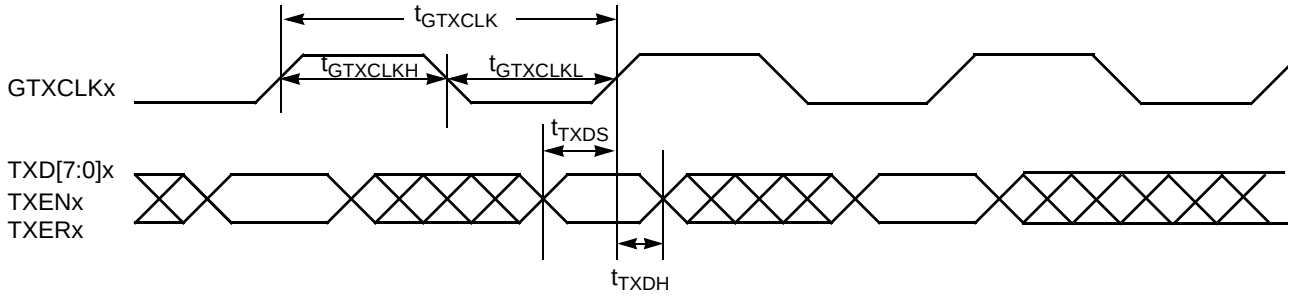
PARAMETER	DESCRIPTION	MIN	MAX	UNITS
Vo_{SE}	Single Ended Output Voltage[11]	400	950	mV peak-to-peak
Vo_{DIFF}	Differential Output Voltage[11]	800	1900	mV peak-to-peak
t_{RISE}	Rise Time (10% to 90%)	110	200	ps
t_{FALL}	Fall Time (10% to 90%)	110	200	ps

Notes:

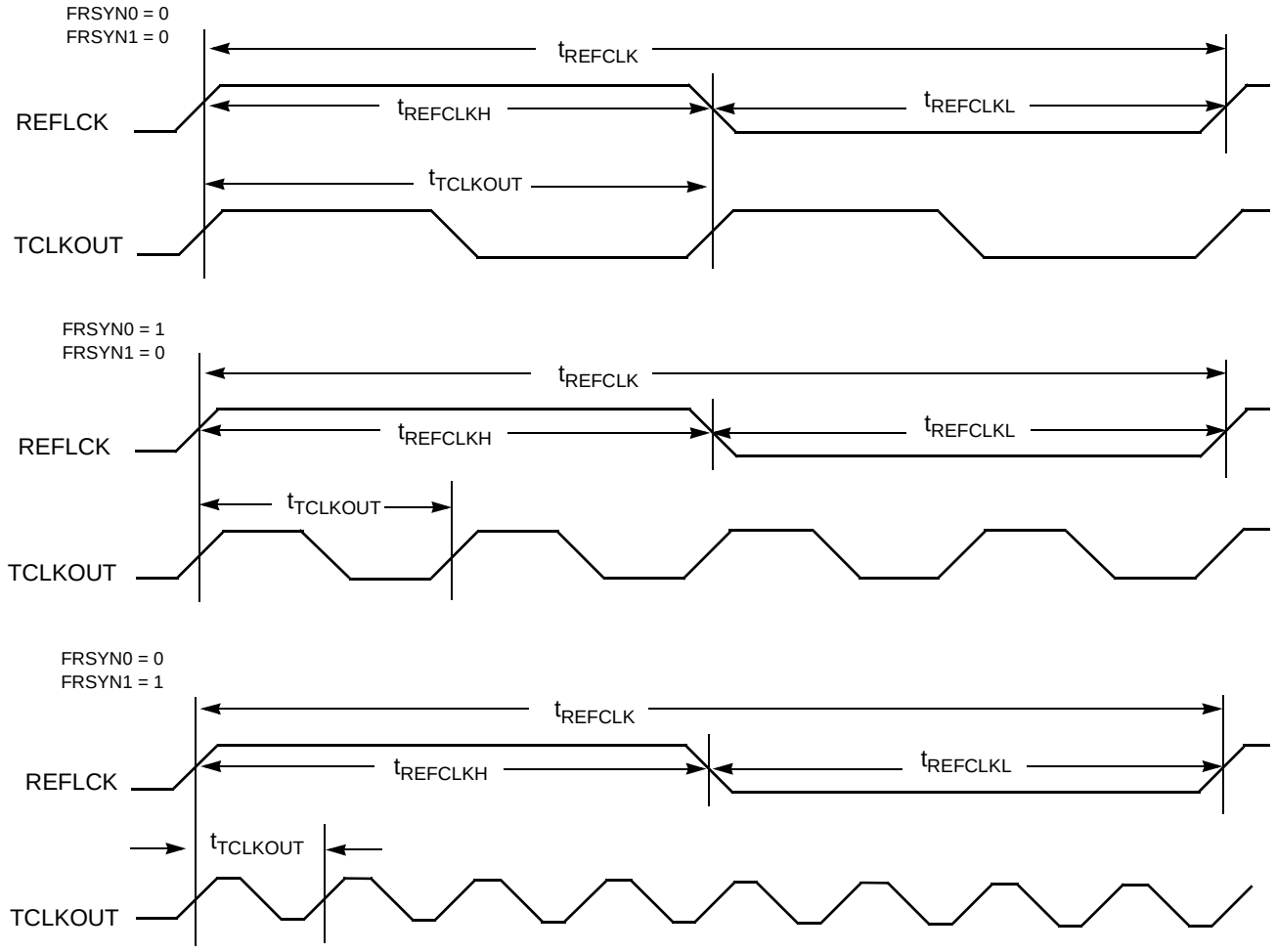
10. Using receiver input termination shown in *Figure 6*.
11. Voltage swings measured with 100Ω load AC coupled line to line.

Switching Waveforms for the CYP32G0401DX Transmitter

Transmit Interface Write Timing[12]



TCLKOUT Timing[13]

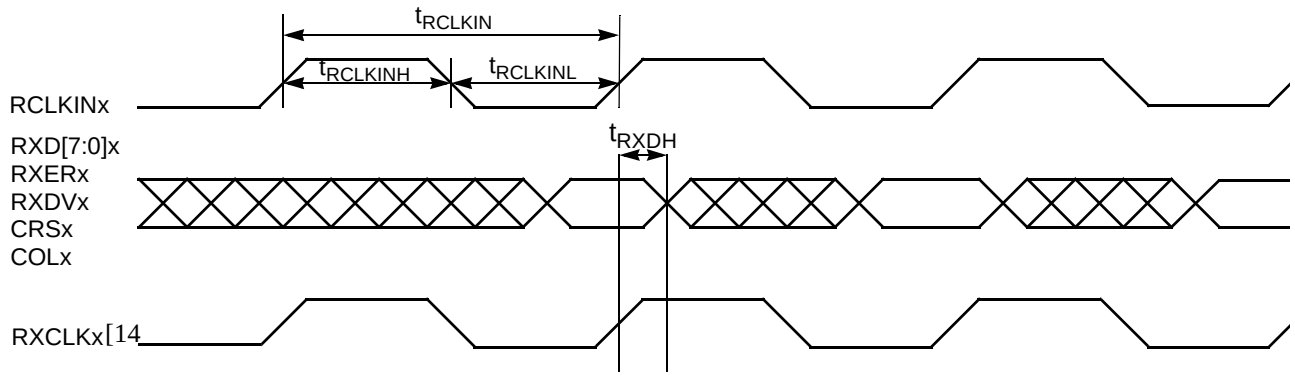


Notes:

12. Lowercase suffix 'x' is used to denote channels a, b, c, and d.
13. TCLKOUT is phase locked to REFCLK and is a multiple (2x, 4x, or 8x) of the REFCLK frequency. See *Table 2* for further details.

Switching Waveforms for the CYP32G0401DX Receiver

Receive Interface Read Timing[14]



Note:
14. RXCLKx is delayed in phase from RCLKINx.

ANSI X3.230 (FC-PH) Codes and Notation

Information to be transmitted over a serial link is encoded 8 bits at a time into a 10-bit Transmission Character and then sent serially, bit by bit. Information received over a serial link is collected ten bits at a time, and those Transmission Characters that are used for data (Data Characters) are decoded into the correct eight-bit codes. The 10-bit Transmission Code supports all 256 8-bit combinations. Some of the remaining Transmission Characters (Special Characters) are used for functions other than data transmission.

The primary rationale for use of a Transmission Code is to improve the transmission characteristics of a serial link. The encoding defined by the Transmission Code ensures that sufficient transitions are present in the serial bit stream to make clock recovery possible at the Receiver. Such encoding also greatly increases the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of information. In addition, some Special Characters of the Transmission Code selected by Fibre Channel Standard consist of a distinct and easily recognizable bit pattern (the Special Character COMMA) that assists a Receiver in achieving word alignment on the incoming bit stream.

Notation Conventions

The documentation for the 8B/10B Transmission Code uses letter notation for the bits in an 8-bit byte. Fibre Channel Standard notation uses a bit notation of A, B, C, D, E, F, G, H for the 8-bit byte for the raw 8-bit data, and the letters a, b, c, d, e, i, f, g, h, j for encoded 10-bit data. There is a correspondence between bit A and bit a, B and b, C and c, D and d, E and e, F and f, G and g, and H and h. Bits i and j are derived, respectively, from (A,B,C,D,E) and (F,G,H).

The bit labeled A in the description of the 8B/10B Transmission Code corresponds to bit 0 in the numbering scheme of the FC-2 specification, B corresponds to bit 1, as shown below.

FC-2 bit designation—	7	6	5	4	3	2	1	0
HOTLink D/Q designation—	7	6	5	4	3	2	1	0
8B/10B bit designation—	H	G	F	E	D	C	B	A

To clarify this correspondence, the following example shows the conversion from an FC-2 Valid Data Byte to a Transmission Character (using 8B/10B Transmission Code notation)

```
FC-2  45
      Bits: 7654 3210
            0100 0101
```

Converted to 8B/10B notation (note carefully that the order of bits is reversed):

```
Data Byte Name   D5.2
                 Bits:ABCDEFGH
                      10100 010
```

Translated to a transmission Character in the 8B/10B Transmission Code:

```
      Bits: abcdeifghj
            1010010101
```

Each valid Transmission Character of the 8B/10B Transmission Code has been given a name using the following convention: cxx.y, where c is used to show whether the Transmission Character is a Data Character (c is set to D) or a Special Character (c is set to K). When c is set to D, xx is the decimal value of the binary number composed of the bits E, D, C, B, and A in that order, and the y is the decimal value of the binary number composed of the bits H, G, and F in that order. When c is set to K, xx and y are derived by comparing the encoded bit patterns of the Special Character to those patterns derived from encoded Valid Data bytes and selecting the names of the patterns most similar to the encoded bit patterns of the Special Character.

Under the above conventions, the Transmission Character used for the examples above, is referred to by the name D5.2. The Special Character K29.7 is so named because the first six bits (abcdei) of this character make up a bit pattern similar to that resulting from the encoding of the unencoded 11101 pattern (29), and because the second four bits (fghj) make up a bit pattern similar to that resulting from the encoding of the unencoded 111 pattern (7).

Note: This definition of the 10-bit Transmission Code is based on (and is in basic agreement with) the following references, which describe the same 10-bit transmission code.

A.X. Widmer and P.A. Franaszek. “A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code” *IBM Journal of Research and Development*, 27, No. 5: 440–451 (September, 1983).

U.S. Patent 4,486,739. Peter A. Franaszek and Albert X. Widmer. “Byte-Oriented DC Balanced (0.4) 8B/10B Partitioned Block Transmission Code” (December 4, 1984).

Fibre Channel Physical and Signaling Interface (ANS X3.230–1994 ANSI FC–PH Standard).

IBM Enterprise Systems Architecture/390 ESCON I/O Interface (document number SA22–7202).

8B/10B Transmission Code

The following information describes how the tables are used for both generating valid Transmission Characters (encoding) and checking the validity of received Transmission Characters (decoding). It also specifies the ordering rules to be followed when transmitting the bits within a character and the characters within the higher-level constructs specified by the standard.

Transmission Order

Within the definition of the 8B/10B Transmission Code, the bit positions of the Transmission Characters are labeled a, b, c, d, e, i, f, g, h, j. Bit “a” is transmitted first followed by bits b, c, d, e, i, f, g, h, and j in that order. (Note that bit i is transmitted between bit e and bit f, rather than in alphabetical order.)

Valid and Invalid Transmission Characters

The following tables define the valid Data Characters and valid Special Characters (K characters), respectively. The tables are used for both generating valid Transmission Characters (encoding) and checking the validity of received Transmission Characters (decoding). In the tables, each Valid-Data-byte or Special-Character-code entry has two columns that represent two (not necessarily different) Transmission Characters. The two columns correspond to the current value of the running disparity (“Current RD–” or “Current RD+”). Running disparity is a binary parameter with either the value negative (–) or the value positive (+).

After powering on, the Transmitter will assume a negative value for its initial running disparity. Upon transmission of any Transmission Character, the transmitter selects the proper version of the Transmission Character based on the current running disparity value, and the Transmitter calculates a new

value for its running disparity based on the contents of the transmitted character.

After powering on, the Receiver may assume either a positive or negative value for its initial running disparity. Upon reception of any Transmission Character, the Receiver decides whether the Transmission Character is valid or invalid according to the following rules and tables and calculates a new value for its Running Disparity based on the contents of the received character.

The following rules for running disparity are used to calculate the new running-disparity value for Transmission Characters that have been transmitted (Transmitter's running disparity) and that have been received (Receiver's running disparity).

Running disparity for a Transmission Character shall be calculated from sub-blocks, where the first six bits (abcdei) form one sub-block and the second four bits (fghj) form the other sub-block. Running disparity at the beginning of the 6-bit sub-block is the running disparity at the end of the previous Transmission Character. Running disparity at the beginning of the 4-bit sub-block is the running disparity at the end of the 6-bit sub-block. Running disparity at the end of the Transmission Character is the running disparity at the end of the 4-bit sub-block.

Running disparity for the sub-blocks are calculated as follows:

1. Running disparity at the end of any sub-block is positive if the sub-block contains more ones than zeros. It is also positive at the end of the 6-bit sub-block if the 6-bit sub-block is 000111, and it is positive at the end of the 4-bit sub-block if the 4-bit sub-block is 0011.
2. Running disparity at the end of any sub-block is negative if the sub-block contains more zeros than ones. It is also negative at the end of the 6-bit sub-block if the 6-bit sub-block is 111000, and it is negative at the end of the 4-bit sub-block if the 4-bit sub-block is 1100.
3. Otherwise, running disparity at the end of the sub-block is the same as at the beginning of the sub-block.

Use of the Tables for Generating Transmission Characters

The appropriate entry in the table are found for the Valid Data byte or the Special Character byte for which a Transmission Character is to be generated (encoded). The current value of the Transmitter's running disparity shall be used to select the Transmission Character from its corresponding column. For each Transmission Character transmitted, a new value of the running disparity shall be calculated. This new value shall be used as the Transmitter's current running disparity for the next Valid Data byte or Special Character byte to be encoded and transmitted. *Table 9* shows naming notations and examples of valid transmission characters.

Use of the Tables for Checking the Validity of Received Transmission Characters

The column corresponding to the current value of the Receiver's running disparity is searched for the received Transmission Character. If the received Transmission Character is found in the proper column, then the Transmission Character is valid and the associated Data byte or Special Character code is determined (decoded). If the received Transmission Character is not found in that column, then the Transmission Character is invalid. This is called a code violation. Independent of the Transmission Character's validity, the received Transmission Character is used to calculate a new value of running disparity. The new value is used as the Receiver's current running disparity for the next received Transmission Character.

Table 9. Valid Transmission Characters

Data			
	D_{IN} or Q_{OUT}		
Byte Name	765	43210	Hex Value
D0.0	000	00000	00
D1.0	000	00001	01
D2.0	000	00010	02
. .	. .	. .	. .
D5.2	010	00010 1	45
. .	. .	. .	. .
D30.7	111	11110	FE
D31.7	111	11111	FF

Detection of a code violation does not necessarily show that the Transmission Character in which the code violation was detected is in error. Code violations may result from a prior error that altered the running disparity of the bit stream which did not result in a detectable error at the Transmission Character in which the error occurred. *Table 10* shows an example of this behavior.

Table 10. Code Violations Resulting from Prior Errors

	RD	Character	RD	Character	RD	Character	RD
Transmitted data character	–	D21.1	–	D10.2	–	D23.5	+
Transmitted bit stream	–	101010 1001	–	010101 0101	–	111010 1010	+
Bit stream after error	–	101010 1011	+	010101 0101	+	111010 1010	+
Decoded data character	–	D21.0	+	D10.2	+	Code Violation	+

Table 11. Valid Data Characters (*MODE 1* and *MODE 3*)

Data Byte Name	Bits	Current RD–	Current RD+	Data Byte Name	Bits	Current RD–	Current RD+
	HGF EDCBA	abcdei fghj	abcdei fghj		HGF EDCBA	abcdei fghj	abcdei fghj
D0.0	000 00000	100111 0100	011000 1011	D0.1	001 00000	100111 1001	011000 1001
D1.0	000 00001	011101 0100	100010 1011	D1.1	001 00001	011101 1001	100010 1001
D2.0	000 00010	101101 0100	010010 1011	D2.1	001 00010	101101 1001	010010 1001
D3.0	000 00011	110001 1011	110001 0100	D3.1	001 00011	110001 1001	110001 1001
D4.0	000 00100	110101 0100	001010 1011	D4.1	001 00100	110101 1001	001010 1001
D5.0	000 00101	101001 1011	101001 0100	D5.1	001 00101	101001 1001	101001 1001
D6.0	000 00110	011001 1011	011001 0100	D6.1	001 00110	011001 1001	011001 1001
D7.0	000 00111	111000 1011	000111 0100	D7.1	001 00111	111000 1001	000111 1001
D8.0	000 01000	111001 0100	000110 1011	D8.1	001 01000	111001 1001	000110 1001
D9.0	000 01001	100101 1011	100101 0100	D9.1	001 01001	100101 1001	100101 1001
D10.0	000 01010	010101 1011	010101 0100	D10.1	001 01010	010101 1001	010101 1001
D11.0	000 01011	110100 1011	110100 0100	D11.1	001 01011	110100 1001	110100 1001
D12.0	000 01100	001101 1011	001101 0100	D12.1	001 01100	001101 1001	001101 1001
D13.0	000 01101	101100 1011	101100 0100	D13.1	001 01101	101100 1001	101100 1001
D14.0	000 01110	011100 1011	011100 0100	D14.1	001 01110	011100 1001	011100 1001
D15.0	000 01111	010111 0100	101000 1011	D15.1	001 01111	010111 1001	101000 1001
D16.0	000 10000	011011 0100	100100 1011	D16.1	001 10000	011011 1001	100100 1001
D17.0	000 10001	100011 1011	100011 0100	D17.1	001 10001	100011 1001	100011 1001
D18.0	000 10010	010011 1011	010011 0100	D18.1	001 10010	010011 1001	010011 1001
D19.0	000 10011	110010 1011	110010 0100	D19.1	001 10011	110010 1001	110010 1001
D20.0	000 10100	001011 1011	001011 0100	D20.1	001 10100	001011 1001	001011 1001
D21.0	000 10101	101010 1011	101010 0100	D21.1	001 10101	101010 1001	101010 1001
D22.0	000 10110	011010 1011	011010 0100	D22.1	001 10110	011010 1001	011010 1001
D23.0	000 10111	111010 0100	000101 1011	D23.1	001 10111	111010 1001	000101 1001
D24.0	000 11000	110011 0100	001100 1011	D24.1	001 11000	110011 1001	001100 1001
D25.0	000 11001	100110 1011	100110 0100	D25.1	001 11001	100110 1001	100110 1001
D26.0	000 11010	010110 1011	010110 0100	D26.1	001 11010	010110 1001	010110 1001
D27.0	000 11011	110110 0100	001001 1011	D27.1	001 11011	110110 1001	001001 1001
D28.0	000 11100	001110 1011	001110 0100	D28.1	001 11100	001110 1001	001110 1001
D29.0	000 11101	101110 0100	010001 1011	D29.1	001 11101	101110 1001	010001 1001
D30.0	000 11110	011110 0100	100001 1011	D30.1	001 11110	011110 1001	100001 1001
D31.0	000 11111	101011 0100	010100 1011	D31.1	001 11111	101011 1001	010100 1001

Table 11. Valid Data Characters (*MODE 1* and *MODE 3*) (continued)

Data Byte Name	Bits	Current RD–	Current RD+	Data Byte Name	Bits	Current RD–	Current RD+
	HGF EDCBA	abcdei fghj	abcdei fghj		HGF EDCBA	abcdei fghj	abcdei fghj
D0.2	010 00000	100111 0101	011000 0101	D0.3	011 00000	100111 0011	011000 1100
D1.2	010 00001	011101 0101	100010 0101	D1.3	011 00001	011101 0011	100010 1100
D2.2	010 00010	101101 0101	010010 0101	D2.3	011 00010	101101 0011	010010 1100
D3.2	010 00011	110001 0101	110001 0101	D3.3	011 00011	110001 1100	110001 0011
D4.2	010 00100	110101 0101	001010 0101	D4.3	011 00100	110101 0011	001010 1100
D5.2	010 00101	101001 0101	101001 0101	D5.3	011 00101	101001 1100	101001 0011
D6.2	010 00110	011001 0101	011001 0101	D6.3	011 00110	011001 1100	011001 0011
D7.2	010 00111	111000 0101	000111 0101	D7.3	011 00111	111000 1100	000111 0011
D8.2	010 01000	111001 0101	000110 0101	D8.3	011 01000	111001 0011	000110 1100
D9.2	010 01001	100101 0101	100101 0101	D9.3	011 01001	100101 1100	100101 0011
D10.2	010 01010	010101 0101	010101 0101	D10.3	011 01010	010101 1100	010101 0011
D11.2	010 01011	110100 0101	110100 0101	D11.3	011 01011	110100 1100	110100 0011
D12.2	010 01100	001101 0101	001101 0101	D12.3	011 01100	001101 1100	001101 0011
D13.2	010 01101	101100 0101	101100 0101	D13.3	011 01101	101100 1100	101100 0011
D14.2	010 01110	011100 0101	011100 0101	D14.3	011 01110	011100 1100	011100 0011
D15.2	010 01111	010111 0101	101000 0101	D15.3	011 01111	010111 0011	101000 1100
D16.2	010 10000	011011 0101	100100 0101	D16.3	011 10000	011011 0011	100100 1100
D17.2	010 10001	100011 0101	100011 0101	D17.3	011 10001	100011 1100	100011 0011
D18.2	010 10010	010011 0101	010011 0101	D18.3	011 10010	010011 1100	010011 0011
D19.2	010 10011	110010 0101	110010 0101	D19.3	011 10011	110010 1100	110010 0011
D20.2	010 10100	001011 0101	001011 0101	D20.3	011 10100	001011 1100	001011 0011
D21.2	010 10101	101010 0101	101010 0101	D21.3	011 10101	101010 1100	101010 0011
D22.2	010 10110	011010 0101	011010 0101	D22.3	011 10110	011010 1100	011010 0011
D23.2	010 10111	111010 0101	000101 0101	D23.3	011 10111	111010 0011	000101 1100
D24.2	010 11000	110011 0101	001100 0101	D24.3	011 11000	110011 0011	001100 1100
D25.2	010 11001	100110 0101	100110 0101	D25.3	011 11001	100110 1100	100110 0011
D26.2	010 11010	010110 0101	010110 0101	D26.3	011 11010	010110 1100	010110 0011
D27.2	010 11011	110110 0101	001001 0101	D27.3	011 11011	110110 0011	001001 1100
D28.2	010 11100	001110 0101	001110 0101	D28.3	011 11100	001110 1100	001110 0011
D29.2	010 11101	101110 0101	010001 0101	D29.3	011 11101	101110 0011	010001 1100
D30.2	010 11110	011110 0101	100001 0101	D30.3	011 11110	011110 0011	100001 1100
D31.2	010 11111	101011 0101	010100 0101	D31.3	011 11111	101011 0011	010100 1100

Table 11. Valid Data Characters (*MODE 1* and *MODE 3*) (continued)

Data Byte Name	Bits	Current RD–	Current RD+	Data Byte Name	Bits	Current RD–	Current RD+
	HGF EDCBA	abcdei fghj	abcdei fghj		HGF EDCBA	abcdei fghj	abcdei fghj
D0.4	100 00000	100111 0010	011000 1101	D0.5	101 00000	100111 1010	011000 1010
D1.4	100 00001	011101 0010	100010 1101	D1.5	101 00001	011101 1010	100010 1010
D2.4	100 00010	101101 0010	010010 1101	D2.5	101 00010	101101 1010	010010 1010
D3.4	100 00011	110001 1101	110001 0010	D3.5	101 00011	110001 1010	110001 1010
D4.4	100 00100	110101 0010	001010 1101	D4.5	101 00100	110101 1010	001010 1010
D5.4	100 00101	101001 1101	101001 0010	D5.5	101 00101	101001 1010	101001 1010
D6.4	100 00110	011001 1101	011001 0010	D6.5	101 00110	011001 1010	011001 1010
D7.4	100 00111	111000 1101	000111 0010	D7.5	101 00111	111000 1010	000111 1010
D8.4	100 01000	111001 0010	000110 1101	D8.5	101 01000	111001 1010	000110 1010
D9.4	100 01001	100101 1101	100101 0010	D9.5	101 01001	100101 1010	100101 1010
D10.4	100 01010	010101 1101	010101 0010	D10.5	101 01010	010101 1010	010101 1010
D11.4	100 01011	110100 1101	110100 0010	D11.5	101 01011	110100 1010	110100 1010
D12.4	100 01100	001101 1101	001101 0010	D12.5	101 01100	001101 1010	001101 1010
D13.4	100 01101	101100 1101	101100 0010	D13.5	101 01101	101100 1010	101100 1010
D14.4	100 01110	011100 1101	011100 0010	D14.5	101 01110	011100 1010	011100 1010
D15.4	100 01111	010111 0010	101000 1101	D15.5	101 01111	010111 1010	101000 1010
D16.4	100 10000	011011 0010	100100 1101	D16.5	101 10000	011011 1010	100100 1010
D17.4	100 10001	100011 1101	100011 0010	D17.5	101 10001	100011 1010	100011 1010
D18.4	100 10010	010011 1101	010011 0010	D18.5	101 10010	010011 1010	010011 1010
D19.4	100 10011	110010 1101	110010 0010	D19.5	101 10011	110010 1010	110010 1010
D20.4	100 10100	001011 1101	001011 0010	D20.5	101 10100	001011 1010	001011 1010
D21.4	100 10101	101010 1101	101010 0010	D21.5	101 10101	101010 1010	101010 1010
D22.4	100 10110	011010 1101	011010 0010	D22.5	101 10110	011010 1010	011010 1010
D23.4	100 10111	111010 0010	000101 1101	D23.5	101 10111	111010 1010	000101 1010
D24.4	100 11000	110011 0010	001100 1101	D24.5	101 11000	110011 1010	001100 1010
D25.4	100 11001	100110 1101	100110 0010	D25.5	101 11001	100110 1010	100110 1010
D26.4	100 11010	010110 1101	010110 0010	D26.5	101 11010	010110 1010	010110 1010
D27.4	100 11011	110110 0010	001001 1101	D27.5	101 11011	110110 1010	001001 1010
D28.4	100 11100	001110 1101	001110 0010	D28.5	101 11100	001110 1010	001110 1010
D29.4	100 11101	101110 0010	010001 1101	D29.5	101 11101	101110 1010	010001 1010
D30.4	100 11110	011110 0010	100001 1101	D30.5	101 11110	011110 1010	100001 1010
D31.4	100 11111	101011 0010	010100 1101	D31.5	101 11111	101011 1010	010100 1010

Table 11. Valid Data Characters (*MODE 1* and *MODE 3*) (continued)

Data Byte Name	Bits	Current RD–	Current RD+	Data Byte Name	Bits	Current RD–	Current RD+
	HGF EDCBA	abcdei fghj	abcdei fghj		HGF EDCBA	abcdei fghj	abcdei fghj
D0.6	110 00000	100111 0110	011000 0110	D0.7	111 00000	100111 0001	011000 1110
D1.6	110 00001	011101 0110	100010 0110	D1.7	111 00001	011101 0001	100010 1110
D2.6	110 00010	101101 0110	010010 0110	D2.7	111 00010	101101 0001	010010 1110
D3.6	110 00011	110001 0110	110001 0110	D3.7	111 00011	110001 1110	110001 0001
D4.6	110 00100	110101 0110	001010 0110	D4.7	111 00100	110101 0001	001010 1110
D5.6	110 00101	101001 0110	101001 0110	D5.7	111 00101	101001 1110	101001 0001
D6.6	110 00110	011001 0110	011001 0110	D6.7	111 00110	011001 1110	011001 0001
D7.6	110 00111	111000 0110	000111 0110	D7.7	111 00111	111000 1110	000111 0001
D8.6	110 01000	111001 0110	000110 0110	D8.7	111 01000	111001 0001	000110 1110
D9.6	110 01001	100101 0110	100101 0110	D9.7	111 01001	100101 1110	100101 0001
D10.6	110 01010	010101 0110	010101 0110	D10.7	111 01010	010101 1110	010101 0001
D11.6	110 01011	110100 0110	110100 0110	D11.7	111 01011	110100 1110	110100 1000
D12.6	110 01100	001101 0110	001101 0110	D12.7	111 01100	001101 1110	001101 0001
D13.6	110 01101	101100 0110	101100 0110	D13.7	111 01101	101100 1110	101100 1000
D14.6	110 01110	011100 0110	011100 0110	D14.7	111 01110	011100 1110	011100 1000
D15.6	110 01111	010111 0110	101000 0110	D15.7	111 01111	010111 0001	101000 1110
D16.6	110 10000	011011 0110	100100 0110	D16.7	111 10000	011011 0001	100100 1110
D17.6	110 10001	100011 0110	100011 0110	D17.7	111 10001	100011 0111	100011 0001
D18.6	110 10010	010011 0110	010011 0110	D18.7	111 10010	010011 0111	010011 0001
D19.6	110 10011	110010 0110	110010 0110	D19.7	111 10011	110010 1110	110010 0001
D20.6	110 10100	001011 0110	001011 0110	D20.7	111 10100	001011 0111	001011 0001
D21.6	110 10101	101010 0110	101010 0110	D21.7	111 10101	101010 1110	101010 0001
D22.6	110 10110	011010 0110	011010 0110	D22.7	111 10110	011010 1110	011010 0001
D23.6	110 10111	111010 0110	000101 0110	D23.7	111 10111	111010 0001	000101 1110
D24.6	110 11000	110011 0110	001100 0110	D24.7	111 11000	110011 0001	001100 1110
D25.6	110 11001	100110 0110	100110 0110	D25.7	111 11001	100110 1110	100110 0001
D26.6	110 11010	010110 0110	010110 0110	D26.7	111 11010	010110 1110	010110 0001
D27.6	110 11011	110110 0110	001001 0110	D27.7	111 11011	110110 0001	001001 1110
D28.6	110 11100	001110 0110	001110 0110	D28.7	111 11100	001110 1110	001110 0001
D29.6	110 11101	101110 0110	010001 0110	D29.7	111 11101	101110 0001	010001 1110
D30.6	110 11110	011110 0110	100001 0110	D30.7	111 11110	011110 0001	100001 1110
D31.6	110 11111	101011 0110	010100 0110	D31.7	111 11111	101011 0001	010100 1110

Table 12. Valid Special Code-Groups (*MODE 1* and *MODE 3*)

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD -	Current RD +	Notes
			abcdei fghj	abcdei fghj	
K28.0	1C	000 11100	001111 0100	110000 1011	15
K28.1	3C	001 11100	001111 1001	110000 0110	15, 16
K28.2	5C	010 11100	001111 0101	110000 1010	15
K28.3	7C	011 11100	001111 0011	110000 1100	15
K28.4	9C	100 11100	001111 0010	110000 1101	15
K28.5	BC	101 11100	001111 1010	110000 0101	16
K28.6	DC	110 11100	001111 0110	110000 1001	15
K28.7	FC	111 11100	001111 1000	110000 0111	15, 16
K23.7	F7	111 10111	111010 1000	000101 0111	
K27.7	FB	111 11011	110110 1000	001001 0111	
K29.7	FD	111 11101	101110 1000	010001 0111	
K30.7	FE	111 11110	011110 1000	100001 0111	

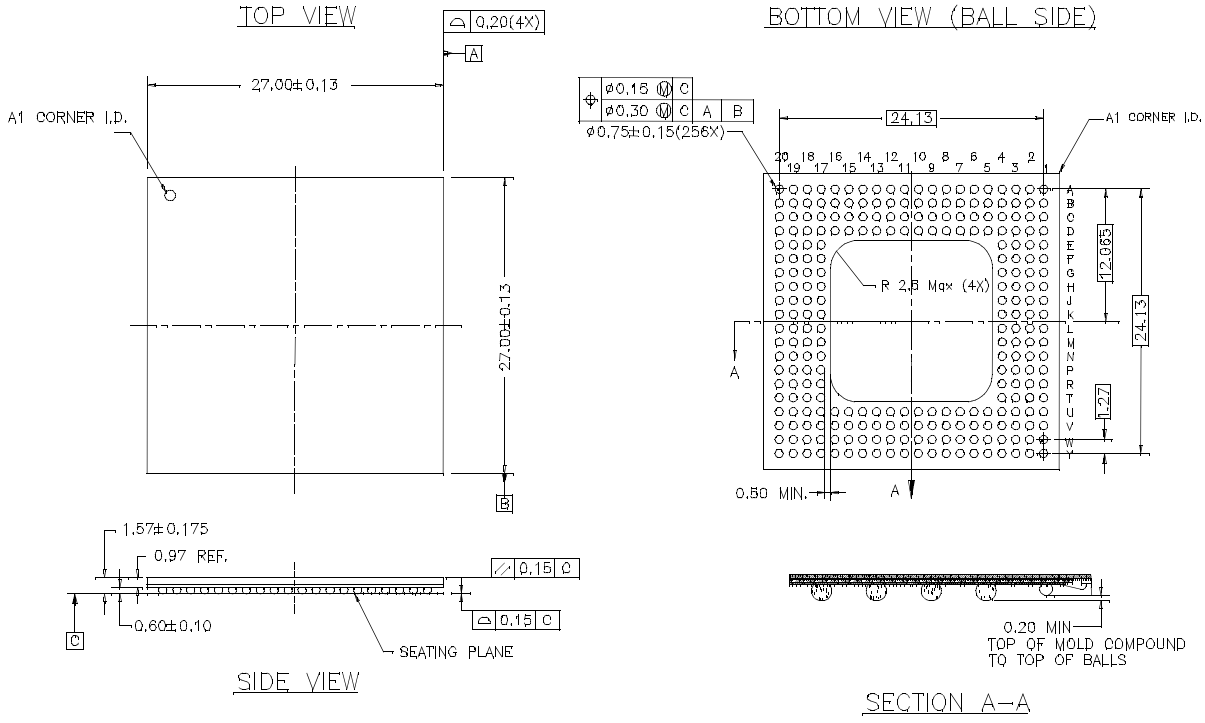
Notes:
15. Reserved.
16. Contains a COMMA.

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
Standard	CYP32G0401DX-BGC	256 L2BGA	256-Ball Thermally Enhanced Ball Grid Array	Commercial
Standard	CYP32G0401DX-BGI	256 L2BGA	256-Ball Thermally Enhanced Ball Grid Array	Industrial

Package Diagram

256-Lead L2 Ball Grid Array (27 x 27 x 1.57 mm) BL256



51-85123-*C

Document Title: CYP32G0401DX Multi-Gigabit Multi-Mode Quad HOTLink-III (TM) Transceiver (Preliminary) Document Number: 38-02019				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107382	06/19/01	KBN	New Data Sheet
*A	108153	07/17/01	KBN	Changed 256 BGA package diagram to 256 L2BGA (#51-85123) Minor rewording of Features section
*B	110119	09/26/01	GHW	Added Functional Description, Block Level Diagram, Pin Descriptions, Electrical Parameters, Waveforms, 8B/10B Codes, Switching Parameters Advance to Preliminary
*C	111408	11/09/01	EK	Reduced Static Discharge Voltage maximum rating to 500V