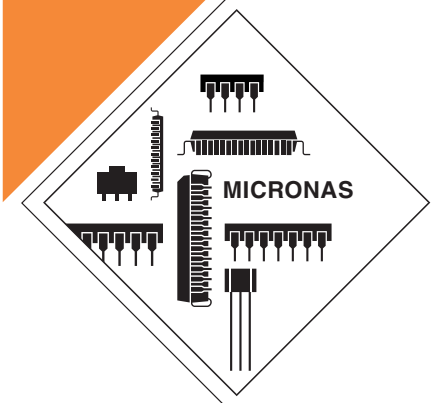


PRELIMINARY DATA SHEET

MAD 4868A
Micronas Audio Delay

Edition May 11, 2004
6251-636-1PD

MICRONAS

Contents

Micronas Audio Delay

1. Introduction

The Micronas Audio Delay IC MAD 4868A acts as a delay line for TV audio and consumer audio applications. The IC is designed for synchronizing audio and video signals ensuring “Lip Sync” by delaying the audio signal with the same amount of time as the video signal is delayed in a TV’s video processing.

For TV designs, independent signals for loudspeakers, headphones, and line-out or S/PDIF out must be provided, resulting in the need to delay six independent audio channels.

Especially modern flat panel TVs (LCD- or plasma-TVs) require “Lip Sync” because of their video deinterlacing, processing, scaling, and pixel-oriented display.

In battery-operated “wireless TVs” using digital transmission, the compression/decompression also may delay video more than audio. Therefore, additional audio delay is necessary.

Consumer audio applications such as A/V-Receivers or HTiB can also use MAD 4868A to offer “Lip Sync” as an additional feature to delay audio according to the video delay appearing in the TV, beamer, or monitor used in a home cinema setup.

The MAD 4868A is equipped with all interfaces, as well as embedded RAM. This makes the IC easy to use and avoids RAM availability and pricing problems.

In its PMQFP44-1 package with 0.8 mm pitch, the MAD 4868A requires only little PCB space but is suitable for wave soldering and reflow soldering.

1.1. Features

- 32 k audio samples RAM:
  Total delay time of 680 ms at 48 kHz or
  1020 ms at 32 kHz sampling rate
- 32/18-bit word width:
  32-bit High-Resolution mode or
  18-bit Standard mode
- Sampling rates from 32 kHz to 48 kHz for serial 8-channel mode are supported
- Sampling rates from 4 kHz to 192 kHz for parallel 2-channel mode are supported
- Memory allocation:
  MAD 4868A’s memory can be allocated for 1…8 audio channels. Delay time can be programmed for each channel individually.

1.2. Interfaces

- 8-channel Micronas I^2S input and output:
  In combination with Micronas ICs (serial mode) (e.g. MSP 44/46xyK, MAS 35xyH), eight audio channels can be routed through MAD 4868A by using four lines only.
- 4×2-channel standard I^2S inputs and outputs (parallel mode) allow routing eight audio channels with sampling rates of 4…192 kHz through MAD 4868A
- I^2C control for delay time programming
- Address select to set one out of two available I^2C addresses

1.3. Miscellaneous

- No crystal required:
  The MAD 4868A derives all internal clocks from the I^2S clock.
- Very few external components required
- 5 V or 3.3 V single supply voltage
- Very low power consumption
- 5 kHz to 192 kHz sampling rates
- Cascadable, extendable:
  Two MAD 4868As can be cascaded to extend the delay time, either in 8-channel (serial) mode using one data line or in 2-channel (parallel) mode using up to four data lines.

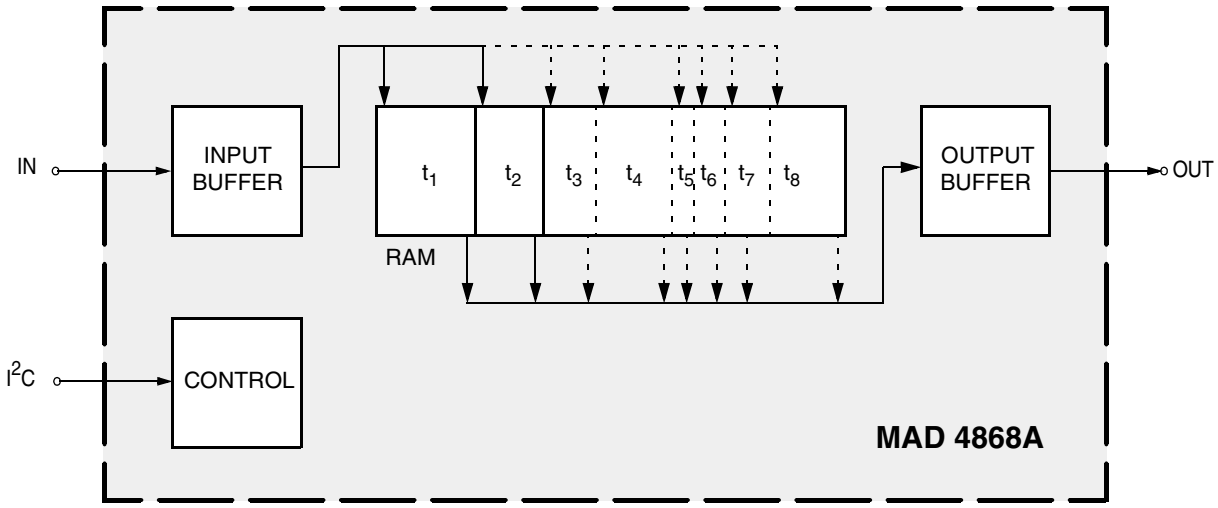


Fig. 1–1: Block diagram of the MAD 4868A

2. Functional Description

2.1. Block Diagram

In Fig. 2–1, a simplified block diagram of the IC is given. Between 1 and 8 channels can be delayed individually by a programmable number of samples n_x. The delay RAM offers, depending on the accumulated adjusted delay, a word width of 32 or 18 bits.

The accumulated delay must not exceed $7FF0_{hex}$ (32752_{dec}) samples (i.e. 682 ms @ 48 kHz F_s). As the bit clock (I2S_DEL_CL) is limited to 12.288 MHz and the used I^2S bus format has a fixed word length of 32 bit, the maximum sample rate f_s is 192 kHz in parallel mode (2-channels per data line) and 48 kHz in serial mode (8-channels on I2S_DEL_IN1/OUT1).

2.2. I^2S Bus Interface

The MAD 4868A has four I^2S data input lines and four I^2S data output lines which together with I2S_DEL_WS and I2S_DEL_CL form one I^2S bus interface for various sample rates in serial (8-channel) or parallel (2-channel) mode. The I2S_DEL_CL, I2S_DEL_WS, and I2S_DEL_IN1...4 are inputs to the MAD 4868A (tristate) while I2S_DEL_OUT1...4 are outputs. Bit[1:0] of the CONTROL register set the output driver active or tristate and its strength to weak or strong (see Table 3–3 on page 10). The interface works only in synchronous slave mode and with a fixed wordlength of each audio sample of 32 bits. Two different operational modes can be adjusted as described in the following sections.

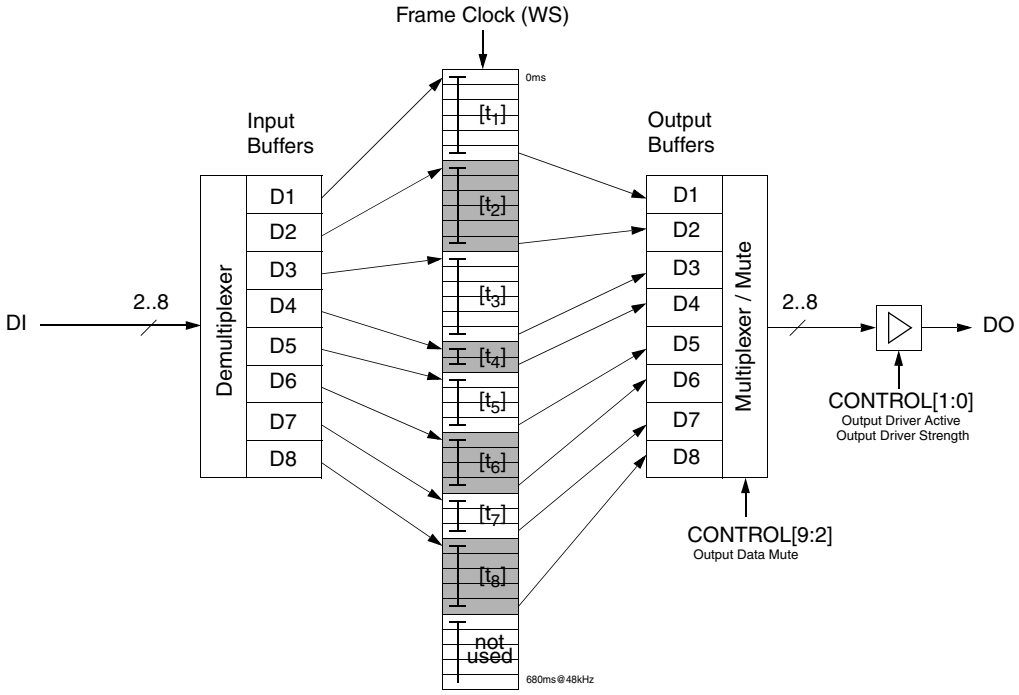


Fig. 2–1: Simplified block diagram of the MAD 4868A

2.2.1. Serial Mode - One Data Line

The MAD 4868A is capable of receiving signals with up to eight audio samples in a fixed 8-channel I^2S format on one data line (serial mode). The interface consists of the pins:

– I2S_DEL_IN1:
I^2S data input, with 8 audio channels per I2S_DEL_WS cycle and 32 bit per audio sample

– I2S_DEL_OUT1:
I^2S data output, with 8 audio channels per I2S_DEL_WS cycle and 32 bit per audio sample

– I2S_DEL_CL:
I^2S clock

– I2S_DEL_WS:
I^2S word strobe signal defines the frame start at the sample rate.

As the bit clock must not exceed 12.288 MHz, the maximum sample rate is limited to 48 kHz when the MAD 4868A is operated in this mode. This mode is used for the connection to the Delay Line Interface of the MSP 44/46xyK. In serial mode, the number of audio channels must be even and less or equal eight. A timing diagram is shown in Fig. 4–8 on page 21. In this mode, it is possible to mute each output channel individually by means of the CONTROL register bit[2:9.]

Note: DVSUP2 drives the pins DA_IN_2...4 and DA_OUT_2...4. To avoid radiation from not connected pins, it is recommended not to connect DVSUP2 when MAD 4868A is to be used in Serial Mode.

2.2.2. Parallel Mode - Four Data Lines

The MAD 4868A is capable of receiving stereo signals on up to four I^2S data lines in Parallel Mode with a total of up to eight audio channels. The interface consists of the pins:

– I2S_DEL_IN1, I2S_DEL_IN2, I2S_DEL_IN3, I2S_DEL_IN4:
I^2S data input with 2 audio channels per I2S_DEL_WS cycle and 32 bit per audio sample

– I2S_DEL_OUT1, I2S_DEL_OUT2, I2S_DEL_OUT3, I2S_DEL_OUT4:
I^2S data output with 2 audio channels per I2S_DEL_WS cycle and 32 bit per audio sample

– I2S_DEL_CL:
I^2S clock

– I2S_DEL_WS:
I^2S word strobe signal defines the left and right sample at the sample rate.

As the bit clock must not exceed 12.288 MHz, the sample rate can be a maximum of 192 kHz when MAD 4868A is operated in this mode. This mode is used for connection to e.g. the I^2S interface of the Micronas MSP 34/44xyG or any other audio DSP.

2.3. Delay Line

The MAD 4868A has a delay line of 32k Words of RAM built in. The RAM can be split up into portions of different length to delay between 1 and 8 channels of audio. This makes the MAD 4868A very flexible. All channels can be delayed individually. The maximum amount of adjusted delay must not exceed $7FF0_{hex}$ (32752_{dec}) samples.

Equipped with a pointer unit and programmed with variable pointer offsets for the delay channels 1 to 8, the programming of the individual delay times is realized by means of its own control register for each delay channel (see Table 3–3 on page 10).

The delay time depends on the used sample frequency on the I²S-bus. Since, not the delay time, but the number of delayed samples is programmed, the corresponding number of samples is calculated using the follwing formula:

$$n_x = (t_{ms}(x) \times f_s) - 1$$

n_x = number of samples
t_{ms} = time in milliseconds
f_s = sample rate

In the pointer unit, the offsets are used as increments for the address pointer to receive the correct RAM address of the delayed sound samples.

Note: Reprogramming the delay length of a channel affects the output of the channels with higher numbers. Due to the “linked list” principle of the RAM organisation, the upper channels read from “wrong memory” until it is filled up with new audio samples. Therefore, it is recommended to mute the output of the delay line for the max programmed delay time of all channels.

2.4. Word Width

The audio sample word width inside the RAM of the MAD 4868A depends on the adjusted number of samples for the delay. MAD 4868A automatically switches the word width to 32 bit if the total delay length is below $3FF8_{hex}$ (16376_{dec}) i.e. half of the maximum length. Otherwise, the delay line is 18 bit wide. By means of bit[14] of the CONTROL register, a read out value is available in parallel mode which indicates the internally adjusted word width.

2.5. Output Data Mute

The output data channel 1-8 can be muted by means of the CONTROL register bit[2:9]. In serial mode, each output data channel can be muted individually, while in parallel mode, all channels 1-8 have to be adjusted individually to the same value. It is recommended to mute the output data channels during the power-up sequence of the MAD 4868A, as well as during readjustment of the delay time during normal operation. To avoid any audible disturbances, the minimum mute time must be at least the maximum programmed delay time of all channels.

2.6. Reset

The Reset is active low and resets the I²S and I²C-interfaces of the MAD 4868A. Since there is no RAM clear facility, the output of the MAD 4868A after reset is random, as long as no valid samples have been inserted and passed the delay line (e.g. after Reset, enable the I²S bus output but keep Mute active until the maximum programmed delay time is passed).

2.7. RAM Clear

A RAM Clear can be performed manually. It is recommended to apply a manual RAM Clear after the power-up of the MAD 4868A. Mute the output data channel 1-8, apply a digital zero signal on all used channels. This can be achieved, for example, by selecting an I²S input with a prescaler setting to Mute in the MSP 44/46xyK for all used MAD 4868A input channels. The digital zero signal must be applied for at least the maximum programmed delay time of all channels.

3. Control Interface

3.1. I²C Bus Interface

The MAD 4868A is controlled via its I²C bus slave interface.

The IC is selected by transmitting an MAD 4868A device address. In order to allow two MAD 4868A ICs to be connected to a single bus, an address select pin (ADR_SEL) has been implemented. With ADR_SEL pulled to high or low, the MAD 4868A responds to different device addresses. A device address pair is defined as a write address and a read address.

Writing is done by sending the write device address, followed by the subaddress byte and the data bytes.

Reading is done by sending the write device address, followed by the subaddress byte. Without sending a stop condition, reading of the addressed data is completed by sending the device read address and reading two bytes of data.

See Table 3–1 for a list of available device addresses.

See Table 3–2 for a list of available subaddresses.

A general timing diagram of the I²C bus is shown in Fig. 3–1 on page 9.

Table 3–1: I²C Bus Device Addresses

ADR_SEL	Low (connected to DVSS)		High (connected to DVSUP)	
Mode	**Write**	**Read**	**Write**	**Read**
MAD 4868A device address	82_{hex}	83_{hex}	84_{hex}	85_{hex}

Table 3–2: I²C Bus Subaddresses

Name	Binary Value	Hex Value	Mode	Function
CONTROL	0000 0000	00	Read / Write	Write: Interface control Read: Status
CH1_DELAY	0000 0001	01	Read / Write	delay channel 1
CH2_DELAY	0000 0010	02	Read / Write	delay channel 2
CH3_DELAY	0000 0011	03	Read / Write	delay channel 3
CH4_DELAY	0000 0100	04	Read / Write	delay channel 4
CH5_DELAY	0000 0101	05	Read / Write	delay channel 5
CH6_DELAY	0000 0110	06	Read / Write	delay channel 6
CH7_DELAY	0000 0111	07	Read / Write	delay channel 7
CH8_DELAY	0000 1000	08	Read / Write	delay channel 8

3.1.1. Protocol Description

Write to CONTROL and CHX_DELAY Registers

S	write device address	Wait	ACK	sub-addr	ACK	data-byte high	ACK	data-byte low	ACK	P

Read from CONTROL or CHX_DELAY Register

S	write device address	Wait	ACK	sub-addr	ACK	S	read device address	Wait	ACK	data-byte-high	ACK	data-byte low	NAK	P

Note: S = I^2C-Bus Start Condition from master
P = I^2C-Bus Stop Condition from master
ACK = Acknowledge-Bit: LOW on SDA from slave (= MAD, light gray) or master (= controller, dark gray)
NAK = Not Acknowledge-Bit: HIGH on I2C_DA from master (dark gray) to indicate 'End of Read' or from MAD indicating internal error state
Wait = I^2C-Clock line is held low, while the MAD is processing the I^2C command. This waiting time is max. 1 ms

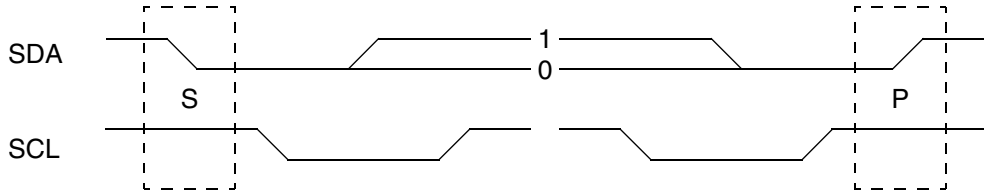


Fig. 3–1: I^2C bus protocol (MSB first; data must be stable while clock is high)

3.1.2. Start-Up Sequence: Power-Up and I^2C-Controlling

After POWER-ON or RESET, the IC is in an inactive state. All registers are in their Reset position (see Table 3–3 on page 10), the Output Driver is set to tristate. The controller has to initialize the CONTROL and CHX_DELAY registers.

3.2. Description of User Interface

Write and read registers are 16 bit wide, whereby the MSB is denoted bit[15]. Transmissions via I^2C bus have to take place in 16-bit words (two byte transfers, with the most significant byte transferred first). All registers are readable.

Unused parts of the 16-bit write registers must be zero. **Addresses not given in this table must not be accessed.**

Table 3–3: User Interface

Sub - Address (hex)	Function	Mode	Reset Value (hex)	Name
00_{hex}	**Control**		0000_{hex}	CONTROL
	bit[15]	must be ignored		
	bit[14][1)]	**HighRes Flag** (word width of delayed samples) 0 18 bit 1 32 bit (high resolution)		
	bit[13:11]	not used, must be set to 0		
	bit[10]	**WS_POL** (word strobe polarity) 0 WS_POL = Low-High marks Framestart e.g. MSP 44/46xyK I^2S-5 Interface, all MSPs 8-channel mode 1 WS_POL = High-Low marks Framestart e.g. MSP I2S_OUT (2-channel mode)		
	bit[9] bit[8] bit[7] bit[6] bit[5] bit[4] bit[3] bit[2]	**Output Data Mute channel 8** **Output Data Mute channel 7** **Output Data Mute channel 6** **Output Data Mute channel 5** **Output Data Mute channel 4** **Output Data Mute channel 3** **Output Data Mute channel 2** **Output Data Mute channel 1** 0 muted 1 0 dB Output Data Mute channel 1-8 can be set individually in serial mode, in parallel mode, Output Data Mute channel 1-8 must all be set to the same value.		
	bit[1]	**Output Driver Active** 0 tristate 1 active		
	bit[0]	**Output Driver Strength** 0 weak 1 strong		
	[1)] bit[14] is read only			

Table 3–3: User Interface, continued

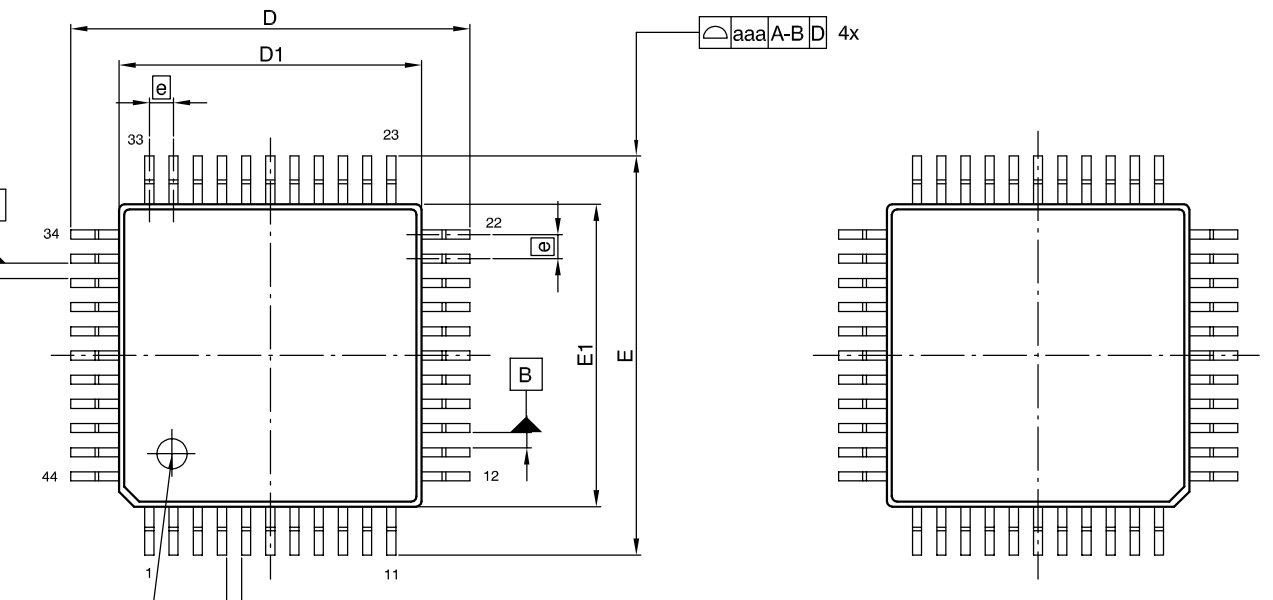
Sub - Address (hex)	Function	Mode	Reset Value (hex)	Name
01_{hex}... 08_{hex}	**Channel Delay** The delay time t_{ms} in milliseconds; Delay n_x must be calculated and set as number of samples: $n_x = (t_{ms}(x) \times f_s) - 1$ x = 1..8; n = 0..32752 bit[15:0] n_x number of delayed samples for channel x, x = 1...8		0000_{hex}	CH1_DELAY CH2_DELAY CH3_DELAY CH4_DELAY CH5_DELAY CH6_DELAY CH7_DELAY CH8_DELAY

example:		f_s =	f_s =	f_s =	f_s =
samples:	n_x	32 kHz	48 kHz	96 kHz	192 kHz
min delay	0	31 µs	21 µs	10 µs	5 µs
	$1F_{hex}$	1.00 ms	0.66 ms	0.33 ms	0.16 ms
	$2F_{hex}$	1.50 ms	1.00 ms	0.50 ms	0.25 ms
	$5F_{hex}$	3.00 ms	2.00 ms	1.00 ms	0.50 ms
	...				
max delay[1)]	$7FF0_{hex}$	1023 ms	682 ms	341 ms	170 ms

[1)] Since there are 32 KWords of RAM accessible, the SUM(n_1:n_8) must be less than $7FF0_{hex}$ (e.g. in total a maximum delay of 682 ms at a 48 kHz sample rate must not be exceeded).

4. Specifications

4.1. Outline Dimensions



UNIT	L2	Θ
mm	1.60	0°-7°

* does not include dambar protrusion of 0.08 max. per side

UNIT	A	A1	A2	aaa	b	Bd	c	CO	D	D1	E	E1	e	L	L1
mm	max 2.45	0.25 0.00	2.20 1.80	0.25	0.45 0.29	0.2	0.23 0.11	0.1	13.2	10.0	13.2	10.0	0.8	1.03 0.73	0.25

JEDEC STANDARD		ANSI	ISSUE DATE YY-MM-DD	DRAWING-NO.	SPZG-NO.
ISSUE	ITEM NO.				
B	MS-022		03-01-23	06599.0001.4	SPZG001003_001_02

Fig. 4–1:
PMQFP44-1: Plastic **M**etric **Q**uad **F**lat **P**ackage, **44** leads, 10 × 10 × 2 mm^3
Ordering code: QG
Weight approximately 0.5 g

4.2. Pin Connections and Short Descriptions

NC = not connected; leave vacant
LV = if not used, leave vacant
OBL = obligatory; connect as described in circuit diagram

Pin No. PMQFP44-1	Pin Name	Type	Connection (If not used)	Short Description
1...12	NC		LV	Not Connected
13	I2S_DEL_OUT2	OUT	OBL	I^2S data output channel 3 + 4
14	I2S_DEL_OUT3	OUT	OBL	I^2S data output channel 5 + 6
15	I2S_DEL_OUT4	OUT	OBL	I^2S data output channel 7 + 8
16	DVSUP2	SUP	DVSUP	Digital Power Supply
17	DVSS2	SUP	DVSS	Digital Ground
18	I2S_DEL_IN2	IN	OBL	I^2S data input channel 3 + 4
19	I2S_DEL_IN3	IN	OBL	I^2S data input channel 5 + 6
20	I2S_DEL_IN4	IN	OBL	I^2S data input channel 7 + 8
21...33	NC		LV	Not Connected
34	RESETQ	IN	OBL	Power-On Reset (active low)
35	TEST	IN	DVSS	Test pin
36	DVSS1	SUP	DVSS	Digital Ground
37	DVSUP1	SUP	DVSUP	Digital Power Supply
38	I2S_DEL_WS	IN	OBL	I^2S word strobe input
39	I2S_DEL_CL	IN	OBL	I^2S clock input
40	I2S_DEL_IN1	IN	OBL	I^2S data input channel 1 + 2 or 1..8
41	I2S_DEL_OUT1	OUT	OBL	I^2S data output channel 1 + 2 or 1..8
42	ADR_SEL	IN	OBL	I^2C bus address select
43	I2C_DA	IN/OUT	OBL	I^2C Data
44	I2C_CL	IN/OUT	OBL	I^2C Clock

4.3. Pin Descriptions

I2C_CL – I^2C Clock Input/Output (Fig. 4–3)
Via this pin, the I^2C-bus clock signal has to be supplied.

I2C_DA – I^2C Data Input/Output (Fig. 4–3)
Via this pin, the I^2C-bus data is written to or read.

I2S_DEL_WS – Word Strobe Input (Fig. 4–4)
Word strobe line for the I^2S bus. An external word strobe has to be supplied.

I2S_DEL_CL – Clock Input (Fig. 4–4)
Clock line for the I^2S bus. An external clock has to be supplied.

I2S_DEL_IN1, I2S_DEL_IN2, I2S_DEL_IN3, I2S_DEL_IN4 – Data Input (Fig. 4–4)
Input of I^2S data.

I2S_DEL_OUT1, I2S_DEL_OUT2, I2S_DEL_OUT3, I2S_DEL_OUT4 – Data Output (Fig. 4–5)
Output of I^2S bus.

DVSUP1, DVSUP2 – Digital Supply Voltage
Power supply must be connected to +5 V or +3.3 V power supply.

DVSS1, DVSS2 – Digital Ground
Ground connection.

TEST – This pin enables factory test modes. For normal operation, it must be connected to DVSS

RESETQ – Reset Input (Fig. 4–4)
In the steady state, high level is required. A low level resets the interfaces of MAD 4868A.

ADR_SEL – I^2C Bus Address Select (Fig. 4–4)
By means of this pin, one of two device addresses can be selected. The pin can be connected to DVSS (I^2C device addresses $82/83_{hex}$) or to DVSUP ($84/85_{hex}$).

NC – Pin not connected

4.4. Pin Configuration

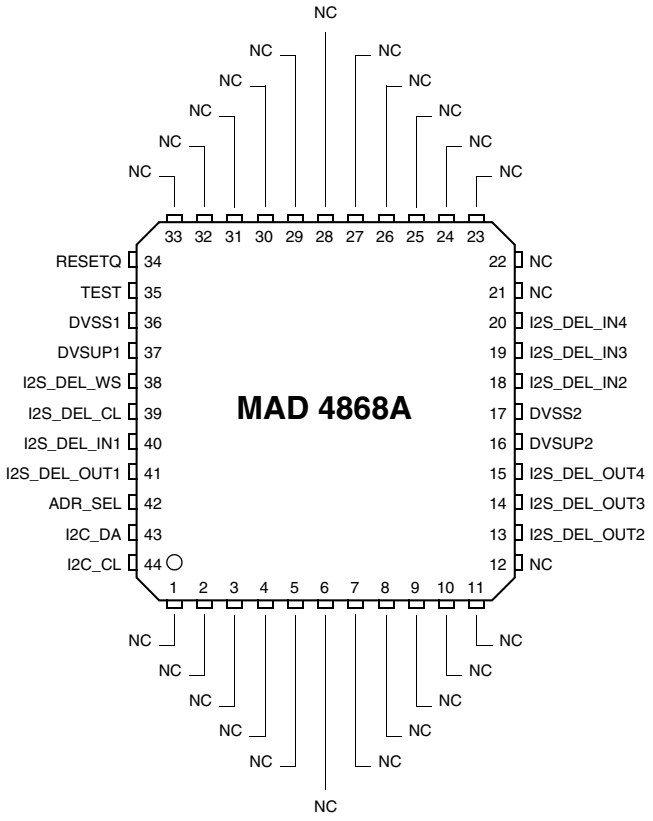


Fig. 4–2: PMQFP44-1 package

4.5. Pin Circuits

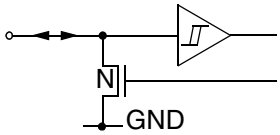


Fig. 4–3: Input/Output Pins: **I2C_CL, I2C_DA**

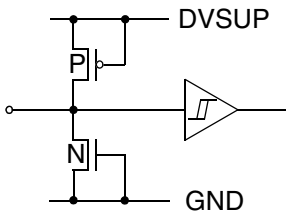


Fig. 4–4: Input Pins:**I2S_DEL_CL, I2S_DEL_WS, I2S_DEL_IN1, I2S_DEL_IN2, I2S_DEL_IN3, I2S_DEL_IN4, ADR_SEL, RESETQ**

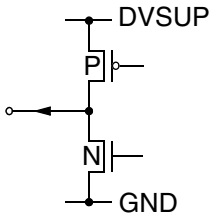


Fig. 4–5: Output Pins: **I2S_DEL_OUT1, I2S_DEL_OUT2, I2S_DEL_OUT3, I2S_DEL_OUT4**

4.6. Electrical Characteristics

Abbreviations:

tbd = to be defined
vacant = not applicable
positive current values mean current flowing into the chip

4.6.1. Absolute Maximum Ratings

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods will affect device reliability.

This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than absolute maximum-rated voltages to this high-impedance circuit.

All voltages listed are referenced to ground (V_{SS} = 0 V) except where noted.

All GND pins must be connected to a low-resistive ground plane close to the IC.

Table 4–1: Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Limit Values		Unit
			Min.	Max.	
T_A [1)]	Ambient Temperature	–	–10	70	°C
T_C	Case Temperature	–	–10	95	°C
T_S	Storage Temperature	–	–40	125	°C
P_{MAX}	Maximum Power Dissipation			860	mW
V_{SUP}	Supply Voltage	DVSUP1, DVSUP2	–0.3	6.0	V
V_{Idig}	Input Voltage, all Digital Inputs		–0.3	V_{SUP2}+0.3	V
I_{Idig}	Input Current, all Digital Pins	–	–20	+20	mA

1) Measured on standard board according to JESD 51 Standard with maximum power consumption allowed for this package.

4.6.2. Recommended Operating Conditions

Functional operation of the device beyond those indicated in the “Recommended Operating Conditions/Characteristics” is not implied and may result in unpredictable behavior, reduce reliability and lifetime of the device.

All voltages listed are referenced to ground (V_{SS} = 0 V) except where noted.

All GND pins must be connected to a low-resistive ground plane close to the IC.

Do not insert the device into a live socket. Instead, apply power by switching on the external power supply. For power up/down sequences, see the instructions in Section 4.6.3.3. of this document.

4.6.2.1. General Recommended Operating Conditions

Symbol	Parameter	Pin Name	Limit Values			Unit
			Min.	Typ.	Max.	
T_A	Ambient Operating Temperature	–	0		70	°C
T_C	Case Operating Temperature	–	0		70	°C
P_{MAX}	Maximum Power Dissipation				50	mW
V_{SUP}	Supply Voltage	DVSUP1, DVSUP2	3.0		5.25	V

4.6.3. Characteristics

For Min./Max. values: at T_A = 0 to 70 °C
V_{SUP} = 3.15 to 3.45 V if V_{SUP} = 3.3 V
V_{SUP} = 4.75 to 5.25 V if V_{SUP} = 5 V

For typical values: at T_A = 60 °C
V_{SUP} = 3.3 V or V_{SUP} = 5 V

4.6.3.1. General Characteristics

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Supply							
I_{SUP}	Supply Current (active) (VSUP = 5 V)	DVSUP1, DVSUP2		2.4 2.9 0.8		mA mA mA	Serial mode f_s = 48 kHz Parallel mode f_s 192 kHz Parallel mode f_s 48 kHz
	Supply Current (active) (VSUP = 3.3 V)			1.15 1.5 0.5		mA mA mA	Serial mode f_s = 48 kHz Parallel mode f_s 192 kHz Parallel mode f_s 48 kHz

4.6.3.2. Digital Inputs, Digital Outputs

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Digital Input Levels							
V_{DIGIL}	Digital Input Low Voltage	ADR_SEL			0.2	V_{SUP}	
V_{DIGIH}	Digital Input High Voltage		0.5			V_{SUP}	
Z_{DIGI}	Input Capacitance				5	pF	

4.6.3.3. Reset Input and Power-Up

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
RESETQ Input Levels							
V_{RHL}	Reset High-Low Transition Voltage	RESETQ			0.2	V_{SUP}	
V_{RLH}	Reset Low-High Transition Voltage		0.5			V_{SUP}	
Z_{RES}	Input Capacitance				5	pF	

4.6.3.4. I²C-Bus Characteristics

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
V_{I2CIL}	I²C-Bus Input Low Voltage	SCL, SDA			0.3	V_{SUP}	
V_{I2CIH}	I²C-Bus Input High Voltage		0.6			V_{SUP}	
t_{I2C1}	I²C Start Condition Setup Time		120			ns	
t_{I2C2}	I²C Stop Condition Setup Time		120			ns	
t_{I2C5}	I²C-Data Setup Time before Rising Edge of Clock		55			ns	
t_{I2C6}	I²C-Data Hold Time after Falling Edge of Clock		55			ns	
t_{I2C3}	I²C-Clock Low Pulse Time	SCL	500			ns	
t_{I2C4}	I²C-Clock High Pulse Time		500			ns	
f_{I2C}	I²C-BUS Frequency				1.0	MHz	
V_{I2COL}	I²C-Data Output Low Voltage	SCL, SDA			0.4	V	I_{I2COL} = 3 mA
I_{I2COH}	I²C-Data Output High Leakage Current				1.0	µA	V_{I2COH} = 5 V
t_{I2COL1}	I²C-Data Output Hold Time after Falling Edge of Clock		15			ns	
t_{I2COL2}	I²C-Data Output Setup Time before Rising Edge of Clock		100			ns	f_{I2C} = 1 MHz

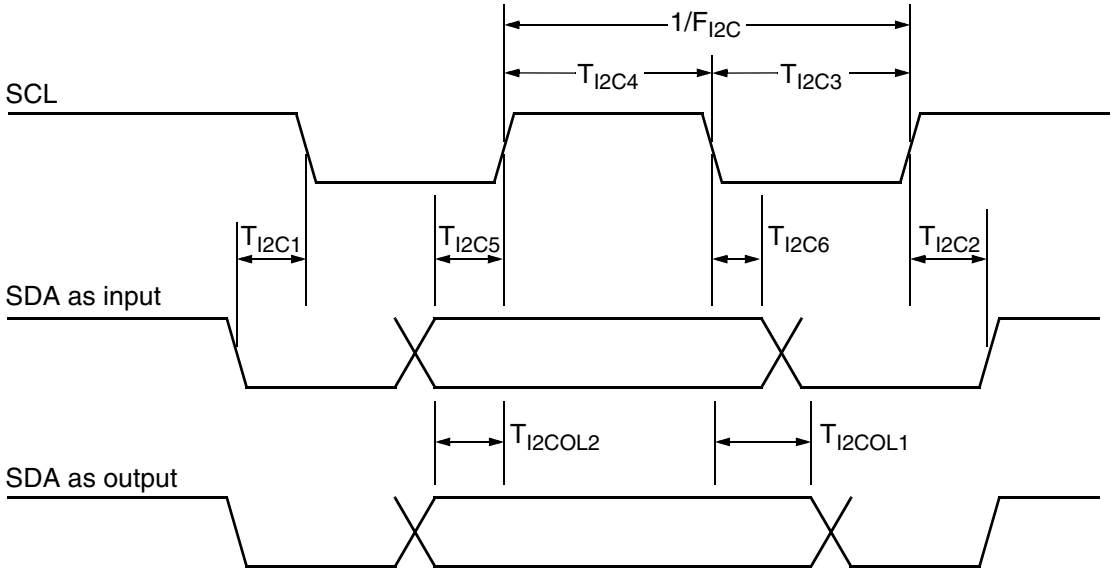
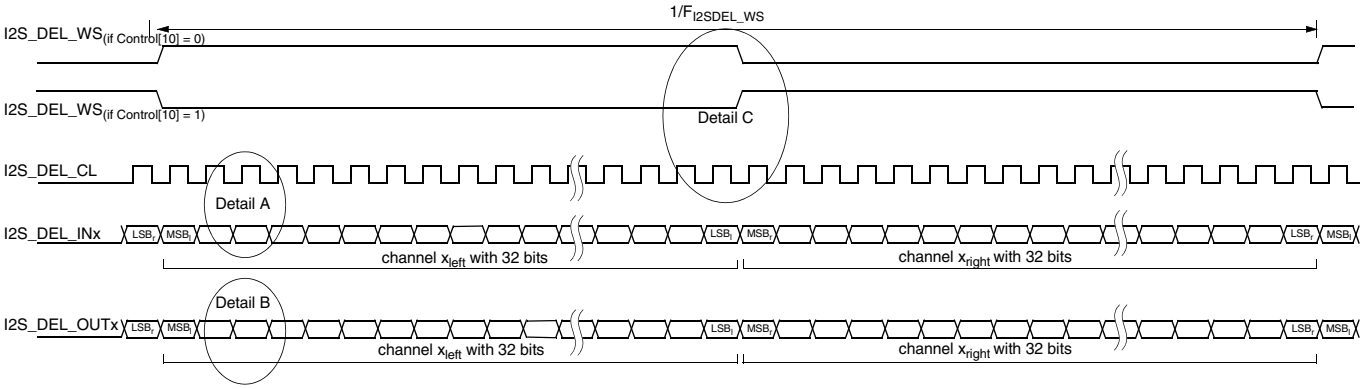


Fig. 4–6: I²C bus timing diagram

4.6.3.5. I^2S-Bus Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	I2S_DEL_CL I2S_DEL_WS I2S_DEL_IN1 I2S_DEL_IN2 I2S_DEL_IN3 I2S_DEL_IN4			0.2	V_{SUP}	
V_{IH}	Input High Voltage		0.5			V_{SUP}	
Z_I	Input Impedance				5	pF	
I_{LEAK}	Input Leakage Current		−1		1	µA	0 V < U_{INPUT}< DVSUP
V_{OL}	Output Low Voltage	I2S_DEL_OUT1, I2S_DEL_OUT2, I2S_DEL_OUT3, I2S_DEL_OUT4			0.4	V	I_{OL} = 1 mA
V_{OH}	Output High Voltage		V_{SUP} − 0.3			V	I_{OH} = −1 mA
I^2S Interface Parallel Mode 2-channel							
t_{s_I2SDEL}	Input Setup Time before Rising Edge of Clock	I2S_DEL_CL I2S_DEL_IN1, I2S_DEL_IN2, I2S_DEL_IN3, I2S_DEL_IN4	7			ns	for details see Fig. 4–8 "I^2S bus timing diagram, serial mode (8-channel)"
t_{h_I2SDEL}	Input Hold Time after Rising Edge of Clock		10			ns	
t_{d_I2SDEL}	Output Delay Time after Falling Edge of Clock	I2S_DEL_OUT1, I2S_DEL_OUT2, I2S_DEL_OUT3, I2S_DEL_OUT4			15	ns	C_L=30 pF
f_{I2SDEL_WS}	Word Strobe Input Frequency	WS	4		192	kHz	deviation = ±300 ppm
f_{I2SDEL_CL}	Clock Input Frequency	CL	0.256		12.288	MHz	deviation = ±300 ppm
R_{CL}	Clock Input Ratio		0.9		1.1		
I^2S Interface Serial Mode 8-channel							
t_{s_I2SDEL}	Input Setup Time before Rising Edge of Clock	I2S_DEL_CL I2S_DEL_WS I2S_DEL_IN1	7			ns	for details see Fig. 4–8 "I^2S bus timing diagram, serial mode (8-channel)"
t_{h_I2SDEL}	Input Hold Time after Rising Edge of Clock		10			ns	
t_{d_I2SDEL}	Output Delay Time after Falling Edge of Clock	I2S_DEL_OUT1,			15	ns	C_L=30 pF
f_{I2SDEL_WS}	Word Strobe Input Frequency	I2S_DEL_WS	4		48	kHz	
f_{I2SDEL_CL}	Clock Input Frequency	I2S_DEL_CL	1.024		12.288	MHz	
R_{CL}	Clock Input Ratio		0.9		1.1		



Detail A,B,C

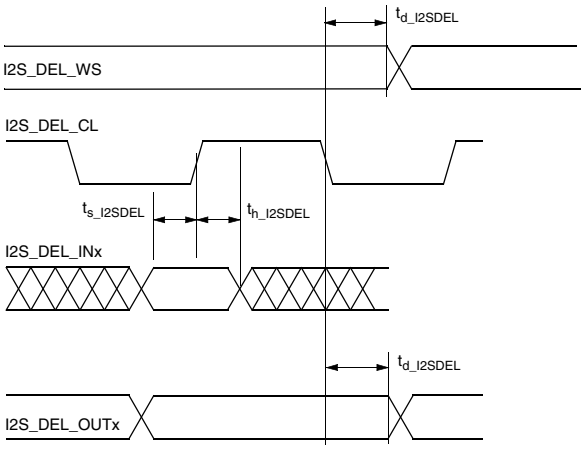
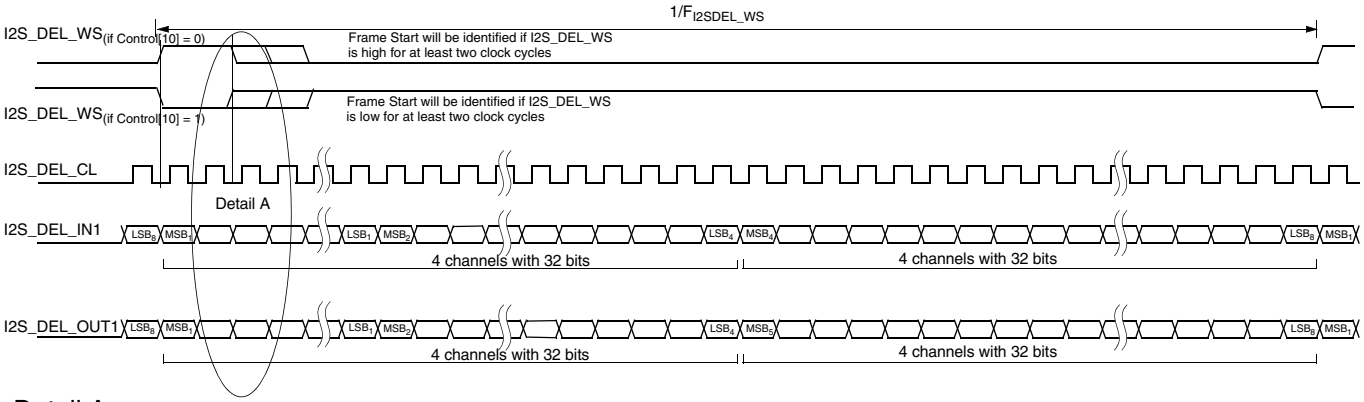


Fig. 4–7: I²S bus timing diagram, parallel mode (2-channel)



Detail A

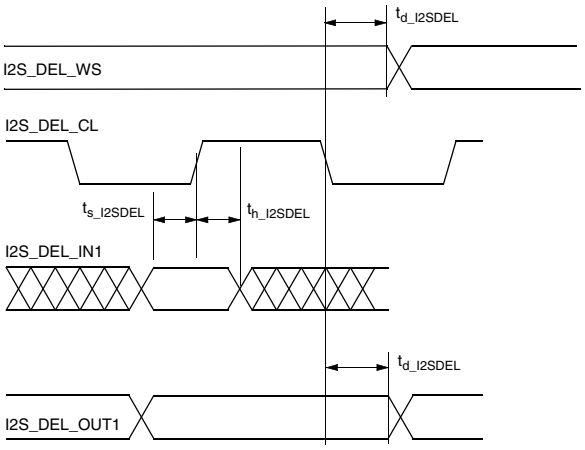
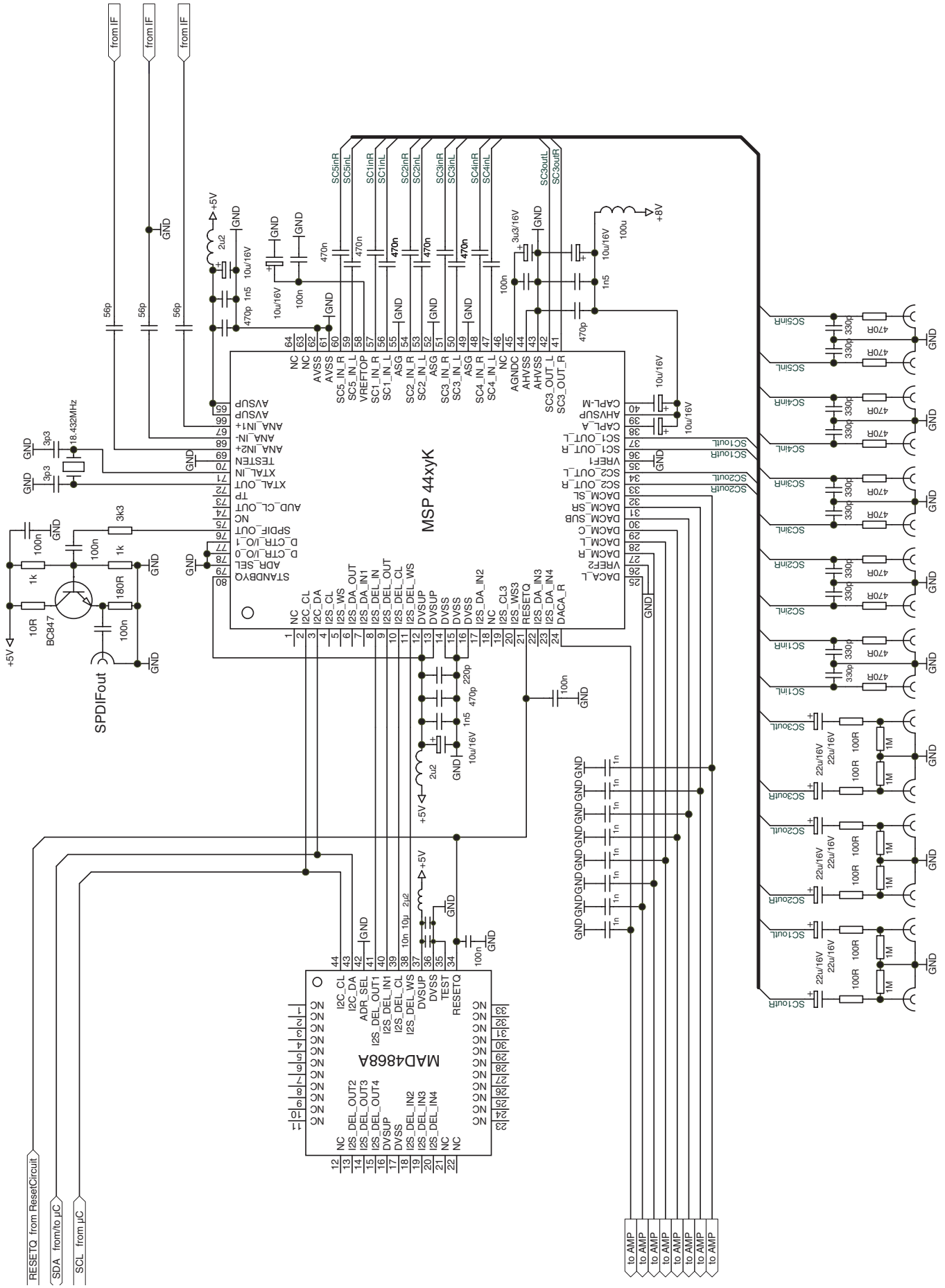


Fig. 4–8: I^2S bus timing diagram, serial mode (8-channel)

5. Appendix A: Application Diagram (Exemplary)



6. Data Sheet History

1. Preliminary Data Sheet: “MAD 4868A Micronas Audio Delay”, May 11, 2004, 6251-636-1PD. First release of the preliminary data sheet.

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