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Fiberoptic Postamplifier MC2045-2

Postamplifier/Quantiser for applications to 200Mbps

Main Features

- Low-cost IC, available as die or in SOIC16, TSSOP20 and QSOP16 packages. Fabricated in advanced sub-micron BiCMOS process.
- Pin-compatible, superior replacement for Signetics NE5224/5.
- SONET, FDDI, ESCON compatible.
- Programmable input-signal level detector.
- Fully differential. Input sensitivity better than 0.8mV at 155Mbps, permitting system sensitivities better than -38dBm (BER 10^{-9}).
- Fully supports 3.3V and 5V supplies.
- Differential PECL data and level detect outputs.

Ordering Information

Part Number	Pin Package
MC2045-2S16	SOIC16
MC2045-2T20	TSSOP20
MC2045-2Q16	QSOP16
MC2045-2DIEWP	Waffle Pack
MC2045-2WAFER	Expanded whole 8” on a 10” grip ring

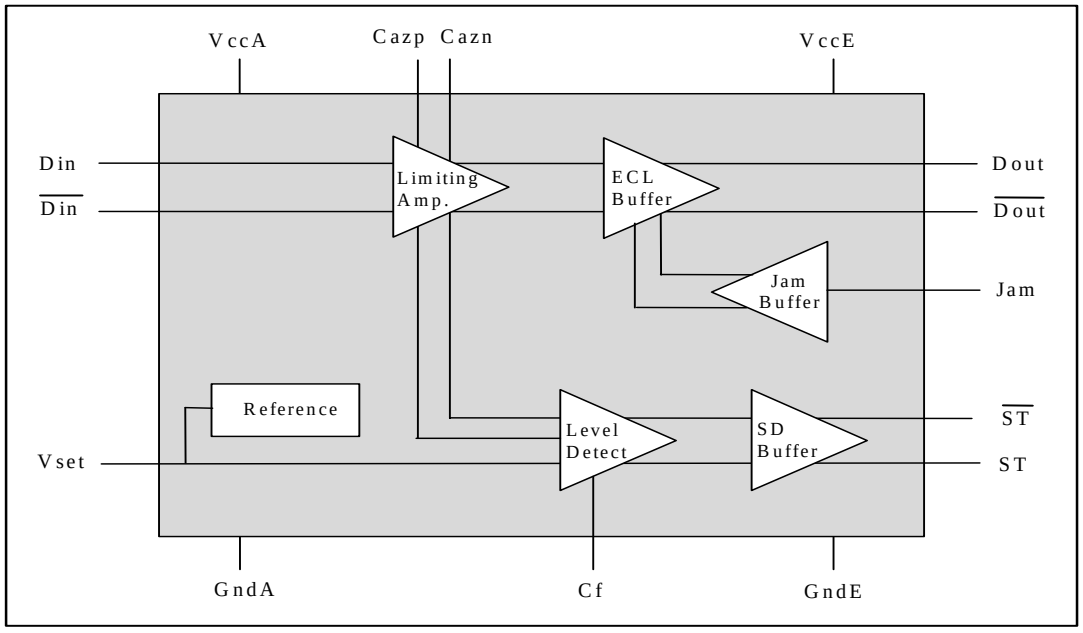
General Description

The MC2045-2 is a second-generation, high gain limiting amplifier intended for fiberoptics based communications to 200Mbps. Normally placed following the photodetector and transimpedance or pre-amplifier, the limiting amplifier provides the necessary gain to give ECL compatible logic outputs.

The MC2045 also includes a programmable signal-level detector, allowing the user to set thresholds at which the logic outputs are enabled.

Though capable of operating over a wide frequency range, the MC2045 has been optimised for 155/200Mbps OC-3/STM-1 and ESCON applications.

Note also the MC2044C for applications at 622Mbps and >1Gbps.



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
P_{TOT}	Total power dissipation (TSSOP20)	TBA	mW
V_{CC}	Power supply (V_{CC}-GND)	6	V
T_A	Operating ambient	-40 to +85	°C
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature	-65 to +150	°C

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Recommended Operating Conditions

Symbol	Parameter	Rating	Units
V_{CC}	Power supply (V_{CC}-GND)	3.0 to 5.5	V
T_A	Operating ambient	-40 to +85	°C

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V_{IN}	Input signal voltage[1] (D_{IN}) Single-ended: Differential:	0.8 1.6	-	400 800	mVp-p
V_{OS}	Input offset voltage	-	-	50	µV
V_N	Input RMS noise in 100MHz	-	-	85	µV
V_{TH}	Input level detect programmability	2	-	20	mVp-p
V_{HYS}	Level detect hysteresis (optical)	1.75	2.25	2.75	dB
I_{INL}	JAM input current (at 0V)	-10	-	10	µA
I_{CC}	Supply current (no ECL loads)	-	-	35	mA

AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units
BW	Bandwidth: Lower -3dB point Upper -3dB point	1.5	-	 100	KHz MHz
R_{IN}	Input resistance	-	4.5	-	kΩ
C_{IN}	Input capacitance	-	-	2	pF
T_{PWD}	Pulse Width Distortion	-	-	0.3	ns
T_R,T_F	ECL out rise/fall times (20-80% points)	-	1.0	2.0	ns
R_F	Level detect filter resistance	14	25	41	kΩ
T_{LD}	Level detect time constant	0.5	1	2.0	µs

❑

[1] **0.8mV is worst case sensitivity @BER10-9**

Pin Descriptions[1]

Name	Function	SOIC16 / QSOP16 Pin #	Die Bond #	TSSOP20 Pin #
C_{AZN}	Auto-zero capacitor pin. Connect C_{AZ} between this pin and C_{AZP}.	1	1	1
C_{AZP}	See C_{AZN}	2	2	2
GND_A	Analogue section ground pin. Connect to most negative supply. Must be at the same potential as GND_E. See application diagram.	3	4	4
D_{IN}	Differential data input.	4	5	5
D_{INB}	Inverse differential data input	5	6	6
V_{CCA}	Analogue section power pin. Connect to most positive supply. Must be at the same potential as V_{CCE}. See application diagram	6	3	7
C_F	Level-detect filter capacitor pin. Connect the capacitor between here and V_{CCA}	7	9	8
Jam	ECL compatible input controlling D_{OUT} output buffers (Pins 12&13).	8	11	11
STb	Logical inverse of ST. Normally connected on the PCB to Jam to enable automatic signal-threshold function to operate.	9	12	12
ST	Input signal-level status. This ECL[2] output is LOW when the input signal is below the threshold set by the user. This is a differential output.	10	13	13
GND_E	Digital section ground pin. Connect to the most negative supply. Must be at the same potential as GND_A. See application diagram	11	14, 15	14, 15
D_{OUTB}	Logical inverse of Pin 13. JAM high forces D_{OUTB} high.	12	16	16
D_{OUT}	ECL compatible differential data output. JAM high forces D_{OUT} low.	13	17	17
V_{CCE}	Digital/Output section power pin. Connect to the most positive supply. De-couple using ferrite bead/capacitors. See diagram.	14	18, 19	18, 19
V_{SET}	Input threshold-level setting circuit. Connect to analogue ground via a resistor. See application diagram	16	20	20
NC	Not connected. Compatible with NE5224/5 PCBs.	15		3
NC	Not connected.			9, 10

[1] ECL outputs are 100k compatible

Microcosm MC2044C/MC2045-2 Compatibility

The MC2044C and MC2045-2 are pin and functionally compatible, except that the MC2045-2 has reduced bandwidth throughout, to maximise sensitivity at 155/200Mbps. In addition, the MC2044C has CMOS-level outputs on the ST/STb pins, whereas the MC2045-2 has ECL levels.

Signal Path Description

Input biasing

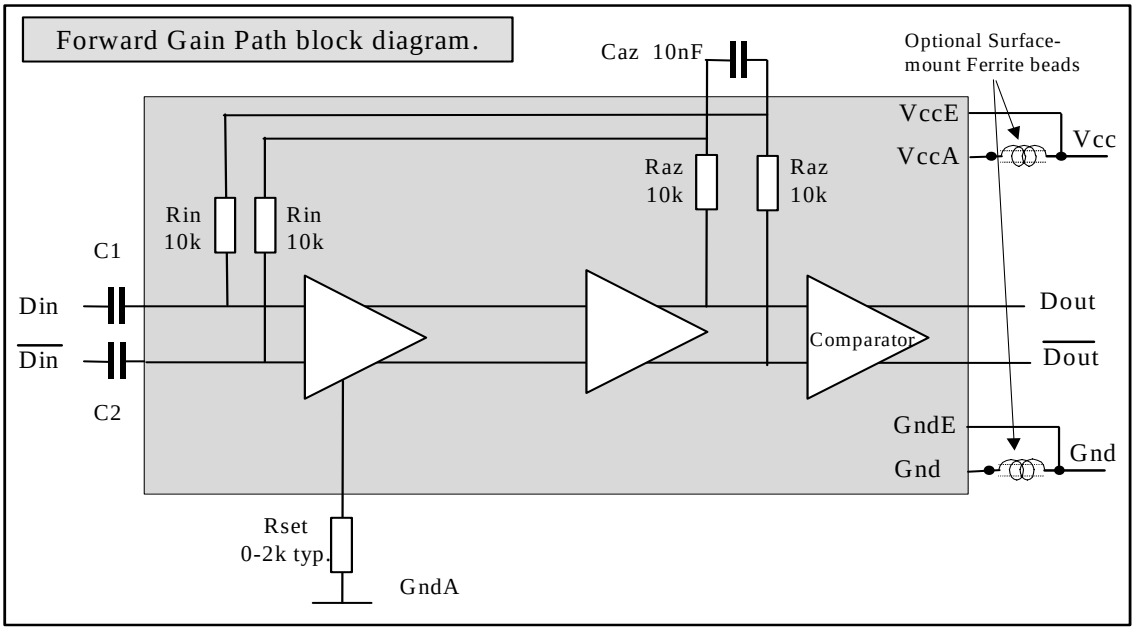
The Data Input pins are internally DC biased at approximately 4V, via the Rin resistors. Although the MC2045-2 can be DC coupled, normally it will be AC coupled, using capacitors C1 & C2. Note that Rin and C1,2 form a filter to low frequencies. The capacitors must therefore be large enough to pass the lowest input frequencies (consecutive '1's or '0's) of interest. For example, setting C1,2 to 10nF will give a typical -3dB point of approx. 3.5KHz.

Autozero circuit

The MC2045-2 includes an autozero circuit. In the absence of data, the feedback amplifier and summing circuit cancel the inherent offset voltage of the signal path, keeping the comparator at its toggle point. The time constant of this circuit is set by the combination of R_{AZ} and C_{AZ}, but is not critical. C_{AZ} is normally set to 10nF.

Power supply decoupling & optimising sensitivity

The MC2045-2 is *not* expected to require ferrite beads in order to give adequate performance. However, if pin-compatibility with the Microcosm MC2044C is preferred, or optimum MC2045-2 sensitivity required, the V_{CCA}(3) and GND_A(6) pins of the MC2045-2 should each be connected to their respective power rails via a BLM31A601SPT (Murata) ferrite suppressor. See the diagram, below. The lower-cost BLM21A601SPT has not been tested, but would also be expected to work well.



Level detector

The MC2045-2 provides for programmable input-signal level detection, and this may be used to automatically force the data outputs to a known state if the input signal falls below threshold. This is normally used to allow data to propagate only when the signal is above the Bit-Error-Rate (BER) requirement. It therefore also stops the data outputs toggling due to noise when no signal is present.

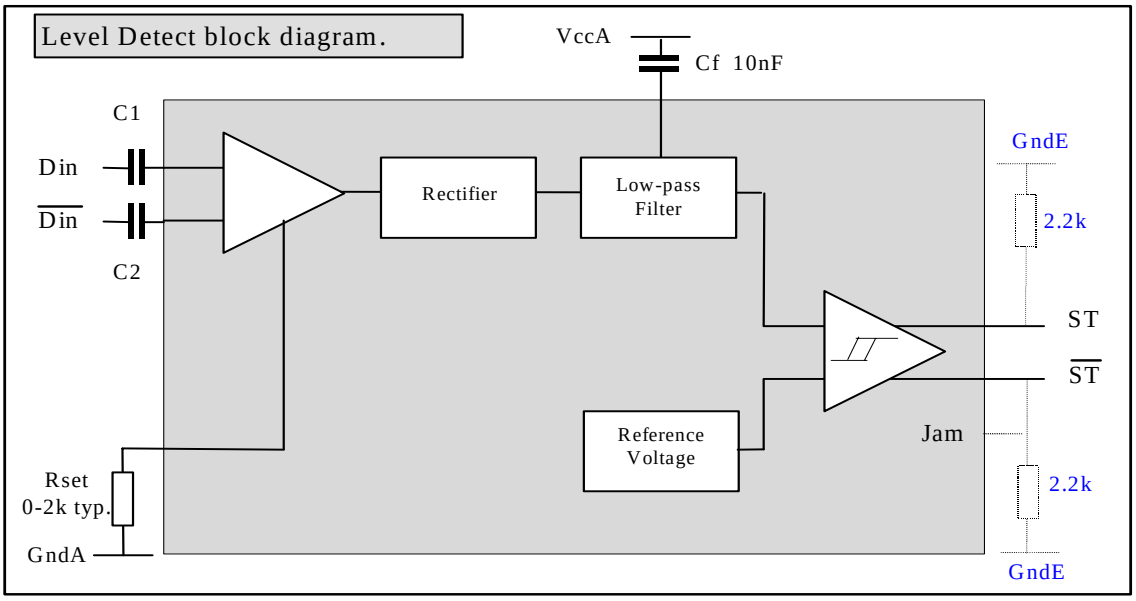
The input data is first amplified, with the level of amplification set by R_{SET}, then rectified and low-pass filtered before being compared with a reference voltage. The low-pass filter is controlled by C_F, and 10nF will provide a nominal 1µs time constant, thus avoiding false triggering due to noise spikes.

The comparator has the equivalent of approx. 2.25dB (typ.) of optical hysteresis, operating either side of the set level.

To complete the automatic level detect function, STb should be connected to the JAM input (See level detect diagram, above), thus forcing the data outputs to logical zero when the signal falls below threshold.

Note that for compatibility with the NE5224/5, Pin 15 on the SOIC16-packaged MC2045-2 is not connected to the die ('NC'). On the NE5224/5 this pin is V_{REF}, and a R1/R2 voltage divider is used to generate V_{SET}. Microcosm's solution requires only one resistor, whilst remaining compatible with the NE5224/5.

Note that R_{SET} must be connected, even if the Level-Detect function is not required.



Application Note on 3.3V Operation.

When running PECL at 3.3V the output pull-downs need to be lower than 300Ω when running into a capacitively coupled 50ohm load.

A 50ohm resistor driven by a capacitively coupled 0.8V signal will have +/- 8mA flowing in it. The output of an ECL circuit cannot sink current, the pull-down has to do this. If logic '0' is 1.6volt below V_{CC}, then it is 1.4V above GND, assuming V_{CC} is 3.0V minimum. The pull-down must be less than 175Ω to still sink the 8mA. Actually, because the emitter of a transistor does not go from low to high resistance suddenly, but inversely with emitter current, so some current must always flow to maintain a low output resistance. This indicates that 150Ω pulldowns should be used. Now the circuit sees not 50Ω, but a ***150 //50 = 37.5Ω*** ac load, and so you will get a smaller voltage swing than is normal for V_{CC}=5V.

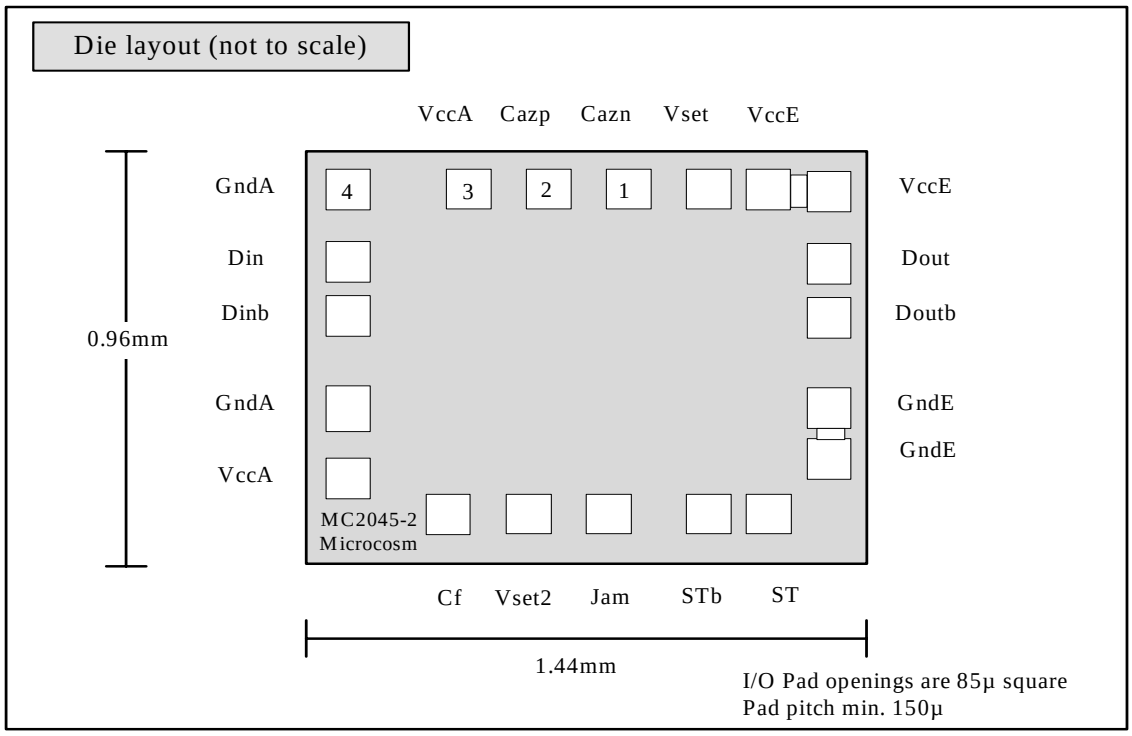
If now you operate this circuit at V_{CC}= 5.5V you get an average current in the pull-down.

(5.5-1.2)/150 = 28mA.

Users should therefore decide in advance whether it is a 3.3V or 5V power supply and set the external pull-downs accordingly.

Similarly, if the user is able to use higher impedance lines matched to a higher impedance load, then less pull-down current is required, e.g. ***$R_{pulldown}$=220ohms*** if ***Z_{load}=75ohms*** for 3.3V operation.

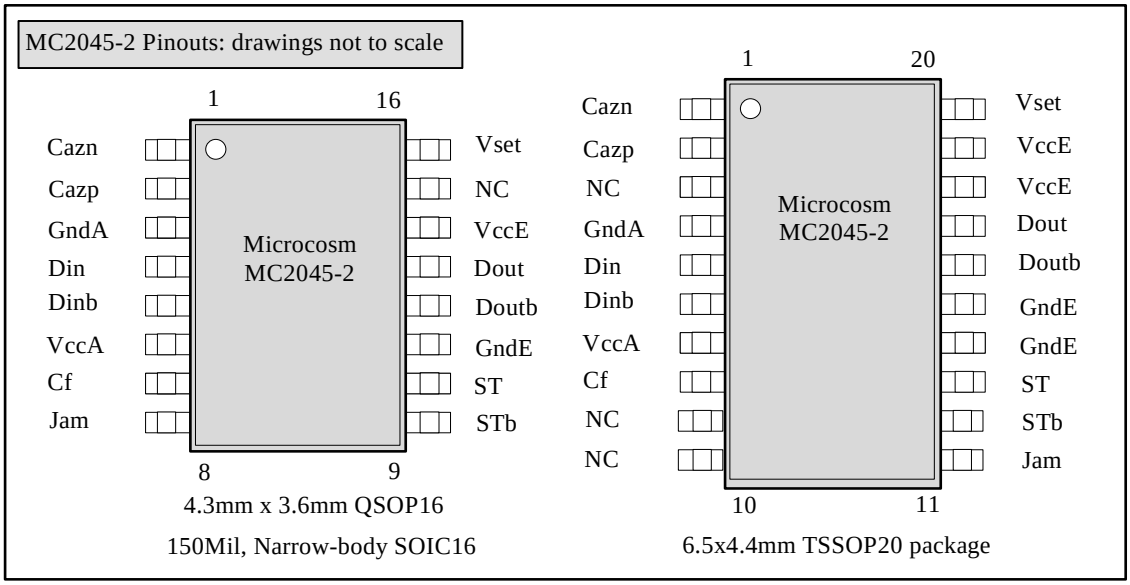
Bare Die



V_{SET} and V_{SET2} are alternative inputs to the same 'Vset' function. Connect one or other, not both.

The 2 sets of V_{CCA} and GND_A on the left of the die (Die pins 3,7 and 4,8) are to accommodate certain customer applications. Only one pair need be connected, though no harm will result from both pairs being connected. On the TSSOP package pairs of VccE and GNDE connections are brought out, and all should be connected.

Packaged Devices



MINDSPEED

World Wide Sales Offices

Headquarters

Newport Beach
Mindspeed Technologies
4000 MacArthur Boulevard, East Tower
Newport Beach, CA 92660
Phone: (949) 579-3000

www.mindspeed.com

MINDSPEED

Americas

US Southwest/Pacific Southwest
Newbury Park
Phone: (805) 786-2000
Fax: (805) 480-4486

US Northwest/Pacific Northwest
Santa Clara
Phone: (408) 423-4500
Fax: (408) 249-7113

US North Central
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Phone: (858) 228 3000
Fax: (858) 228 3000

Santa Clara
Phone: (408) 423 4500
Fax: (408) 249 7133

Asia

Taiwan
Phone: (886-2) 8789-8366
Fax: (886-2) 8789-8366

China - Hong Kong
Phone: 86-755-518-2495
Fax: 86-755-518-3024

Hong Kong
Phone: 852-2-827-0181
Fax: 852-2-827-6488

China - Central and North
Phone: (86-21) 6350-5701
Fax: (86-21)-6350-5702

Korea
Phone: 82-2-565-2880
Fax: 82-2-528-4301

Mindspeed Technologies Japan
Company Limited.
Phone: (81-3) 5380 1730
Fax: (81-3) 5371 1501

Europe

Europe Central
Germany, Switzerland Eastern
Europe
and Turkey
Phone: (49) 89 829 1320
Fax: (49) 89 834 2734

Europe Mediterranean
Italy, Spain and Portugal
Phone: (39) 02 9317 9911
Fax: (39) 02 9317 9913

Europe North
UK, Ireland and Scandinavia
Phone: 44 (0) 118 920 9500
Fax: 44 (0) 118 920 9595

UK
Phone: 44 (0) 1925-661968
Fax: 44 (0) 1925-661800

Europe South
France, Belgium and Netherlands
Phone: +33 (0) 1 56 30 80 40
Fax: +33 (0) 1 56 30 80 20

Europe - Israel/Greece
Phone: (972) 9961-5100
Fax: (972) 9957 5166

Europe - Finland
Phone: (35) 892316 6495
Fax: (35) 892316 6220