



MP7643

4-Channel, Programmable Gain
Voltage Output, 15 MHz Input Bandwidth
8-Bit DACs with Multiplying
Parallel Digital Data Port

FEATURES

- Programmable Gain
- 4 Independent 2-Quadrant Multiplying 8-Bit DACs with Output Amplifiers
- Dual Positive (+10 V and +5 V) Supplies or Dual (± 5 V) Supplies Capability
- High Speed:
 - 12.5 MHz Digital Clock Rate
 - V_{REF} to V_{OUT} Settling Time: 150ns to 8-bit (typ)
 - Voltage Reference Input Bandwidth: 15 MHz
- Very Low Noise Gain Control
- Low Power: 80mW
- Low AC Voltage Reference Feedthrough
- Excellent Channel-to-Channel Isolation

- DNL = ± 0.5 LSB, INL = ± 1 LSB (typ)
- DACs Matched to $\pm 0.5\%$ (typ)
- Low Harmonic Distortion: 0.25% typical with $V_{REF} = 1$ V p-p @ 1 MHz
- Latch-Up Free
- ESD Protection: 2000 V Minimum

APPLICATIONS

- Direct High-Frequency Automatic Gain Control
- Video AGC & CCD Level AGC
- Convergence Adjustment for High-Resolution Monitors (Workstations)
- Multiplier Replacement

GENERAL DESCRIPTION

The MP7643 is ideal for digital gain control of high frequency analog signals such as video, composite video and CCD. The device includes 4-channels of high speed, wide bandwidth, two quadrant multiplying, 8-bit accurate digital-to-analog converter. It includes an output drive buffer per channel capable of driving a ± 1 mA (typ) load. DNL of better than ± 0.5 LSB is achieved with a channel-to-channel matching of typically 0.5%. Stability, matching, and precision of the DACs are achieved by using MPS' thin film technology. Excellent channel-to-channel isolation is also achieved with MPS' BiCMOS process which cannot be achieved using a typical CMOS technology.

An open loop architecture (patent pending) provides wide small signal bandwidth from V_{REF} to output up to 15 MHz (typ),

fast output settling time of 150 ns, and excellent V_{REF} feedthrough isolation. The negative feedback terminal of the output op amp is available for user gain control. In addition, low distortion in the order of 0.25% with a 1 V p-p, 1 MHz signal is achieved.

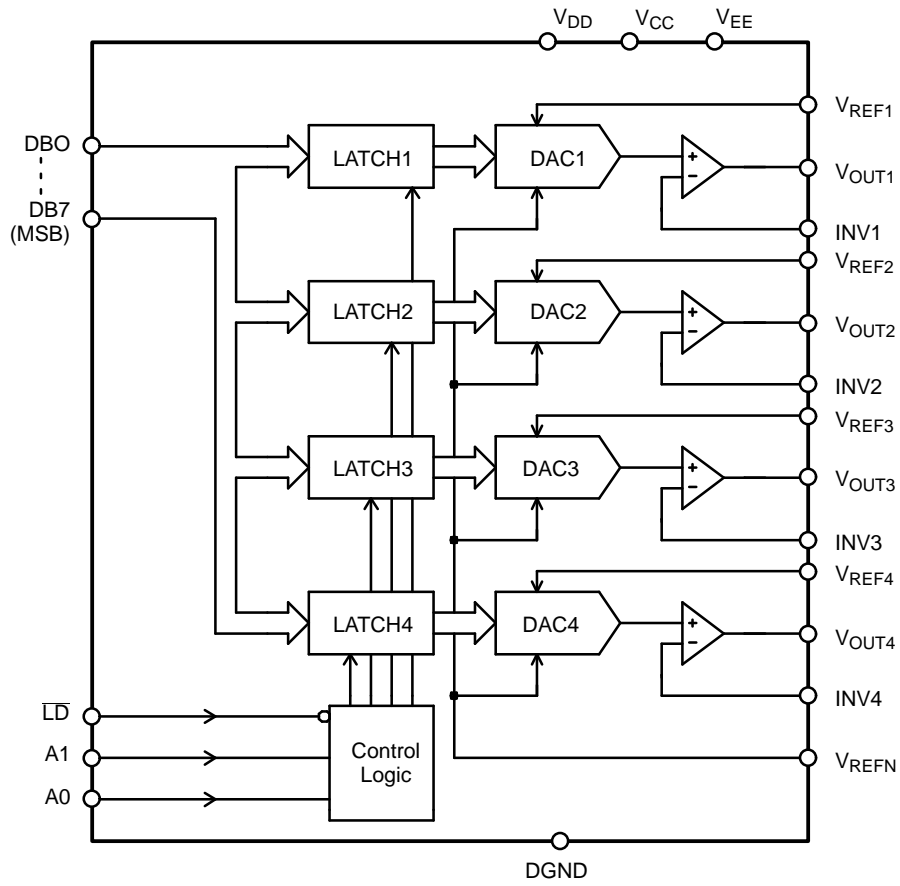
The combination of a constant input Z and the ability to vary V_{REFN} within $V_{CC} - 1.8$ V to $V_{EE} + 1.5$ V allows flexibility for optimum system design.

The MP7643 is fabricated on a junction isolated, high speed BiCMOS (BiCMOS IVTM) process with thin film resistors. This process enables precision high speed analog/digital (mixed-mode) circuits to be fabricated on the same chip.

ORDERING INFORMATION

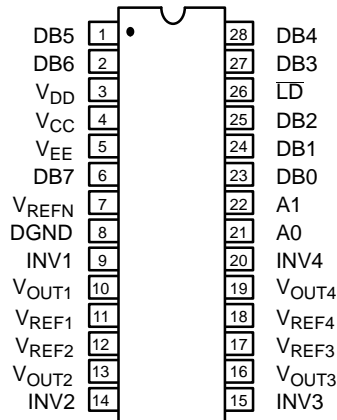
| Package Type | Temperature Range | Part No. | INL (LSB) | DNL (LSB) | Gain Error (% FSR) |
|--------------|-------------------|----------|-----------|-----------|--------------------|
| SOIC | -40 to +85°C | MP7643AS | ± 1 | ± 0.5 | ± 1.5 |
| Plastic Dip | -40 to +85°C | MP7643AN | ± 1 | ± 0.5 | ± 1.5 |

SIMPLIFIED BLOCK DIAGRAM

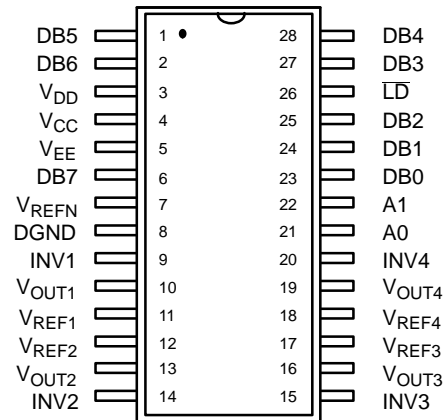


PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



**28 Pin PDIP (0.300")
NN28**



**28 Pin SOIC (Jedec, 0.300")
S28**

PIN OUT DEFINITIONS

| PIN NO. | NAME | DESCRIPTION |
|---------|-------------------|--------------------------------|
| 1 | DB5 | Data Input Bit 5 |
| 2 | DB6 | Data Input Bit 6 |
| 3 | V _{DD} | Digital Positive Supply |
| 4 | V _{CC} | Analog Positive Supply |
| 5 | V _{EE} | Analog Negative Supply |
| 6 | DB7 | Data Input Bit 7 |
| 7 | V _{REFN} | Negative Reference Input |
| 8 | DGND | Digital Ground |
| 9 | INV1 | Inverting Input 1 |
| 10 | V _{OUT1} | DAC 1 Output |
| 11 | V _{REF1} | DAC 1 Positive Reference Input |
| 12 | V _{REF2} | DAC 2 Positive Reference Input |
| 13 | V _{OUT2} | DAC 2 Output |
| 14 | INV2 | Inverting Input 2 |

| PIN NO. | NAME | DESCRIPTION |
|---------|-------------------|--------------------------------|
| 15 | INV3 | Inverting Input 3 |
| 16 | V _{OUT3} | DAC 3 Output |
| 17 | V _{REF3} | DAC 3 Positive Reference Input |
| 18 | V _{REF4} | DAC 4 Positive Reference Input |
| 19 | V _{OUT4} | DAC 4 Output |
| 20 | INV4 | Inverting Input 4 |
| 21 | A0 | DAC Address Bit 0 |
| 22 | A1 | DAC Address Bit 1 |
| 23 | DB0 | Data Input Bit 0 |
| 24 | DB1 | Data Input Bit 1 |
| 25 | DB2 | Data Input Bit 2 |
| 26 | \overline{LD} | Load Data to Selected DAC |
| 27 | DB3 | Data Input Bit 3 |
| 28 | DB4 | Data Input Bit 4 |

ELECTRICAL CHARACTERISTICS TABLE FOR DUAL SUPPLIES

Unless Otherwise Noted: $V_{DD} = 5\text{ V}$, $V_{CC} = +5\text{ V}$, $V_{EE} = -5\text{ V}$, $V_{REF} = 3\text{ V}$ and -3 V , $T = 25^\circ\text{C}$,
 Output Load = No Resistive Load, $V_{REFN} = \text{DGND} = 0\text{ V}$, Gain = 1

| Parameter | Symbol | 25°C | | | Units | Test Conditions/Comments |
|--|-------------------|----------------------|-------|----------------------|-------|--|
| | | Min | Typ | Max | | |
| DC CHARACTERISTICS | | | | | | |
| Resolution (All Grades) | N | 8 | | | Bits | |
| Differential Non-Linearity | DNL | | ±0.5 | ±0.8 | LSB | |
| Integral Non-Linearity | INL | | ±1 | ±1 | LSB | |
| Monotonicity | | Guaranteed | | | | |
| Gain Error | GE | | | ±1.5 | % FSR | FSR = Full Scale Range ¹ |
| Zero Scale Offset | Z _{OFS} | | | ±50 | mV | |
| Output Drive Capability | I _O | | ±1 | | mA | |
| REFERENCE/INV INPUTS | | | | | | |
| Impedance of V _{REF} | REF | 6 | | 18 | kΩ | V _{REF} Max Swing is V _{REFN} ±3 V |
| Voltage Range | V _{RP} | V _{EE} +1.5 | | V _{CC} -1.8 | V | |
| INV DC Voltage Range | V _{RN} | V _{EE} +1 | | 0 | V | |
| DYNAMIC CHARACTERISTICS² | | | | | | |
| Input to Output Bandwidth | | | 15 | | MHz | R _L = 5 k, C _L = 20 pF V _R = 1.6 V p-p, R _L = 5k to V _{EE} V _R = 1.6 V p-p, R _L = 5k to V _{EE} V _{OUT} =50mV p-p above code 16 |
| Input to Output Settling Time ⁵ | | | 150 | | ns | |
| Small Signal Voltage Reference | f _{tr} | | 15 | | MHz | |
| Input to Output Bandwidth | | | | | | V _{OUT} =50mV p-p for all codes |
| Small Signal Voltage Reference | f _{tr} | | 15 | | MHz | |
| Input to Output Bandwidth | | | | | | V _R =0 to V _R = 3V Step ⁶ to 1 LSB ZS to FS to 1 LSB |
| Voltage Settling from V _{REF} to V _{DAC} Out | t _{sr} | | 300 | | ns | |
| Voltage Settling from Digital Code to V _{DAC} Out | t _{sd} | | 300 | | ns | |
| V _{REF} Feedthrough | F _{DT} | | TBD | | dB | Codes=0 @ 1 MHz |
| Group Delay | GD | | TBD | | ns | |
| Harmonic Distortion | T _{HD} | | TBD | | % | V _{REF} =1MHz Sine 3V p-p |
| Channel-to-Channel Crosstalk | C _T | | TBD | | dB | @ 1 MHz, single channel |
| Digital Feedthrough | Q | | TBD | | nVS | CLK to V _{OUT} |
| Power Supply Rejection Ratio | PSRR | | ±0.05 | | %/% | ΔV=±5% |
| POWER CONSUMPTION | | | | | | |
| Positive Supply Current | I _{CC} | | | 12 | mA | V _{REF} = 0 V |
| Negative Supply Current | I _{EE} | | | 12 | mA | V _{REF} = 0 V |
| Power Dissipation | P _{DISS} | | 80 | | mW | V _{REF} = 0 V, Codes = all 1 |
| DIGITAL INPUT CHARACTERISTICS | | | | | | |
| Logic High ³ | V _{IH} | 2.4 | | | V | |
| Logic Low ³ | V _{IL} | | | 0.8 | V | |
| Input Current | I _L | | | ±10 | μA | |
| Input Capacitance ² | C _L | | 8 | | pF | |

ELECTRICAL CHARACTERISTICS TABLE

| Description | Symbol | 25°C | | | Units | Conditions |
|---|----------|------|-----|-----|-------|------------|
| | | Min | Typ | Max | | |
| DIGITAL TIMING SPECIFICATIONS (2, 4) | | | | | | |
| Address to $\overline{\text{LD}}$ Setup | t_{AS} | 70 | | | ns | |
| Address to $\overline{\text{LD}}$ Hold | t_{AH} | 0 | | | ns | |
| Data to $\overline{\text{LD}}$ Setup | t_{DS} | 70 | | | ns | |
| Data to $\overline{\text{LD}}$ Hold | t_{DH} | 0 | | | ns | |
| $\overline{\text{LD}}$ Pulse Width | t_{LD} | 70 | | | ns | |
| $\overline{\text{PRESET}}$ Pulse Width | t_{PR} | 50 | | | ns | |

NOTES

- 1 Full Scale Range (FSR) is 3V.
- 2 Guaranteed but not production tested.
- 3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
- 4 See Figure 1.
- 5 For reference input pulse: $t_R = t_F \geq 100$ ns.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)^{1, 2}

| | | | |
|---|-------------------------|--|----------------|
| V_{CC} to V_{REFN} | +6.5 V | Operating Temperature Range | |
| V_{EE} to V_{REFN} | -6.5 V | Extended Industrial | -40°C to +85°C |
| V_{CC} to DGND | +13.0 V | Maximum Junction Temperature | -65°C to 150°C |
| V_{EE} to DGND | -6.5 V | Storage Temperature | 150°C |
| V_{REF} 1-4 to DGND, V_{REFN} | V_{CC} to V_{EE} | Lead Temperature (Soldering, 10 sec) | +300°C |
| V_{OUT} 1-4 to DGND, V_{REFN} | V_{CC} to V_{EE} | Package Power Dissipation Rating @ 75°C | |
| Digital Input & Output Voltage to DGND | -0.5 to V_{DD} +0.5 V | PDIP, SOIC, PLCC | 1050mW |
| | | Derates above 75°C | 14mW/°C |

NOTES:

- 1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- 2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

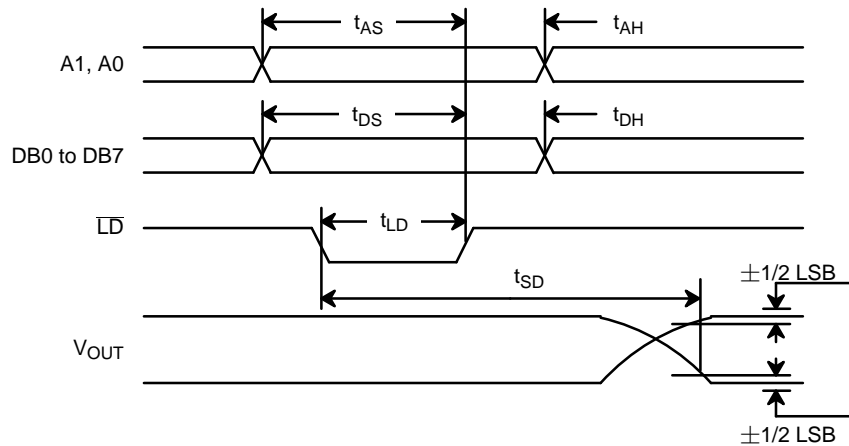


Figure 1. Timing Diagram

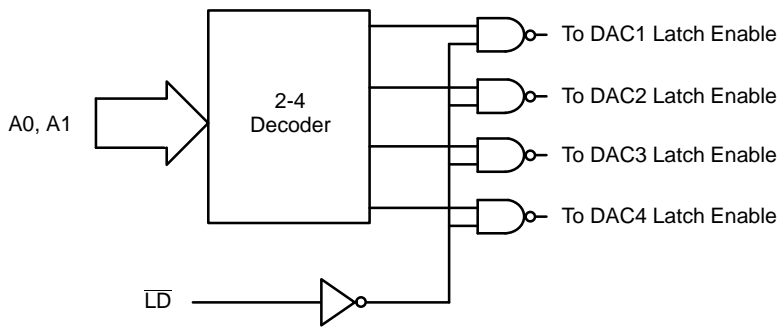


Figure 2. Input Control Logic (Simplified) Block Diagram

| LD | A1 | A0 | Operation |
|----|----|----|------------------|
| L | L | L | DAC1 Transparent |
| ↑ | L | L | DAC1 Latched |
| L | L | H | DAC2 Transparent |
| ↑ | L | H | DAC2 Latched |
| L | H | L | DAC3 Transparent |
| ↑ | H | L | DAC3 Latched |
| L | H | H | DAC4 Transparent |
| ↑ | H | H | DAC4 Latched |
| H | X | X | No Operation |

Table 1. Truth Table

| D7 MSB | D6 | D5 | D4 | D3 | D2 | D1 | D0 LSB | DAC Output Voltage $V_{O_i} = V_{REFN} + (V_{R_i} - AGND) \left(\frac{D}{256} \right)$ |
|-----------|----|----|----|----|----|----|-----------|--|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | V_{REFN} |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | $(V_{R_i} - V_{REFN}) \left(\frac{1}{256} \right) + V_{REFN}$ |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | $(V_{R_i} - V_{REFN}) \left(\frac{254}{256} \right) + V_{REFN}$ |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | $(V_{R_i} - V_{REFN}) \left(\frac{255}{256} \right) + V_{REFN}$ |

Note: These outputs must be ratioed up for gain in the output amplifier.

**Table 2. DAC Transfer Function
Analog Output vs. Digital Code (With V_{REF} Shorted to INV)**

THEORY OF OPERATION

The MP7643 is a 4-channel multiplying D/A converter that incorporates a novel open loop architecture invented by MPS. The design produces the wider bandwidth, faster settling time, more constant group delay, and a lower noise operation compared to the conventional R-2R based architectures. This device is particularly useful in applications where analog multipliers are used to perform the gain adjustment function for high frequency analog signal conditioning. Analog multipliers produce higher noise and offset. This design allows for digital control of gain with constant and very low noise from the low gain through high gain ranges of operation.

Linearity Characteristics

Each DAC achieves $DNL \leq \pm 0.5$ LSB (typ), $INL \leq \pm 1$ LSB (typ), and gain error $\leq \pm 1.5\%$. Since all 4 channel D/A converters are fabricated on the same IC, the linearity matching and gain matching of $\pm 0.5\%$ (typ) is achieved.

AC and Transient Settling Characteristics

The novel subranging architecture delivers a 15 MHz (typ.) -3 dB bandwidth. With all codes = 1 and a 1.6 V step impulse at $V_{REF}(1-4)$, the analog output settles to 8 bits of accuracy in typically 150 ns (with $R_L = 5k$ to V_{EE}). Also with $V_{REF} = 3$ V or -3 V and a FS to ZS or ZS to FS code change, the respective analog output settles to 8 bits typically in 300 ns. Note that the AC performance specifications also match between all 4 channels. The above AC and transient performance is achieved with each channel consuming only 20 mW (typ.) with either ± 5 V or 0 V to 10 V supplies.

Digital Interface

The MP7643 allows direct interface to most microprocessor buses without additional I/O circuitry. *Figure 1.* and *Figure 2.* describe the operation, specification and interface characteristics of the logic port.

The address bits A0 and A1 determine which D/A channel is selected. When \overline{LD} input is low the respective latch of the D/A is enabled (digital input data becomes transparent to the latch and the selected DAC channel), and digital data is loaded into the selected DAC.

Power Supplies and Voltage Reference DC Voltage Ranges

For the single supply operation, $V_{CC} = +10$ V, $V_{DD} = +5$ V, and $V_{EE} = GND = 0$ V. The $V_{OUT} 1-4$ and $V_{REF} 1-4$ range would be $V_{CC} - 1.8$ V ($10 - 1.8 = 8.2$ V) to $V_{EE} + 1.5$ V ($0 + 1.5 = 1.5$ V). V_{REFN} is the equivalent of AGND for this DAC. In this mode V_{REFN} can be set at $(V_{CC} + V_{EE})/2 = (10 + 0)/2 = 5$ V. V_{REFN} DC range can, however, be set from $V_{EE} + 1.5 = 1.5$ V to $V_{CC} - 1.5 = 8.2$ V. Refer to *Table 2.* for the relationship equations.

For the dual supply operation, $V_{CC} = +5$, $V_{DD} = +5$, and $V_{EE} = -5$ V. The $V_{OUT} 1-4$ and $V_{REF} 1-4$ range would be $V_{CC} - 1.8$ V ($5 - 1.8 = 3.2$ V) to $V_{EE} + 1.5$ V ($-5 + 1.5 = -3.5$ V). In this mode V_{REFN} can be set to $(V_{CC} + V_{EE})/2 = (5 - 5)/2 = 0$ V. However, V_{REFN} DC range can be set from $V_{EE} + 1.5 = -3.5$ V to $V_{CC} - 1.8 = +3.2$ V. Refer to *Table 2.* for the relationship equations.

About the INV Input and its DC Voltage Range

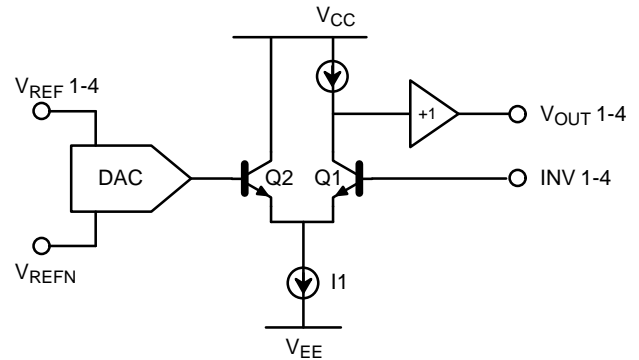
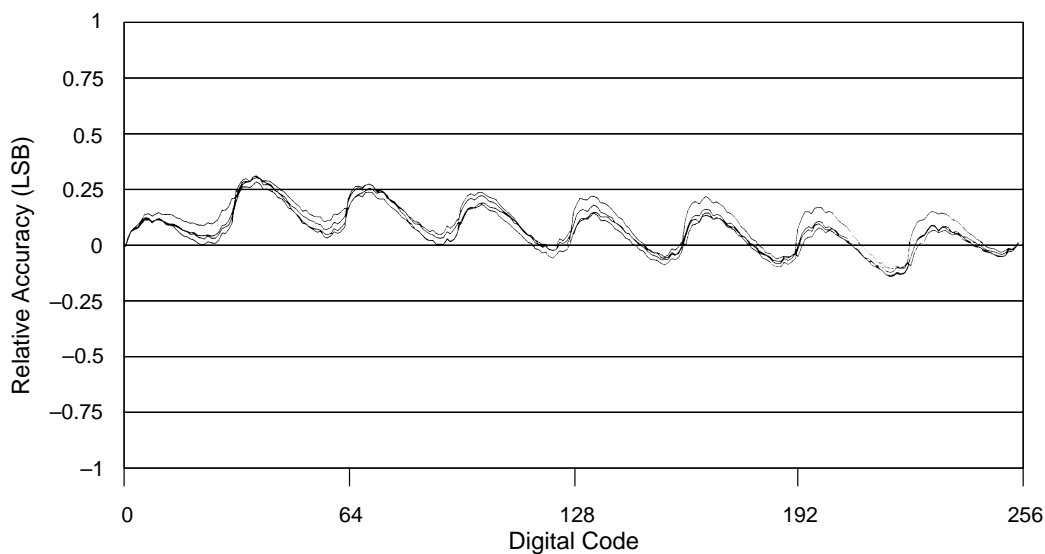


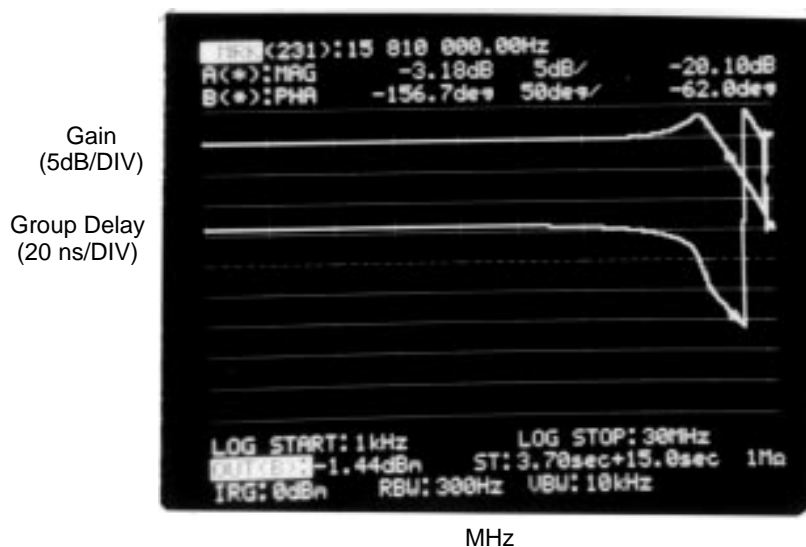
Figure 3. Simplified Block Diagram

As noted in the specification table, the max DC value of the INV input pin is V_O . *Figure 3.* shows a simplified block diagram of the internal circuitry around INV. If V_{INV} exceeds V_O , Q1 will saturate and the amp and consequently the DAC becomes non-functional.

The min DC range of INV is limited to $V_{be}(Q1)$ and $V_{CE}(sat)$ of I_1 . Therefore, $INV (min-DC) = V_{EE} + 1$ V.

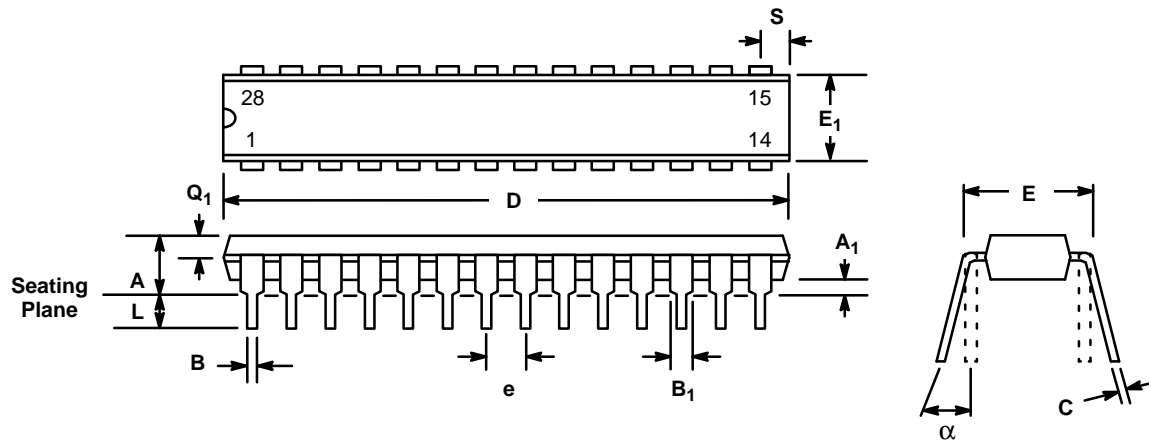


**Graph 1. Relative Accuracy vs. Digital Code
DACs 1 to 4**



**Graph 2. Typical Gain and Group Delay vs. Frequency
(with 5K Resistor Across Output to V_{EE})**

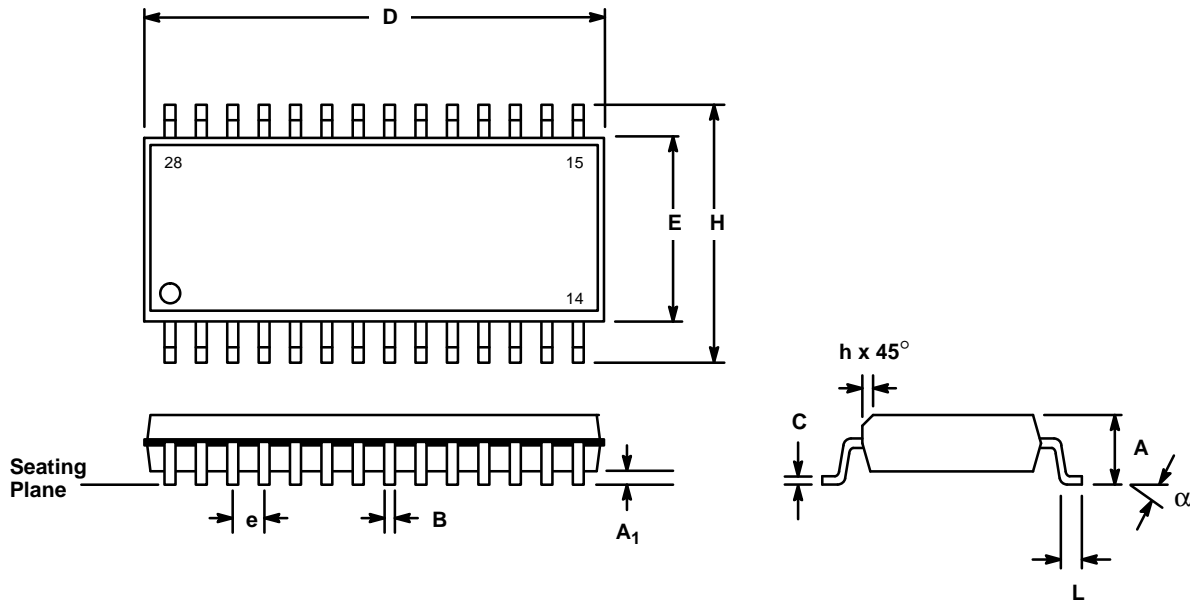
**28 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
NN28**



| SYMBOL | INCHES | | MILLIMETERS | |
|--------------------|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.130 | 0.230 | 3.30 | 5.84 |
| A ₁ | 0.015 | — | 0.381 | — |
| B | 0.014 | 0.023 | 0.356 | 0.584 |
| B ₁ (1) | 0.038 | 0.065 | 0.965 | 1.65 |
| C | 0.008 | 0.015 | 0.203 | 0.381 |
| D | 1.340 | 1.485 | 34.04 | 37.72 |
| E | 0.290 | 0.325 | 7.37 | 8.26 |
| E ₁ | 0.240 | 0.310 | 6.10 | 7.87 |
| e | 0.100 BSC | | 2.54 BSC | |
| L | 0.115 | 0.150 | 2.92 | 3.81 |
| α | 0° | 15° | 0° | 15° |
| Q ₁ | 0.055 | 0.070 | 1.40 | 1.78 |
| S | 0.020 | 0.100 | 0.508 | 2.54 |

Note: (1) The minimum limit for dimensions B₁ may be 0.023" (0.58 mm) for all four corner leads only.

28 LEAD SMALL OUTLINE (300 MIL JEDEC SOIC) S28



| SYMBOL | INCHES | | MILLIMETERS | |
|----------|-----------|--------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.097 | 0.104 | 2.464 | 2.642 |
| A1 | 0.0050 | 0.0115 | 0.127 | 0.292 |
| B | 0.014 | 0.019 | 0.356 | 0.483 |
| C | 0.0091 | 0.0125 | 0.231 | 0.318 |
| D | 0.701 | 0.711 | 17.81 | 18.06 |
| E | 0.292 | 0.299 | 7.42 | 7.59 |
| e | 0.050 BSC | | 1.27 BSC | |
| H | 0.400 | 0.410 | 10.16 | 10.41 |
| h | 0.010 | 0.016 | 0.254 | 0.406 |
| L | 0.016 | 0.035 | 0.406 | 0.889 |
| α | 0° | 8° | 0° | 8° |

Notes

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