NOVATEK

NT7704

240 Output LCD Segment/Common Driver

Features

(Segment mode)

- Shift Clock frequency:
  20 MHz (Max.) (V_{DD} = 5 V ± 10%)
  12 MHz (Max.) (V_{DD} = 2.5V - 4.5V)
- Adopts a data bus system
- 4-bit/8-bit parallel input modes are selectable with a mode (MD) pin
- Automatic transfer function with an enable signal
- Automatic counting function when in "chip select" mode, which causes the internal clock to be stopped by automatically counting 240 bits of input data

(Common mode)

- Shift clock frequency :
  4.0 MHz (Max.)
- Built-in 240-bits bidirectional shift register (divisible into 120-bits x 2)
- Available in a single mode (240-bits shift register) or in a dual mode(120-bits shift register x 2)
  1. Y1 → Y240 Single mode
  2. Y240 → Y1 Single mode
  3. Y1 → Y120, Y121 → Y240 Dual mode
  4. Y240 → Y121, Y120 → Y1 Dual mode
  The above 4 shift directions are pin-selectable

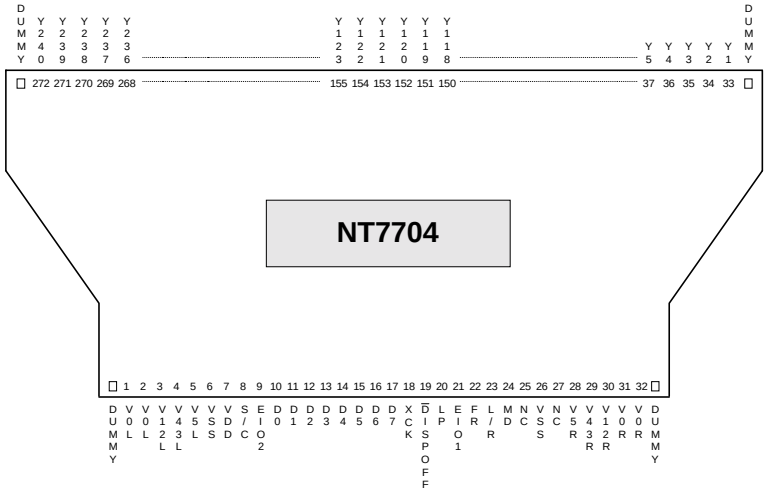
(Both for segment mode and common mode)

- Supply voltage for LCD driver: 15.0 to 30.0 V
- Number of LCD driver outputs: 240
- Low output impedance
- Low power consumption
- Supply voltage for the logic system: +2.5 to +5.5 V
- COMS process
- Package: Gold bump die / 272 Pin TCP(Tape Carrier Package)
- Not designed or rated as radiation hardened

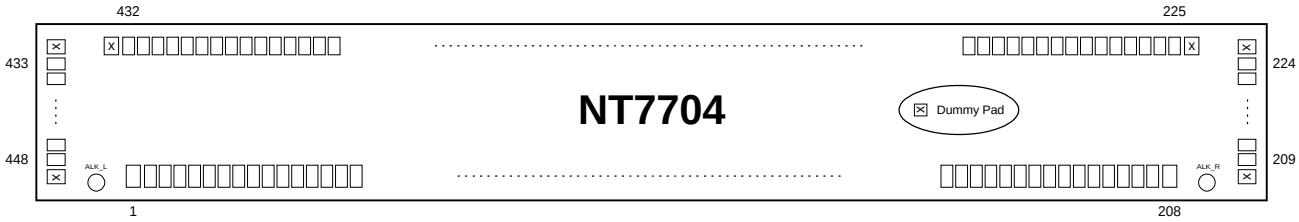
General Description

The NT7704 is a 240-bit output segment/common driver LSI suitable for driving large scale dot matrix LCD panels used by PDA's, personal computers and work stations for example. Through the use of COG technology, it is ideal for substantially decreasing the size of the frame section of the LCD module. The NT7704 is good as both a segment driver and as a common driver, and a low power consuming, high-precision LCD panel display can be assembled using the NT7704. In the segment mode, the data input is selected as 4bit parallel input mode or as 8bit parallel input mode by a mode (MD) pin. In the common mode, the data input/output pins are bi-directional and the four data shift directions are pin-selectable.

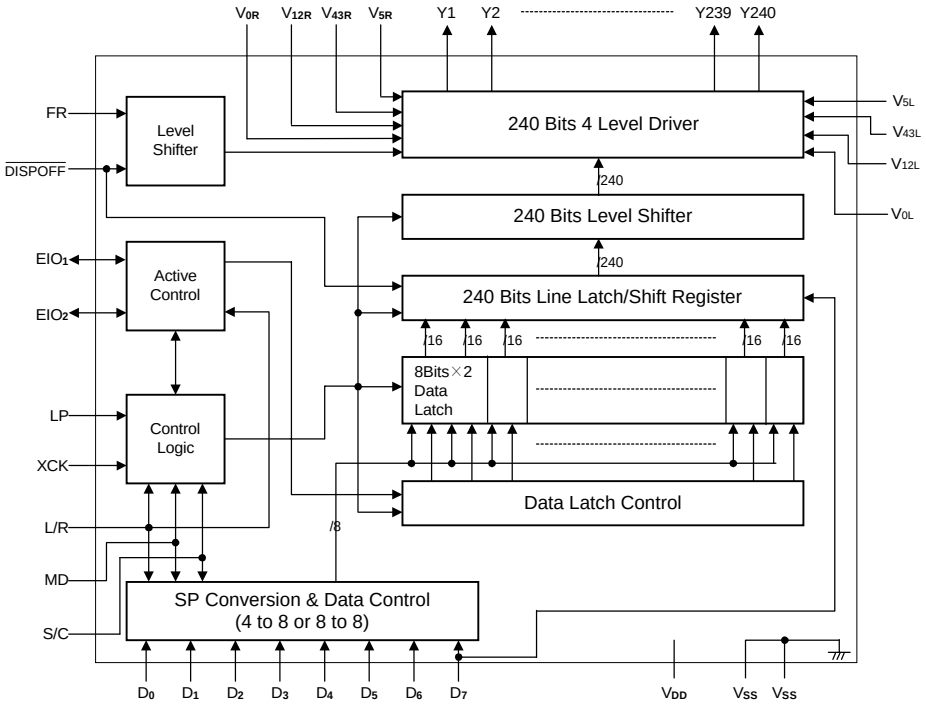
Pin Configuration



Pad Configuration



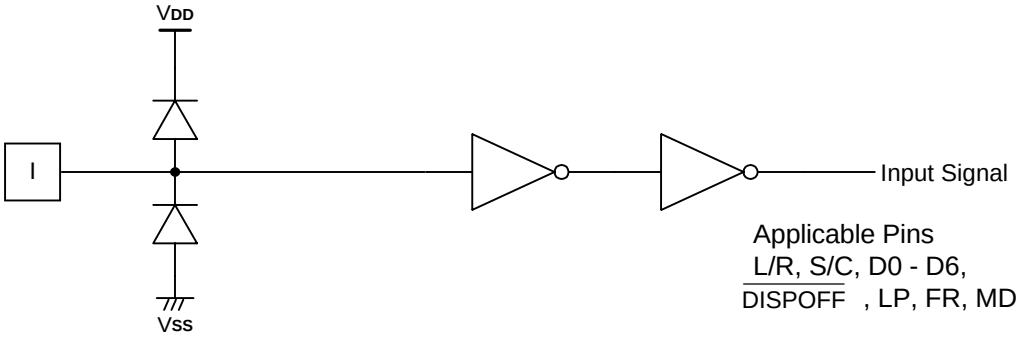
Block Diagram



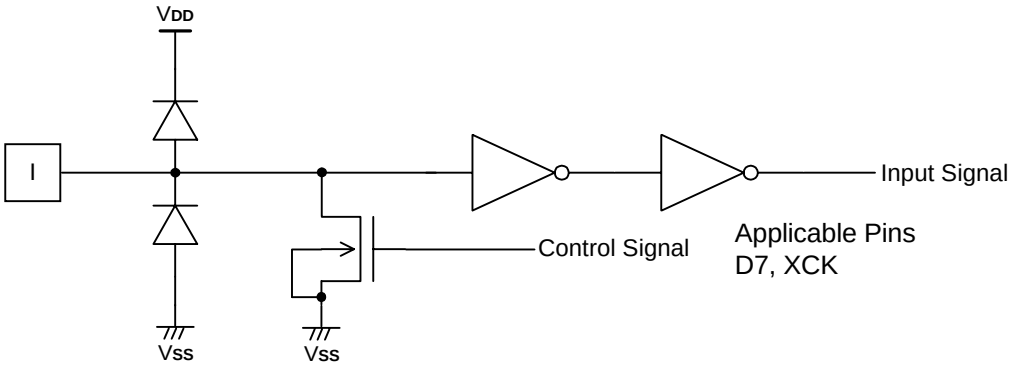
Pad Description

Pad No.	Designation	I/O	Description
1 - 12	V_{0L}	P	Power supply for LCD driver
13 - 20	V_{12L}	P	Power supply for LCD driver
21 -28	V_{43L}	P	Power supply for LCD driver
29 - 40	V_{5L}	P	Power supply for LCD driver
41 - 66	V_{SS}	P	Ground (0V), these pads must be connected to each other
67 - 92	V_{DD}	P	Power supply for the logic system (+2.5 to +5.5V)
93 - 94	S/C	I	Segment mode/common mode selection
95 - 97	EIO_2	I/O	Input/output for chip select or data of the shift register
98, 99, 100 - 116, 117, 118	D0 - D6	I	Display data input for segment mode
119 - 121	D7	I	Display data input for Segment mode/ Dual mode data input
122 - 124	XCK	I	Display data shift clock input for segment mode
125 - 127	$\overline{DISPOFF}$	I	Control input for deselect output level
128 - 130	LP	I	Latch pulse input/shift clock input for the shift register
131 - 133	EIO_1	I/O	Input/output for chip select or data of the shift register
134 - 136	FR	I	AC-converting signal input for LCD driver waveform
137 - 139	L/R	I	Display data shift direction selection
140 - 142	MD	I	Mode selection input
143 - 168	V_{SS}	P	Ground (0V), these pads must be connected to each other
169 - 180	V_{5R}	P	Power supply for LCD driver
181 - 188	V_{43R}	P	Power supply for LCD driver
189 - 196	V_{12R}	P	Power supply for LCD driver
197 - 208	V_{0R}	P	Power supply for LCD driver
209 - 448	Y1 - Y240	O	LCD driver output

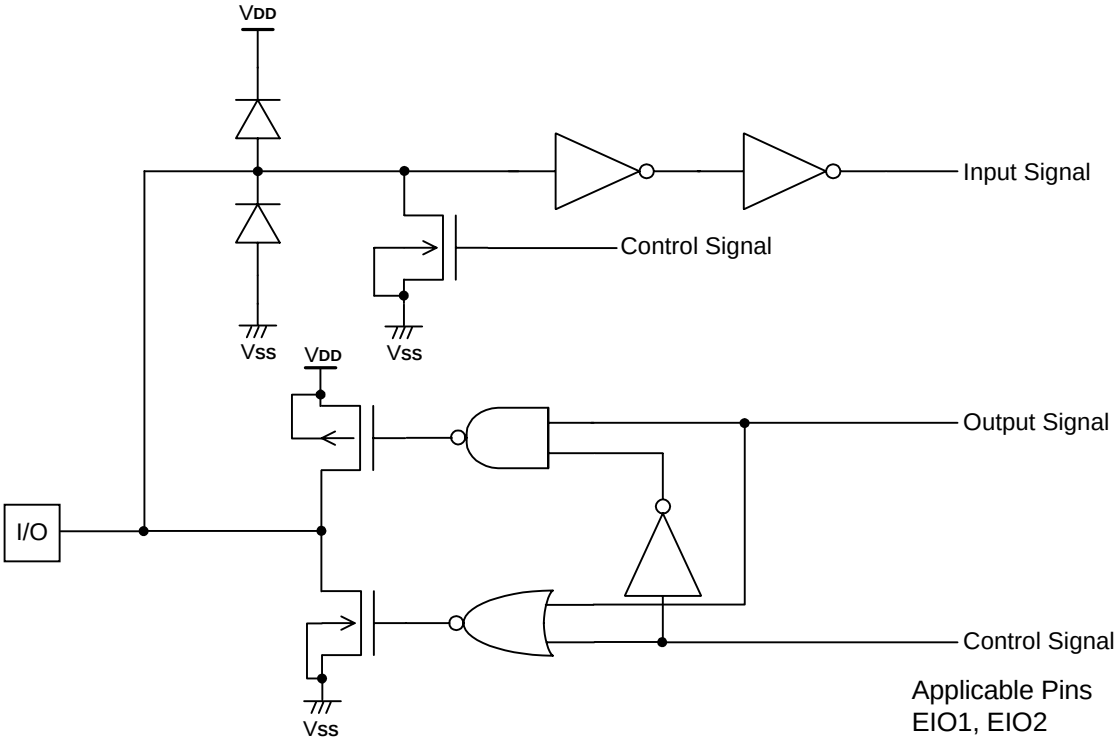
Input / Output Circuits



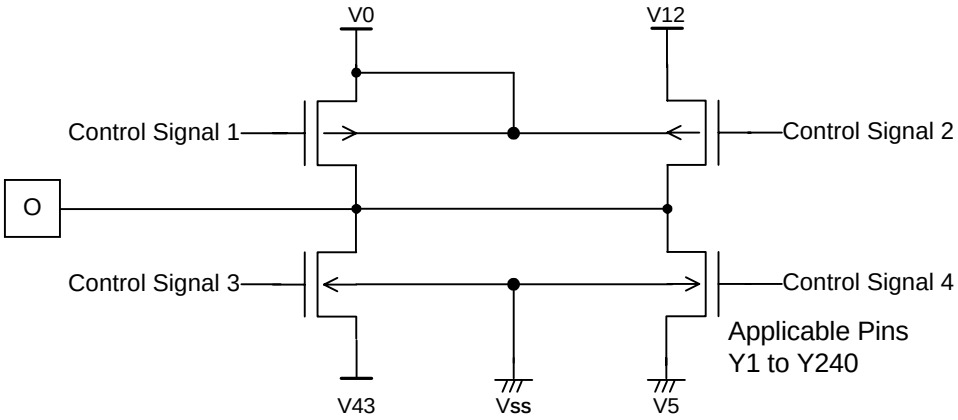
Input Circuit (1)



Input Circuit (2)



Input / Output Circuit



LCD Driver Output circuit

Pad Description

Segment mode

Symbol	Function
V_{DD}	Logic system power supply pin connects from +2.5 to +5.5V
V_{SS}	Ground pin connects to 0V
V_{OR}, V_{OL} V_{12R}, V_{12L} V_{43R}, V_{43L} V_{5R}, V_{5L}	Power supply pin for LCD driver voltage bias ● Normally, the bias voltage used is set by a resistor divider ● Ensure that the voltages are set such that $V_{SS} \le V_5 < V_{43} < V_{12} < V_0$ ● To further reduce the differences between the output waveforms of the LCD driver output pins Y_1 and Y_{240}, externally connect V_{iR} and V_{iL} (I = 0, 12, 43, 5)
D_0 - D_7	Input pin for display data ● In 4-bit parallel input mode, input data into the 4 pins D_0 - D_3. Connect D_4 - D_7 to V_{SS} or V_{DD} ● In 8-bit parallel input mode, input data into the 8 pins D_0 - D
XCK	Clock input pin for taking display data ● Data is read on the falling edge of the clock pulse
LP	Latch pulse input pin for display data ● Data is latched on the falling edge of the clock pulse
L/R	Direction selection pin for reading display data ● When set to V_{SS} level "L", data is read sequentially from Y240 to Y1 ● When set to V_{DD} level "H", data is read sequentially from Y1 to Y240
$\overline{DISPOFF}$	Control input pin for output deselect level ● The input signal is level-shifted from the logic voltage level to the LCD driver voltage level, and controls the LCD driver circuit. ● When set to V_{SS} level “L”, the LCD driver output pins (Y1-Y240) are set to level V_5 ● When $\overline{DISPOFF}$ is set to “L”, the contents of the line latch are reset, but the display data in the data latch are read regardless of the condition of $\overline{DISPOFF}$. When the $\overline{DISPOFF}$ function is canceled, the driver outputs deselect level (V_{12} or V_{43}), then outputs the contents of the date latch onto the next falling edge of the LP. At that time, if the $\overline{DISPOFF}$ removal time can not keep regulation with what is shown on the AC characteristics, then it can not output the reading data correctly.
FR	AC signal input for LCD driving waveform ● The input signal is level-shifted from the logic voltage level to the driver voltage level and controls the LCD driver circuit. ● It normally inputs a frame inversion signal The LCD driver output pin’s output voltage level can be set to the line latch output signal and the FR signal
MD	Mode selection pin ● When set to V_{SS} level “L”, 8-bit parallel input mode is set ● When set to V_{DD} level “H", 4-bit parallel input mode is set

Segment mode continued

Symbol	Function
S/C	Segment mode/common mode selection pin ● When set to V_{DD} level "H", segment mode is set ● When set to V_{SS} level "L", common mode is set
EIO_1, EIO_2	Input/output pin for chip selection ● When L/R input is at V_{SS} level "L", EIO_1 is set for output, and EIO_2 is set for input ● When L/R input is at V_{DD} level "H", EIO_1 is set for input, and EIO_2 is set for output ● During output, it is set to "H" while LP* $\overline{XCK}$ is "H" and then after 240-bits of data have been read, it is set to "L" for one cycle (from falling edge to falling edge of XCK), after which it returns to "H" ● During input, after the LP signal is input, the chip is selected while EI is set to "L". After 240-bits of data have been read, the chip is deselected
Y_1 - Y_{240}	LCD driver output pins These correspond directly to each bit of the data latch, one level (V_0, V_{12}, V_{43}, or V_5) is selected and output

Common mode

Symbol	Function
V_{DD}	Logic system power supply pin connects to +2.5 to +5.5V
V_{SS}	Ground pin connects to 0V
V_{0R}, V_{0L} V_{12R}, V_{12L} V_{43R}, V_{43L} V_{5R}, V_{5L}	Power supply pin for LCD driver voltage bias. ● Normally, the bias voltage used is set by a resistor divider ● Ensure the voltages are set such that $V_{SS} \le V_5 < V_{43} < V_{12} < V_0$ To further reduce the differences between the output waveforms of the LCD driver output pins Y_1 and Y_{240}, externally connect V_{iR} and V_{iL} (I = 0, 12, 43, 5)
EIO_1	Bi-directional shift register shift data input/output pin ● Is an output pin when L/R is at V_{SS} level "L" and is an input pin when L/R is at V_{DD} level "H" ● When EIO_1 is used as an input pin, it will be pulled-down ● When EIO_1 is used as an output pin, it won't be pulled-down
EIO_2	Bi-directional shift register shift data input/output pin ● Is an input pin when L/R is at V_{SS} level "L" and is an output pin when L/R is at V_{DD} level "H" ● When EIO_2 is used as an input pin, it will be pulled-down ● When EIO_2 is used as an output pin, it won't be pulled-down
LP	Bi-directional shift register shift clock pulse input pin ● Data is shifted on the falling edge of the clock pulse
L/R	Bi-directional shift register shift direction selection pin ● Data is shifted from Y_{240} to Y_1 when it is set to V_{SS} level "L", and data is shifted from Y_1 to Y_{240} when it is set to V_{DD} level "H"

Common mode continued

Symbol	Function
$\overline{DISPOFF}$	Control input pin for output deselect level ● The input signal is level-shifted from the logic voltage level to the LCD driver voltage level, and controls the LCD driver circuit ● When set to V_{SS} level "L", the LCD driver output pins (Y_1-Y_{240}) are set to level V_5 ● While set to "L", the contents of the shift resister are reset and are not reading data. When the $\overline{DISPOFF}$ function is canceled, the driver outputs deselect level (V_{12} or V_{43}), and the shift data is read on the falling edge of the LP. At that time, if the $\overline{DISPOFF}$ removal time can not keep regulation with what is shown on the AC characteristics, the shift data is not read correctly
FR	AC signal input for LCD driving waveform ● The input signal is level-shifted from logic voltage level to the LCD driver voltage level, and it controls the LCD driver circuit ● Normally, it inputs a frame inversion signal The LCD driver output pin's output voltage level can be set using the shift register output signal and the FR signal
MD	Mode selection pin ● When set to V_{SS} level "L", Single Mode operation is selected. When set to V_{DD} level "H", Dual Mode operation is selected
D_7	Dual Mode data input pin ● According to the data shift direction of the data shift register, data can be input starting from the 121st bit When the chip is used in Dual Mode, D_7 will be pulled-down When the chip is used in Single Mode, D_7 won't be pulled-down
S/C	Segment mode/common mode selection pin ● When set to V_{SS} level "L", common mode is set
D_0 - D6	Not used ● Connect D_0-D_6 to V_{SS} or V_{DD}. Avoid floating
XCK	Not used ● XCK is pull-down in common mode, so connect to V_{SS} or leave open
Y_1 - Y_{240}	LCD driver output pins ● These correspond directly to each bit of the shift register, one level (V_0, V_{12}, V_{43}, or V_5) is selected and output

Functional Description

1. Block description

1.1 Active Control

In segment mode, it controls the selection or deselection of the chip. Following a LP signal input, and after the select signal is input, a select signal is generated internally until 240 bits of data have been read in. Once data input has been completed, a select signal for cascade connection is output, and the chip is deselected.

In common mode, it controls the input/output data of the bi-directional pins.

1.2. SP Conversion & Data Control

In segment mode, it keeps input data which are 2 clocks of XCK at 4-bit parallel mode into latch circuit, or keeps input data which are 1 clock of XCK at 8-bit parallel mode into latch circuit, after that they are put on the internal data bus 8 bits at a time.

1.3. Data Latch Control

In segment mode, it selects the state of the data latch, which reads in the data bus signals. The shift direction is controlled by the control logic and for every 16 bits of data read in, the selection signal shifts one bit, based on the state of the control circuit.

1.4. Data Latch

In segment mode, it latches the data on the data bus. The latched state of each LCD driver output pin is controlled by the control logic and the data latch control. 240 bits of data are read in 20 sets of 8 bits.

1.5. Line Latch/Shift Register

In segment mode, it ensures all 240 bits which have been read into the data latch, are simultaneously latched on to the falling edge of the LP signal, and output to the level shift block.

In common mode, it shifts data from the data input pin on to the falling edge of the LP signal.

1.6. Level Shifter

It ensures the logic voltage signal is level-shifted to the LCD driver voltage level, and output to the driver block.

1.7. 4-Level Driver

It drives the LCD driver output pins from the line latch/shift register data, selecting one of 4 levels (V_0, V_{12}, V_{43}, V_5) based on the S/C, FR and $\overline{\text{DISPOFF}}$ signals.

1.8. Control Logic

Controls the operation of each block. In segment mode, when an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission are controlled, 240 bits of data are read in, and the chip is deselected.

In common mode, it controls the direction of data shift.

2. LCD Driver Output Voltage Level

The relationship between the data bus signal, AC converted signal FR and LCD driver output voltage is as shown in the table below:

2.1. Segment Mode

FR	Latch Data	$\overline{DISPOFF}$	Driver Output Voltage Level (Y_1 - Y_{240})
L	L	H	V_{43}
L	H	H	V_5
H	L	H	V_{12}
H	H	H	V_0
X	X	L	V_5

Here, $V_{SS} \le V_5 < V_{43} < V_{12} < V_0$, H: V_{DD} (+2.5 to +5.5V), L: V_{SS} (0V), X: Don't care

2.2. Common Mode

FR	Latch Data	$\overline{DISPOFF}$	Driver Output Voltage Level (Y_1 - Y_{240})
L	L	H	V_{43}
L	H	H	V_0
H	L	H	V_{12}
H	H	H	V_5
X	X	L	V_5

Here, $V_{SS} \le V_5 < V_{43} < V_{12} < V_0$, H: V_{DD} (+2.5 to +5.5V), L: V_{SS} (0V), X: Don't care

Note: There are two kinds of power supply (logic level voltage, LCD driver voltage) for the LCD driver. Please supply regular voltage which is assigned by specification for each power pin.
That time "Don't care" should be fixed to "H" or "L", avoiding floating.

3. Relationship between the Display Data and Driver Output pins

3.1. Segment Mode:

(a) 4-bit Parallel Mode

MD	L/R	EIO_1	EIO_2	Data Input	Number of Clock						
					60clock	59clock	58clcok	~	3clock	2clock	1clock
H	L	Output	Input	D_0	Y1	Y5	Y9	~	Y229	Y233	Y237
				D_1	Y2	Y6	Y10	~	Y230	Y234	Y238
				D_2	Y3	Y7	Y11	~	Y231	Y235	Y239
				D_3	Y4	Y8	Y12	~	Y232	Y236	Y240
H	H	Input	Output	D_0	Y240	Y236	Y232	~	Y12	Y8	Y4
				D_1	Y239	Y235	Y231	~	Y11	Y7	Y3
				D_2	Y238	Y234	Y230	~	Y10	Y6	Y2
				D_3	Y237	Y233	Y229	~	Y9	Y5	Y1

(b) 8-bit Parallel Mode

MD	L/R	EIO_1	EIO_2	Data Input	Number of Clock						
					30clock	29clock	28clcok	~	3clock	2clock	1clock
L	L	Output	Input	D_0	Y1	Y9	Y17	~	Y217	Y225	Y233
				D_1	Y2	Y10	Y18	~	Y218	Y226	Y234
				D_2	Y3	Y11	Y19	~	Y219	Y227	Y235
				D_3	Y4	Y12	Y20	~	Y220	Y228	Y236
				D_4	Y5	Y13	Y21	~	Y221	Y229	Y237
				D_5	Y6	Y14	Y22	~	Y222	Y230	Y238
				D_6	Y7	Y15	Y23	~	Y223	Y231	Y239
				D_7	Y8	Y16	Y24	~	Y224	Y232	Y240
L	H	Input	Output	D_0	Y240	Y232	Y224	~	Y24	Y16	Y8
				D_1	Y239	Y231	Y223	~	Y23	Y15	Y7
				D_2	Y238	Y230	Y222	~	Y22	Y14	Y6
				D_3	Y237	Y229	Y221	~	Y21	Y13	Y5
				D_4	Y236	Y228	Y220	~	Y20	Y12	Y4
				D_5	Y235	Y227	Y219	~	Y19	Y11	Y3
				D_6	Y234	Y226	Y218	~	Y18	Y10	Y2
				D_7	Y233	Y225	Y217	~	Y17	Y9	Y1

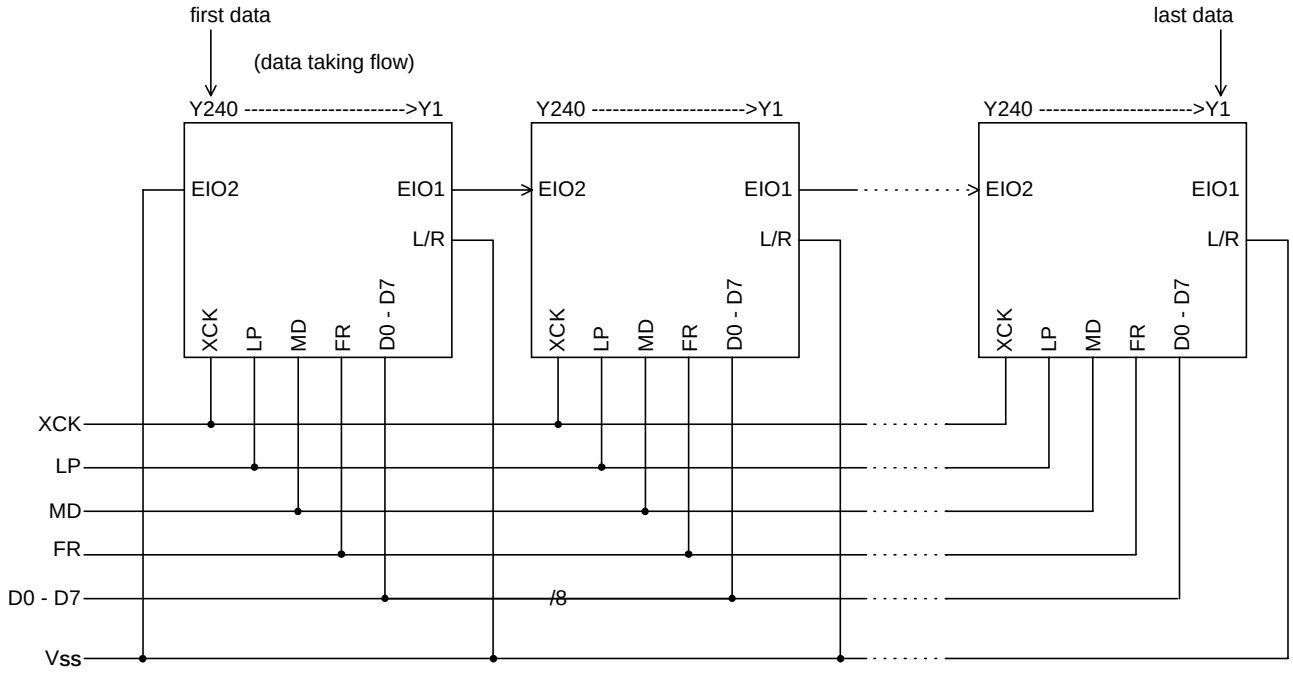
3.2. Common Mode

MD	L/R	Data Transfer Direction	EIO1	EIO2	D7
L (Single)	L (shift to left)	Y240 to Y1	Output	Input	X
	H (shift to right)	Y1 to Y240	Input	Output	X
H (Dual)	L (shift to left)	Y240 to Y121 Y120 to Y1	Output	Input	Input
	H (shift to right)	Y1 to Y120 Y121 to Y240	Input	Output	Input

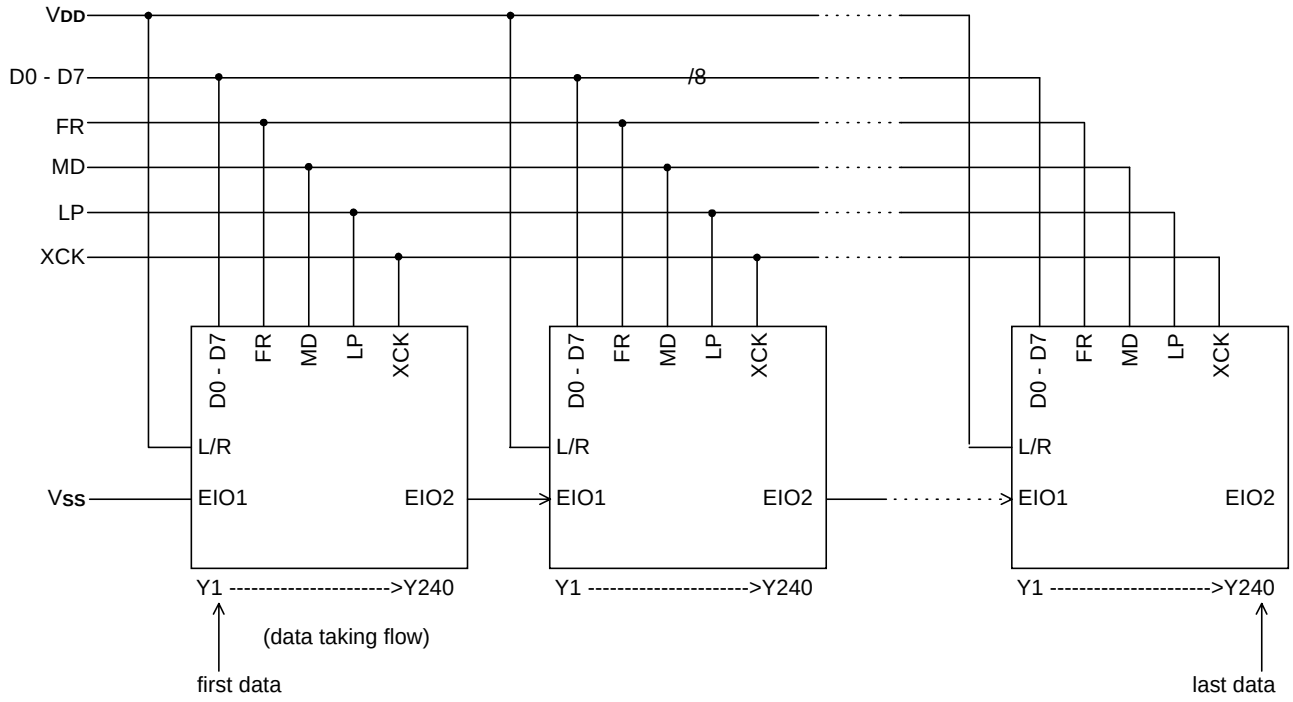
Here, L: V_{SS} (0V), H: V_{DD} (+2.5V to +5.5V), X: Don't care
Note: "Don't care" should be fixed to "H" or "L", avoiding floating.

4. Connection Examples of Segment Drivers

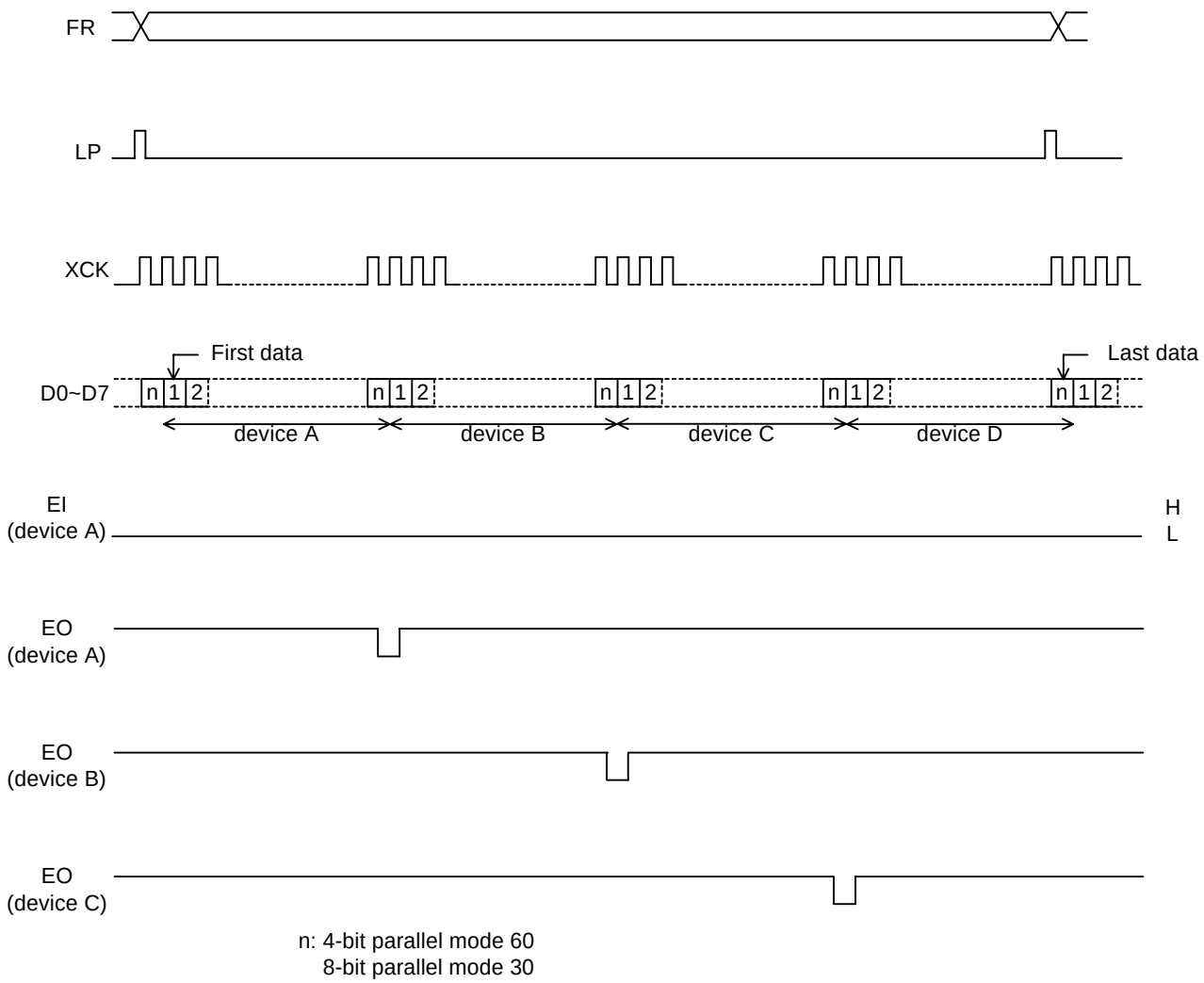
4.1. Case of L/R = "L"



4.2. Case of L/R = "H"

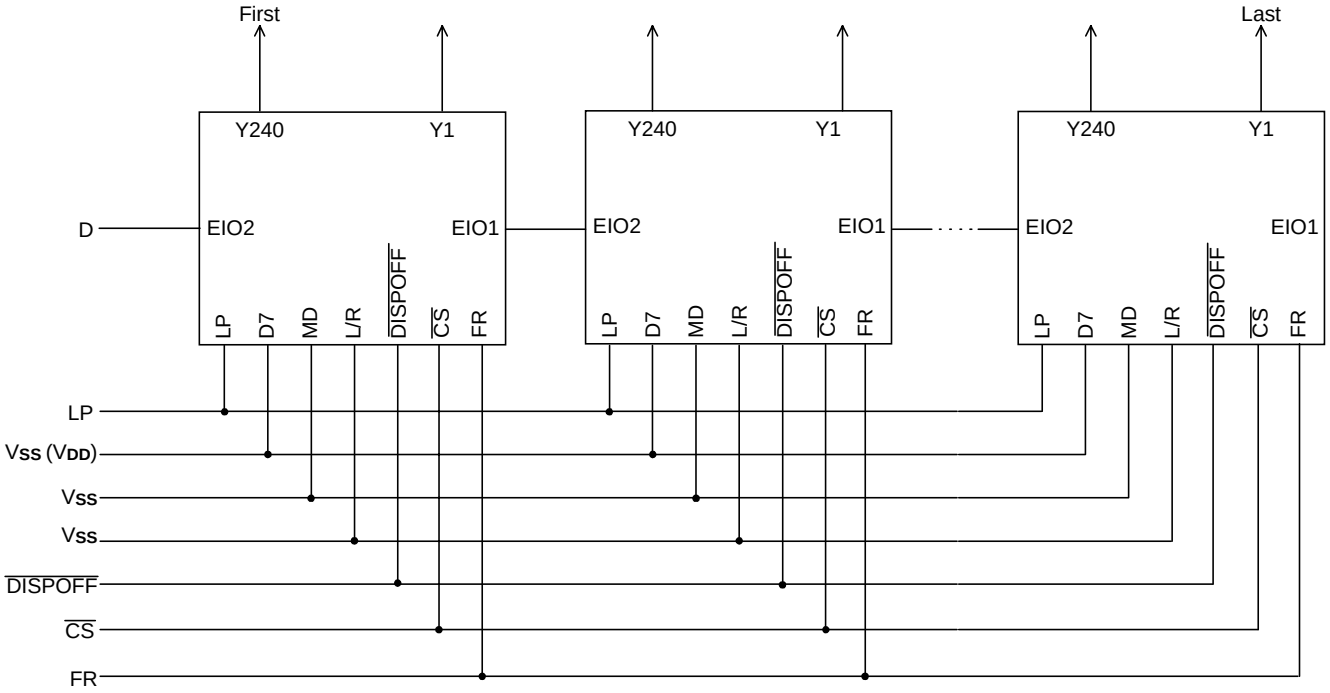


5. Timing waveform of 4-Device cascade Connection of Segment Drivers

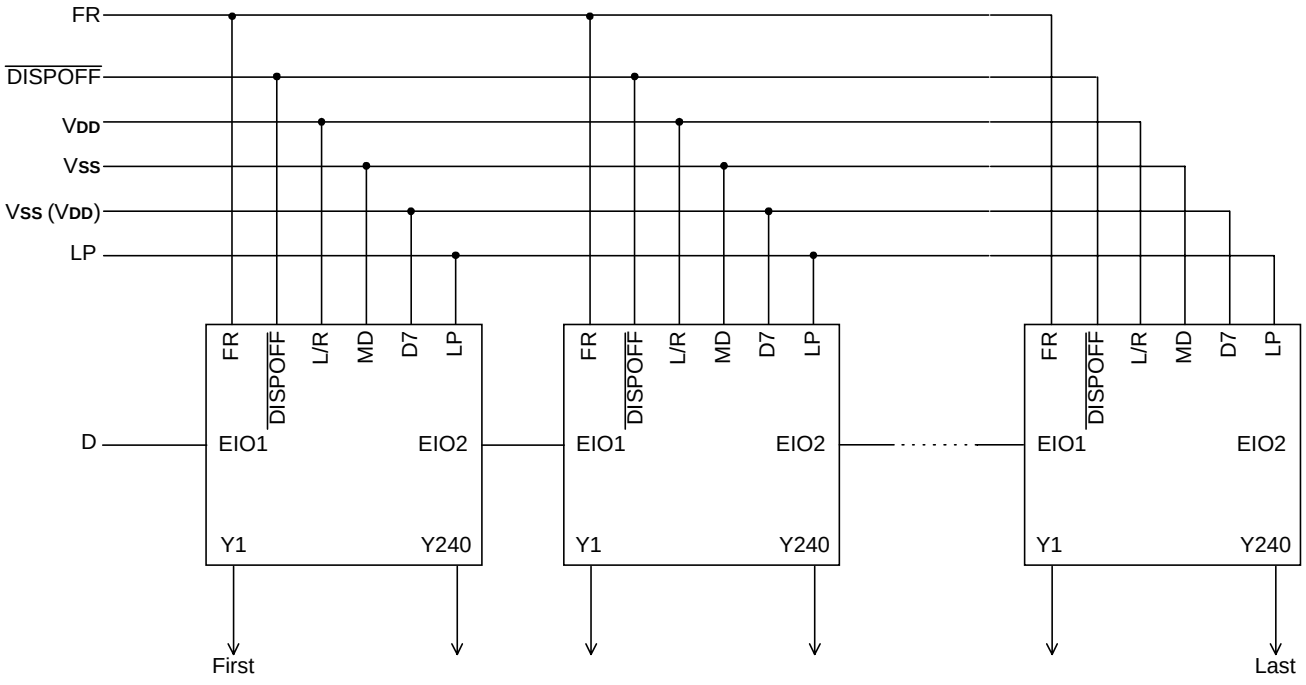


n: 4-bit parallel mode 60
8-bit parallel mode 30

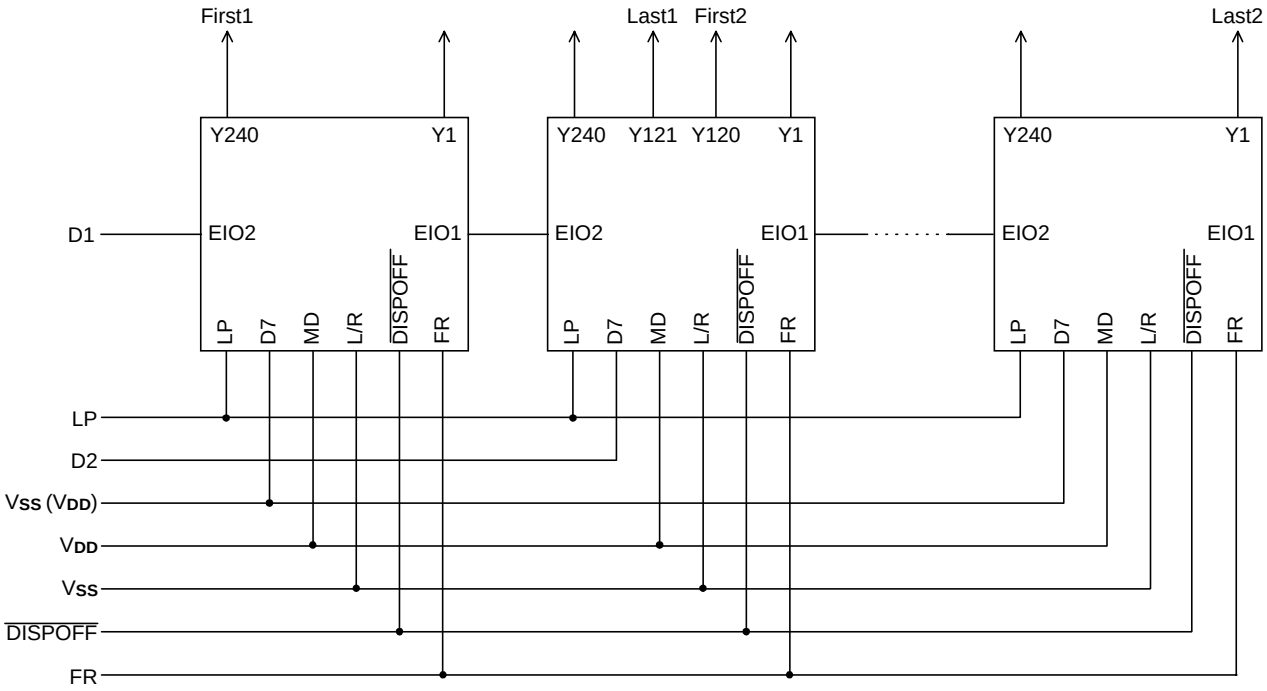
6. Connection Examples for Common Drivers



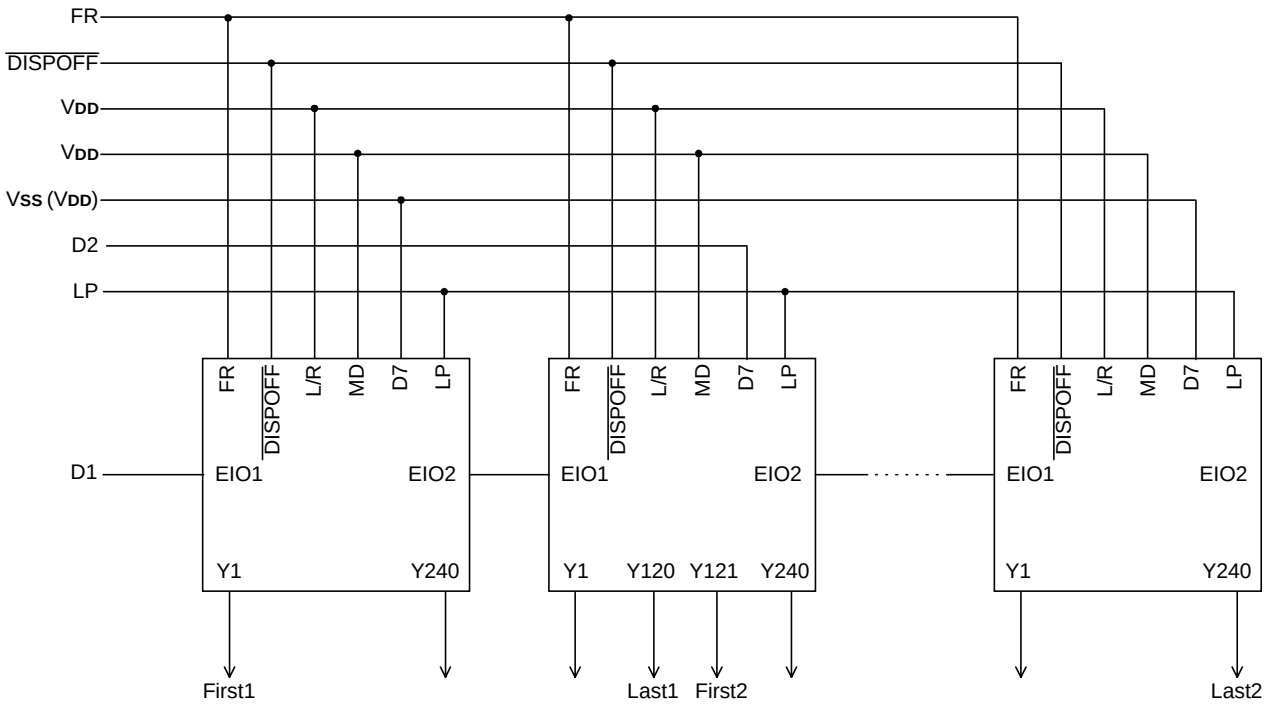
Single Mode (Shifting towards the left)



Single Mode (Sifting towards the right)



Dual mode (Shifting towards the left)



Dual mode (Shifting towards the right)

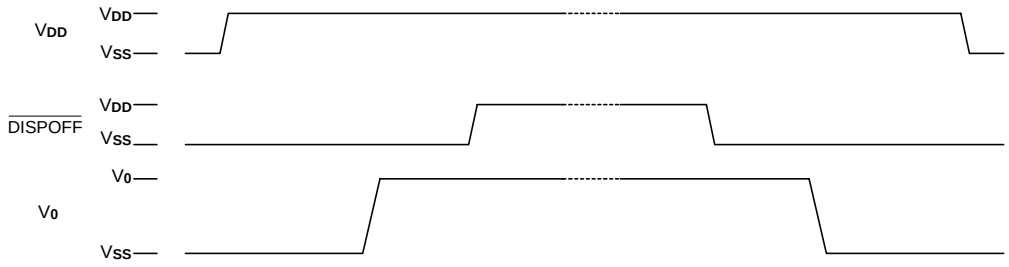
7. Precaution

Be careful when connecting or disconnecting the power

This LSI has a high-voltage LCD driver, so it may be permanently damaged by a high current, which may occur if voltage is supplied to the LCD driver power supply while the logic system power supply is floating.
The details are as follows:

- When connecting the power supply, connect the LCD driver power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD driver power.
- We recommend that you connect a serial resistor (50-100 Ω) or fuse to the LCD driver power V_0 of the system as a current limiting device. Also, set a suitable value of the resistor in consideration of LCD display grade.

In addition, when connecting the logic power supply, the logic condition of the LSI inside is insecure. Therefore, connect the LCD driver power supply only after resetting the logic condition of this LSI inside to the $\overline{\text{DISPOFF}}$ function. After that, the $\overline{\text{DISPOFF}}$ cancel the function after the LCD driver power supply has become stable. Furthermore, when disconnecting the power, set the LCD driver output pins to level V_5 on the $\overline{\text{DISPOFF}}$ function. After that, disconnect the logic system power after disconnecting the LCD driver power.
When connecting the power supply, follow the recommended sequence shown.



Absolute Maximum Rating*

DC Supply Voltage V_{DD} . . . . . -0.3V to +7.0V

DC Supply Voltage V_0 . . . . . -0.3V to +30V

Input Voltage . . . . . -0.3V to V_{DD} +0.3V

Operating Ambient Temperature . . . . -30°C to +85°C

Storage Temperature . . . . . .-45°C to +125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

DC Characteristics

Segment Mode (V_{SS} = V_5 = 0V, V_{DD} = 2.5 - 5.5V, V_0 = 15 to 30 V, and T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage 1	V_{DD}	2.5	-	5.5	V	
Operating Voltage 2	V_0	15	-	30	V	
Input high voltage	V_{IH}	0.8 V_{DD}	-	-	V	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$ pins
Input low voltage	V_{IL}	-	-	0.2 V_{DD}	V	
Output high voltage	V_{OH}	V_{DD} - 0.4	-	-	V	EIO_1, EIO_2 pins, I_{OH} = -0.4mA
Output low voltage	V_{OL}	-	-	+0.4	V	EIO_1, EIO_2 pins, I_{OL} = +0.4mA
Input leakage current 1	I_{IH}	-	-	+1.0	μA	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$ pins, V_I = V_{DD}
Input leakage current 2	I_{IL}	-	-	-1.0	μA	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$ pins, V_I = V_{SS}
Output resistance	R_{ON}	-	1.5	2.0	kΩ	V0 = +30.0V; Y_1 - Y_{240} pins, $\lvert\Delta V_{ON}\rvert$ = 0.5V
		-	2.0	2.5		V0 = +20.0V; Y_1 - Y_{240} pins, $\lvert\Delta V_{ON}\rvert$ = 0.5V
Stand-by current	I_{SB}	-	-	10	μA	V_{SS} pin, Note 1
Consumed current (1) (Deselection)	I_{DD1}	-	-	2	mA	V_{DD} pin, Note 2
Consumed current (2) (Selection)	I_{DD2}	-	-	12	mA	V_{DD} pin, Note 3
Consumed current	I_0	-	-	1.5	mA	V_0 pin, Note 4

Note:

1. V_{DD} = +5.0V, V_0 = +30V, V_I = V_{SS}
2. V_{DD} = +5.0V, V_0 = +30V, f_{XCK} = 20MHz, No-load, EI = V_{DD}
   The input data is turned over by the data taking clock (4-bit Parallel input mode)
3. V_{DD} = +5.0V, V_0 = +30V, f_{XCK} = 20MHz, No-load. EI = V_{SS}
   The input data is turned over by the data taking clock (4-bit parallel input mode)
4. V_{DD} = +5.0V, V_0 = +30V, f_{XCK} = 20MHz, f_{LP} = 41.6kHz. f_{FR} = 80 Hz, No-load
   The input data is turned over by the data taking clock (4-bit parallel-input mode)

Common Mode (V_{SS} = V_5 = 0V, V_{DD} = 2.5 - 5.5V, V_0 = 15 to 30 V, and T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.5	-	5.5	V	
Operating Voltage	V_0	15	-	30	V	
Input high voltage	V_{IH}	0.8 V_{DD}	-	-	V	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$ pins
Input low voltage	V_{IL}	-	-	0.2 V_{DD}	V	
Output high voltage	V_{OH}	V_{DD} - 0.4	-	-	V	EIO_1, EIO_2 pins, I_{OH} = -0.4mA
Output low voltage	V_{OL}	-	-	+0.4	V	EIO_1, EIO_2 pins, I_{OL} = +0.4mA
Input leakage current 1	I_{IH}	-	-	+1.0	µA	D0 - 6, LP, L/R, FR, MD, S/C and $\overline{DISPOFF}$ pins, V_I = V_{DD}
Input leakage current 2	I_{IL}	-	-	-1.0	µA	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, $\overline{DISPOFF}$ pins, V_I = V_{SS}
Input pull down current	I_{PD}	-	-	100	µA	XCK, EIO_1, EIO_2, D7 pins
Output resistance	R_{ON}	-	1.5	2.0	kΩ	V0 = +30.0V; Y_1 - Y_{240} pins, $\lvert\Delta V_{ON}\rvert$ = 0.5V
		-	2.0	2.5		V0 = +20.0V; Y_1 - Y_{240} pins, $\lvert\Delta V_{ON}\rvert$ = 0.5V
Stand-by current	I_{SB}	-	-	10	µA	V_{SS} pin, Note 1
Consumed current (1)	I_{DD}	-	-	120	µA	V_{DD} pin, Note 2
Consumed current (2)	I_0	-	-	240	µA	V_0 pin, Note 2

Note:

1. V_{DD} = +5.0V, V_0 = +30.0V, V_I = V_{SS}
2. V_{DD} = +5.0V, V_0 = +30.0V, f_{LP} = 41.6KHz, f_{FR} = 80Hz, case of 1/480 duty operation, No-load

AC Characteristics

Segment Mode 1 (V_{SS} = V_5 = 0V, V_{DD} = 4.5 - 5.5V, V_0 = 15 to 30V, and T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WCK}	50	-		ns	tr, tf ≦ 10ns, Note 1
Shift clock "H" pulse width	t_{WCKH}	15	-		ns	
Shift clock "L" pulse width	t_{WCKL}	15	-		ns	
Data setup time	t_{DS}	10	-		ns	
Data hole time	t_{DH}	12	-		ns	
Latch pulse "H" pulse width	t_{WLPH}	15	-		ns	
Shift clock rise to Latch pulse rise time	t_{LD}	0	-		ns	
Shift clock fall to Latch pulse fall time	t_{SL}	30	-		ns	
Latch pulse rise to Shift clock rise time	t_{LS}	25	-		ns	
Latch pulse fall to Shift clock rise time	t_{LH}	25	-		ns	
Input signal rise time	t_r		-	50	ns	Note 2
Input signal fall time	t_f		-	50	ns	Note 2
Enable setup time	t_S	10	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	t_{SD}	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t_{WDL}	1.2	-		μs	
Output delay time (1)	t_D		-	30	ns	CL = 15pF
Output delay time (2)	t_{pd1}, t_{pd2}		-	1.2	μs	CL = 15pF
Output delay time (3)	t_{pd3}		-	1.2	μs	CL = 15pF

Note:

1. Take the cascade connection into consideration.
2. (t_{CK}-t_{WCKII}-t_{wckI})/2 is the maximum in the case of high speed operation.

Segment Mode 2 (V_{SS} = V_5 = 0V, V_{DD} = 3.0 - 4.5V, V_0 = 15 to 30V, and T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WCK}	66	-		ns	tr, tf ≦ 10ns, Note 1
Shift clock "H" pulse width	t_{WCKH}	23	-		ns	
Shift clock "L" pulse width	t_{WCKL}	23	-		ns	
Data setup time	t_{DS}	15	-		ns	
Data hole time	t_{DH}	23	-		ns	
Latch pulse "H" pulse width	t_{WLPH}	30	-		ns	
Shift clock rise to Latch pulse rise time	t_{LD}	0	-		ns	
Shift clock fall to Latch pulse fall time	t_{SL}	50	-		ns	
Latch pulse rise to Shift clock rise time	t_{LS}	30	-		ns	
Latch pulse fall to Shift clock fall time	t_{LH}	30	-		ns	
Input signal rise time	t_r		-	50	ns	Note 2
Input signal fall time	t_f		-	50	ns	Note 2
Enable setup time	t_S	15	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	t_{SD}	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t_{WDL}	1.2	-		µs	
Output delay time (1)	t_D		-	41	ns	CL = 15pF
Output delay time (2)	t_{pd1}, t_{pd2}		-	1.2	µs	CL = 15pF
Output delay time (3)	t_{pd3}		-	1.2	µs	CL = 15pF

Note:

1. Take the cascade connection into consideration.
2. (t_{CK}-t_{WCKII}-t_{WCKL})/2 is the maximum in the case of high speed operation.

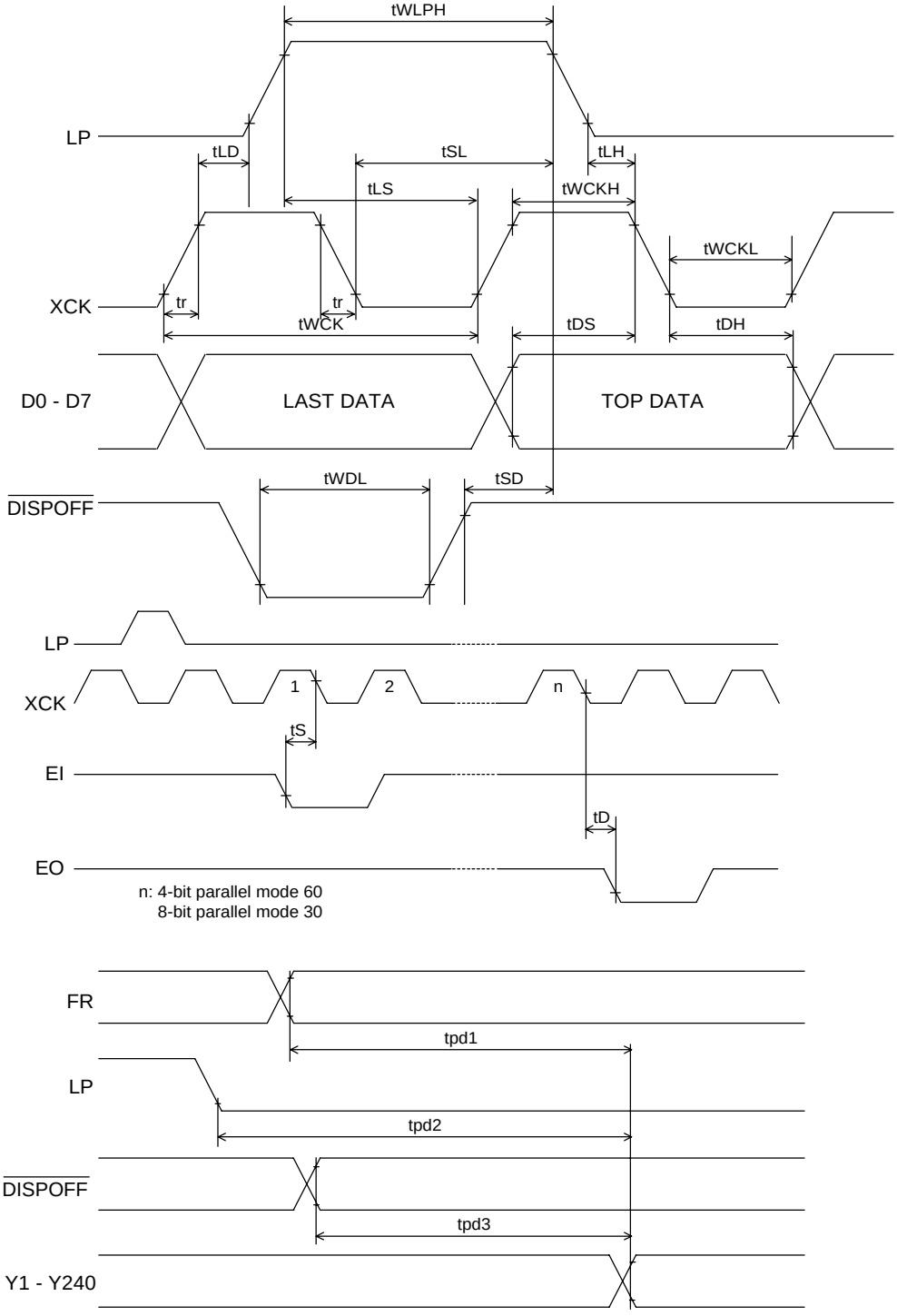
Segment Mode 3 (V_{SS} = V_5 = 0V, V_{DD} = 2.5 - 3.0V, V_0 = 15 to 30V, and T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WCK}	82	-		ns	tr, tf ≦ 10ns, Note 1
Shift clock "H" pulse width	t_{WCKH}	28	-		ns	
Shift clock "L" pulse width	t_{WCKL}	28	-		ns	
Data setup time	t_{DS}	20	-		ns	
Data hole time	t_{DH}	23	-		ns	
Latch pulse "H" pulse width	t_{WLPH}	30	-		ns	
Shift clock rise to Latch pulse rise time	t_{LD}	0	-		ns	
Shift clock fall to Latch pulse fall time	t_{SL}	65	-		ns	
Latch pulse rise to Shift clock rise time	t_{LS}	30	-		ns	
Latch pulse fall to Shift clock fall time	t_{LH}	30	-		ns	
Input signal rise time	t_r		-	50	ns	Note 2
Input signal fall time	t_f		-	50	ns	Note 2
Enable setup time	t_S	15	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	t_{SD}	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t_{WDL}	1.2	-		μs	
Output delay time (1)	t_D		-	57	ns	CL = 15pF
Output delay time (2)	t_{pd1}, t_{pd2}		-	1.2	μs	CL = 15pF
Output delay time (3)	t_{pd3}		-	1.2	μs	CL = 15pF

Note:

1. Take the cascade connection into consideration.
2. (t_{CK}-t_{WCKH}-t_{WCKL})/2 is the maximum in the case of high speed operation.

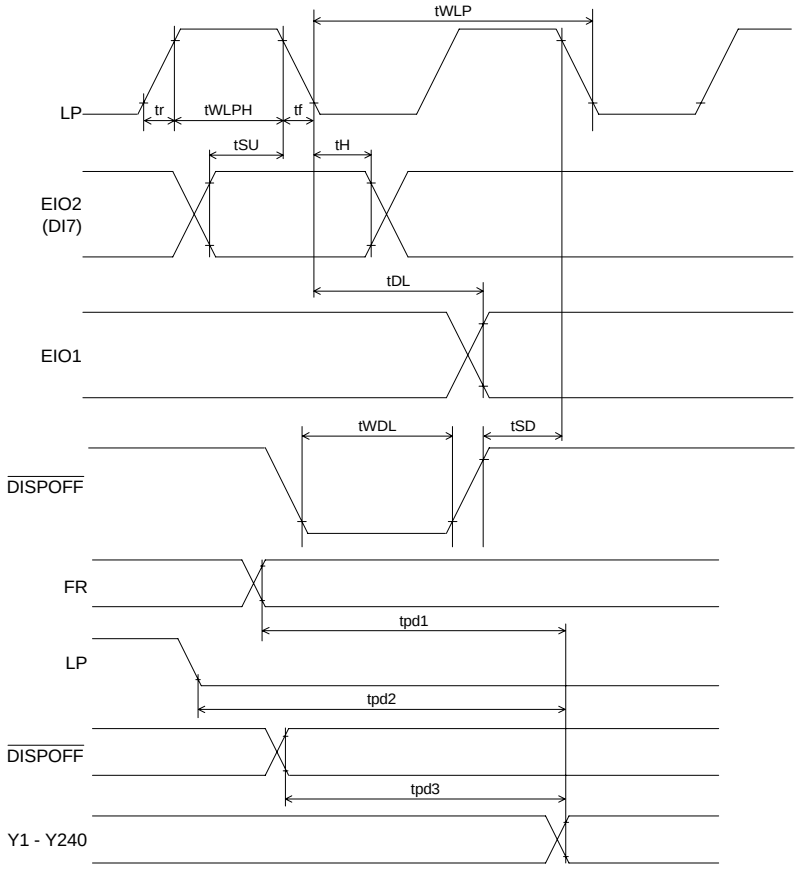
Timing waveform of the Segment Mode



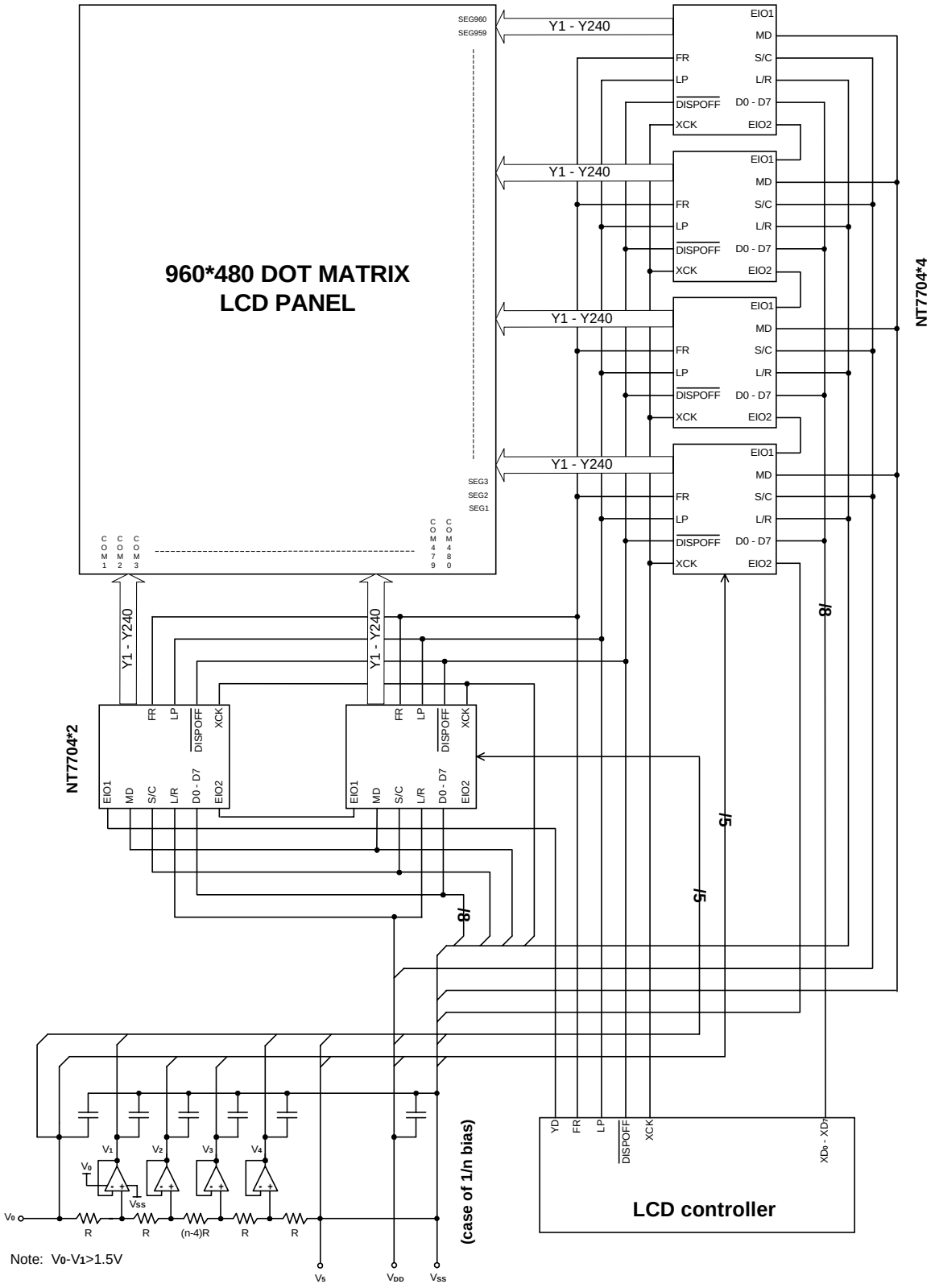
Common Mode (V_{SS} = V_5 = 0V, V_{DD} = 2.5 - 5.5V, V_0 = 15 to 30V and T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WLP}	250	-	-	ns	t_r, t_f ≦ 20ns
Shift clock "H" pulse width	t_{WLPH}	15	-	-	ns	V_{DD} = +5.0V ± 10%
		30	-	-	ns	V_{DD} = +2.5 - +4.5V
Data setup time	t_{SU}	30	-	-	ns	
Data hole time	t_H	50	-	-	ns	
Input signal rise time	t_r		-	50	ns	
Input signal fall time	t_f		-	50	ns	
$\overline{\text{DISPOFF}}$ Removal time	t_{SD}	100	-	-	ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t_{WDL}	1.2	-	-	µs	
Output delay time (1)	t_{DL}	-	-	200	ns	C_L = 15pF
Output delay time (2)	t_{pd1}, t_{pd2}	-	-	1.2	µs	C_L = 15pF
Output delay time (3)	t_{pd3}	-	-	1.2	µs	C_L = 15pF

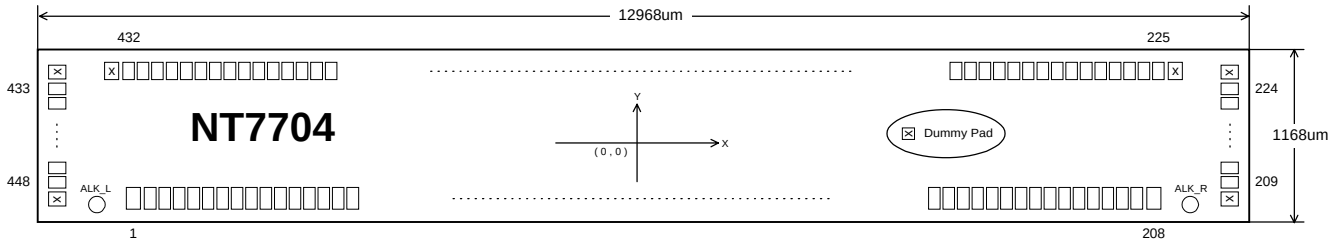
Timing Characteristics of Common Mode



Application Circuit (for reference only)



Bonding Diagram



Pad Location

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	V_{0L}	-6220	-521	31	V_{5L}	-4410	-521
2	V_{0L}	-6150	-521	32	V_{5L}	-4350	-521
3	V_{0L}	-6090	-521	33	V_{5L}	-4290	-521
4	V_{0L}	-6030	-521	34	V_{5L}	-4230	-521
5	V_{0L}	-5970	-521	35	V_{5L}	-4170	-521
6	V_{0L}	-5910	-521	36	V_{5L}	-4110	-521
7	V_{0L}	-5850	-521	37	V_{5L}	-4050	-521
8	V_{0L}	-5790	-521	38	V_{5L}	-3990	-521
9	V_{0L}	-5730	-521	39	V_{5L}	-3930	-521
10	V_{0L}	-5670	-521	40	V_{5L}	-3870	-521
11	V_{0L}	-5610	-521	41	V_{SS}	-3810	-521
12	V_{0L}	-5550	-521	42	V_{SS}	-3750	-521
13	V_{12L}	-5490	-521	43	V_{SS}	-3690	-521
14	V_{12L}	-5430	-521	44	V_{SS}	-3630	-521
15	V_{12L}	-5370	-521	45	V_{SS}	-3570	-521
16	V_{12L}	-5310	-521	46	V_{SS}	-3510	-521
17	V_{12L}	-5250	-521	47	V_{SS}	-3450	-521
18	V_{12L}	-5190	-521	48	V_{SS}	-3390	-521
19	V_{12L}	-5130	-521	49	V_{SS}	-3330	-521
20	V_{12L}	-5070	-521	50	V_{SS}	-3270	-521
21	V_{43L}	-5010	-521	51	V_{SS}	-3210	-521
22	V_{43L}	-4950	-521	52	V_{SS}	-3150	-521
23	V_{43L}	-4890	-521	53	V_{SS}	-3090	-521
24	V_{43L}	-4830	-521	54	V_{SS}	-3030	-521
25	V_{43L}	-4770	-521	55	V_{SS}	-2970	-521
26	V_{43L}	-4710	-521	56	V_{SS}	-2910	-521
27	V_{43L}	-4650	-521	57	V_{SS}	-2850	-521
28	V_{43L}	-4590	-521	58	V_{SS}	-2790	-521
29	V_{5L}	-4530	-521	59	V_{SS}	-2730	-521
30	V_{5L}	-4470	-521	60	V_{SS}	-2670	-521

Pad Location (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
61	V_{SS}	-2610	-521	101	D1	-210	-521
62	V_{SS}	-2550	-521	102	D1	-150	-521
63	V_{SS}	-2490	-521	103	D1	-90	-521
64	V_{SS}	-2430	-521	104	D2	-30	-521
65	V_{SS}	-2370	-521	105	D2	30	-521
66	V_{SS}	-2310	-521	106	D2	90	-521
67	V_{DD}	-2250	-521	107	D3	150	-521
68	V_{DD}	-2190	-521	108	D3	210	-521
69	V_{DD}	-2130	-521	109	D3	270	-521
70	V_{DD}	-2070	-521	110	D4	330	-521
71	V_{DD}	-2010	-521	111	D4	390	-521
72	V_{DD}	-1950	-521	112	D4	450	-521
73	V_{DD}	-1890	-521	113	D5	510	-521
74	V_{DD}	-1830	-521	114	D5	570	-521
75	V_{DD}	-1770	-521	115	D5	630	-521
76	V_{DD}	-1710	-521	116	D6	690	-521
77	V_{DD}	-1650	-521	117	D6	750	-521
78	V_{DD}	-1590	-521	118	D6	810	-521
79	V_{DD}	-1530	-521	119	D7	870	-521
80	V_{DD}	-1470	-521	120	D7	930	-521
81	V_{DD}	-1410	-521	121	D7	990	-521
82	V_{DD}	-1350	-521	122	XCK	1050	-521
83	V_{DD}	-1290	-521	123	XCK	1110	-521
84	V_{DD}	-1230	-521	124	XCK	1170	-521
85	V_{DD}	-1170	-521	125	$\overline{\text{DISPOFF}}$	1230	-521
86	V_{DD}	-1110	-521	126	$\overline{\text{DISPOFF}}$	1290	-521
87	V_{DD}	-1050	-521	127	$\overline{\text{DISPOFF}}$	1350	-521
88	V_{DD}	-990	-521	128	LP	1410	-521
89	V_{DD}	-930	-521	129	LP	1470	-521
90	V_{DD}	-870	-521	130	LP	1530	-521
91	V_{DD}	-810	-521	131	EIO_1	1590	-521
92	V_{DD}	-750	-521	132	EIO_1	1650	-521
93	S/C	-690	-521	133	EIO_1	1710	-521
94	S/C	-630	-521	134	FR	1770	-521
95	EIO_2	-570	-521	135	FR	1830	-521
96	EIO_2	-510	-521	136	FR	1890	-521
97	EIO_2	-450	-521	137	L/R	1950	-521
98	D0	-390	-521	139	L/R	2010	-521
99	D0	-330	-521	139	L/R	2070	-521
100	D0	-270	-521	140	MD	2130	-521

Pad Location (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
141	MD	2190	-521	181	V_{43R}	4590	-521
142	MD	2250	-521	182	V_{43R}	4650	-521
143	V_{SS}	2310	-521	183	V_{43R}	4710	-521
144	V_{SS}	2370	-521	184	V_{43R}	4770	-521
145	V_{SS}	2430	-521	185	V_{43R}	4830	-521
146	V_{SS}	2490	-521	186	V_{43R}	4890	-521
147	V_{SS}	2550	-521	187	V_{43R}	4950	-521
148	V_{SS}	2610	-521	188	V_{43R}	5010	-521
149	V_{SS}	2670	-521	189	V_{12R}	5070	-521
150	V_{SS}	2730	-521	190	V_{12R}	5130	-521
151	V_{SS}	2790	-521	191	V_{12R}	5190	-521
152	V_{SS}	2850	-521	192	V_{12R}	5250	-521
153	V_{SS}	2910	-521	193	V_{12R}	5310	-521
154	V_{SS}	2970	-521	194	V_{12R}	5370	-521
155	V_{SS}	3030	-521	195	V_{12R}	5430	-521
156	V_{SS}	3090	-521	196	V_{12R}	5490	-521
157	V_{SS}	3150	-521	197	V_{0R}	5550	-521
158	V_{SS}	3210	-521	198	V_{0R}	5610	-521
159	V_{SS}	3270	-521	199	V_{0R}	5670	-521
160	V_{SS}	3330	-521	200	V_{0R}	5730	-521
161	V_{SS}	3390	-521	201	V_{0R}	5790	-521
162	V_{SS}	3450	-521	202	V_{0R}	5850	-521
163	V_{SS}	3510	-521	203	V_{0R}	5910	-521
164	V_{SS}	3570	-521	204	V_{0R}	5970	-521
165	V_{SS}	3630	-521	205	V_{0R}	6030	-521
166	V_{SS}	3690	-521	206	V_{0R}	6090	-521
167	V_{SS}	3750	-521	207	V_{0R}	6150	-521
168	V_{SS}	3810	-521	208	V_{0R}	6220	-521
169	V_{5R}	3870	-521	209	Y1	6430	-450
170	V_{5R}	3930	-521	210	Y2	6430	-390
171	V_{5R}	3990	-521	211	Y3	6430	-330
172	V_{5R}	4050	-521	212	Y4	6430	-270
173	V_{5R}	4110	-521	213	Y5	6430	-210
174	V_{5R}	4170	-521	214	Y6	6430	-150
175	V_{5R}	4230	-521	215	Y7	6430	-90
176	V_{5R}	4290	-521	216	Y8	6430	-30
177	V_{5R}	4350	-521	217	Y9	6430	30
178	V_{5R}	4410	-521	218	Y10	6430	90
179	V_{5R}	4470	-521	219	Y11	6430	150
180	V_{5R}	4530	-521	220	Y12	6430	210

Pad Location (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
221	Y13	6430	270	261	Y53	4050	529
222	Y14	6430	330	262	Y54	3990	529
223	Y15	6430	390	263	Y55	3930	529
224	Y16	6430	450	264	Y56	3870	529
225	Y17	6210	529	265	Y57	3810	529
226	Y18	6150	529	266	Y58	3750	529
227	Y19	6090	529	267	Y59	3690	529
228	Y20	6030	529	268	Y60	3630	529
229	Y21	5970	529	269	Y61	3570	529
230	Y22	5910	529	270	Y62	3510	529
231	Y23	5850	529	271	Y63	3450	529
232	Y24	5790	529	272	Y64	3390	529
233	Y25	5730	529	273	Y65	3330	529
234	Y26	5670	529	274	Y66	3270	529
235	Y27	5610	529	275	Y67	3210	529
236	Y28	5550	529	276	Y68	3150	529
237	Y29	5490	529	277	Y69	3090	529
238	Y30	5430	529	278	Y70	3030	529
239	Y31	5370	529	279	Y71	2970	529
240	Y32	5310	529	280	Y72	2910	529
241	Y33	5250	529	281	Y73	2850	529
242	Y34	5190	529	282	Y74	2790	529
243	Y35	5130	529	283	Y75	2730	529
244	Y36	5070	529	284	Y76	2670	529
245	Y37	5010	529	285	Y77	2610	529
246	Y38	4950	529	286	Y78	2550	529
247	Y39	4890	529	287	Y79	2490	529
248	Y40	4830	529	288	Y80	2430	529
249	Y41	4770	529	289	Y81	2370	529
250	Y42	4710	529	290	Y82	2310	529
251	Y43	4650	529	291	Y83	2250	529
252	Y44	4590	529	292	Y84	2190	529
253	Y45	4530	529	293	Y85	2130	529
254	Y46	4470	529	294	Y86	2070	529
255	Y47	4410	529	295	Y87	2010	529
256	Y48	4350	529	296	Y88	1950	529
257	Y49	4290	529	297	Y89	1890	529
258	Y50	4230	529	298	Y90	1830	529
259	Y51	4170	529	299	Y91	1770	529
260	Y52	4110	529	300	Y92	1710	529

Pad Location (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
301	Y93	1650	529	341	Y133	-750	529
302	Y94	1590	529	342	Y134	-810	529
303	Y95	1530	529	343	Y135	-870	529
304	Y96	1470	529	344	Y136	-930	529
305	Y97	1410	529	345	Y137	-990	529
306	Y98	1350	529	346	Y138	-1050	529
307	Y99	1290	529	347	Y139	-1110	529
308	Y100	1230	529	348	Y140	-1170	529
309	Y101	1170	529	349	Y141	-1230	529
310	Y102	1110	529	350	Y142	-1290	529
311	Y103	1050	529	351	Y143	-1350	529
312	Y104	990	529	352	Y144	-1410	529
313	Y105	930	529	353	Y145	-1470	529
314	Y106	870	529	354	Y146	-1530	529
315	Y107	810	529	355	Y147	-1590	529
316	Y108	750	529	356	Y148	-1650	529
317	Y109	690	529	357	Y149	-1710	529
318	Y110	630	529	358	Y150	-1770	529
319	Y111	570	529	359	Y151	-1830	529
320	Y112	510	529	360	Y152	-1890	529
321	Y113	450	529	361	Y153	-1950	529
322	Y114	390	529	362	Y154	-2010	529
323	Y115	330	529	363	Y155	-2070	529
324	Y116	270	529	364	Y156	-2130	529
325	Y117	210	529	365	Y157	-2190	529
326	Y118	150	529	366	Y158	-2250	529
327	Y119	90	529	367	Y159	-2310	529
328	Y120	30	529	368	Y160	-2370	529
329	Y121	-30	529	369	Y161	-2430	529
330	Y122	-90	529	370	Y162	-2490	529
331	Y123	-150	529	371	Y163	-2550	529
332	Y124	-210	529	372	Y164	-2610	529
333	Y125	-270	529	373	Y165	-2670	529
334	Y126	-330	529	374	Y166	-2730	529
335	Y127	-390	529	375	Y167	-2790	529
336	Y128	-450	529	376	Y168	-2850	529
337	Y129	-510	529	377	Y169	-2910	529
338	Y130	-570	529	378	Y170	-2970	529
339	Y131	-630	529	379	Y171	-3030	529
340	Y132	-690	529	380	Y172	-3090	529

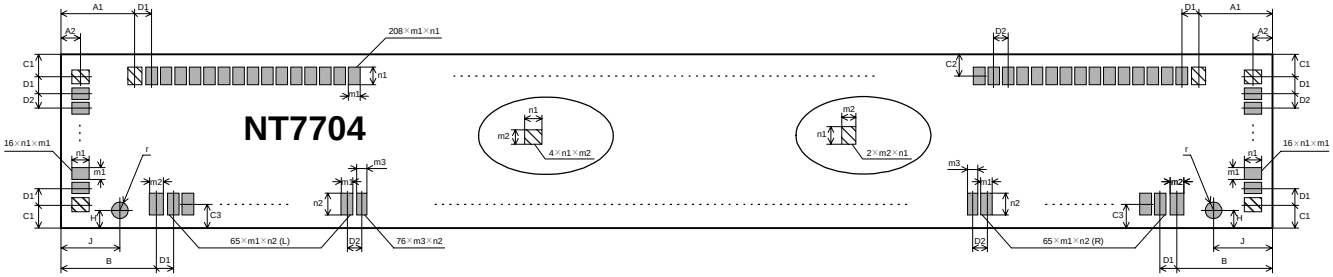
Pad Location (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
381	Y173	-3150	529	416	Y208	-5250	529
382	Y174	-3210	529	417	Y209	-5310	529
383	Y175	-3270	529	418	Y210	-5370	529
384	Y176	-3330	529	419	Y211	-5430	529
385	Y177	-3390	529	420	Y212	-5490	529
386	Y178	-3450	529	421	Y213	-5550	529
387	Y179	-3510	529	422	Y214	-5610	529
388	Y180	-3570	529	423	Y215	-5670	529
389	Y181	-3630	529	424	Y216	-5730	529
390	Y182	-3690	529	425	Y217	-5790	529
391	Y183	-3750	529	426	Y218	-5850	529
392	Y184	-3810	529	427	Y219	-5910	529
393	Y185	-3870	529	428	Y220	-5970	529
394	Y186	-3930	529	429	Y221	-6030	529
395	Y187	-3990	529	430	Y222	-6090	529
396	Y188	-4050	529	431	Y223	-6150	529
397	Y189	-4110	529	432	Y224	-6210	529
398	Y190	-4170	529	433	Y225	-6430	450
399	Y191	-4230	529	434	Y226	-6430	390
400	Y192	-4290	529	435	Y227	-6430	330
401	Y193	-4350	529	436	Y228	-6430	270
402	Y194	-4410	529	437	Y229	-6430	210
403	Y195	-4470	529	438	Y230	-6430	150
404	Y196	-4530	529	439	Y231	-6430	90
405	Y197	-4590	529	440	Y232	-6430	30
406	Y198	-4650	529	441	Y233	-6430	-30
407	Y199	-4710	529	442	Y234	-6430	-90
408	Y200	-4770	529	443	Y235	-6430	-150
409	Y201	-4830	529	444	Y236	-6430	-210
410	Y202	-4890	529	445	Y237	-6430	-270
411	Y203	-4950	529	446	Y238	-6430	-330
412	Y204	-5010	529	447	Y239	-6430	-390
413	Y205	-5070	529	448	Y240	-6430	-450
414	Y206	-5130	529		ALK_L	-6318	-533
415	Y207	-5190	529		ALK_R	6318	-533

Dummy Pad Location (Total: 6 pin)

NO.	X	Y	NO.	X	Y
1	6430	-520	4	-6280	529
2	6430	520	5	-6430	520
3	6280	529	6	-6430	-520

Package Information

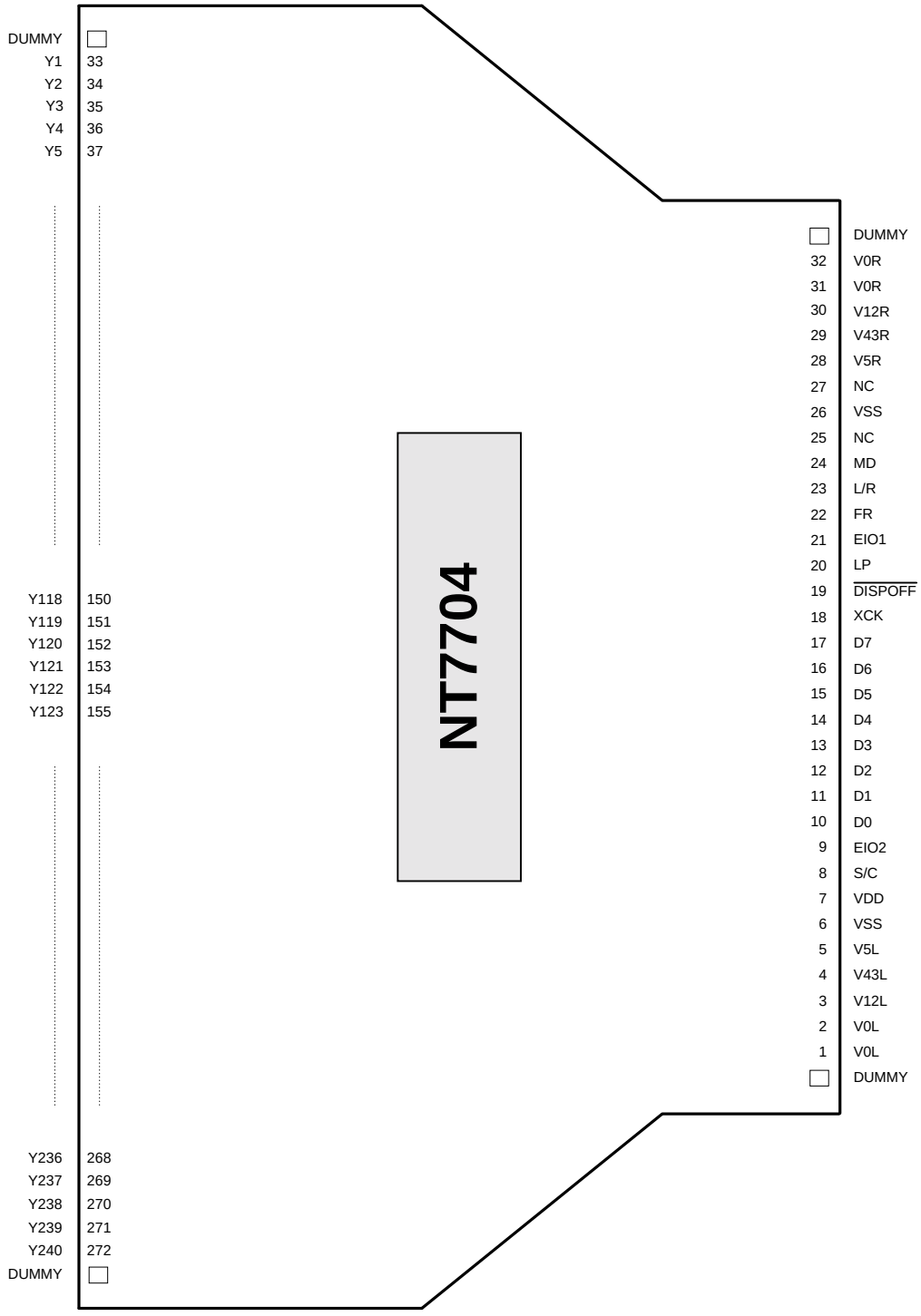


Chip Outline Dimensions

unit: um

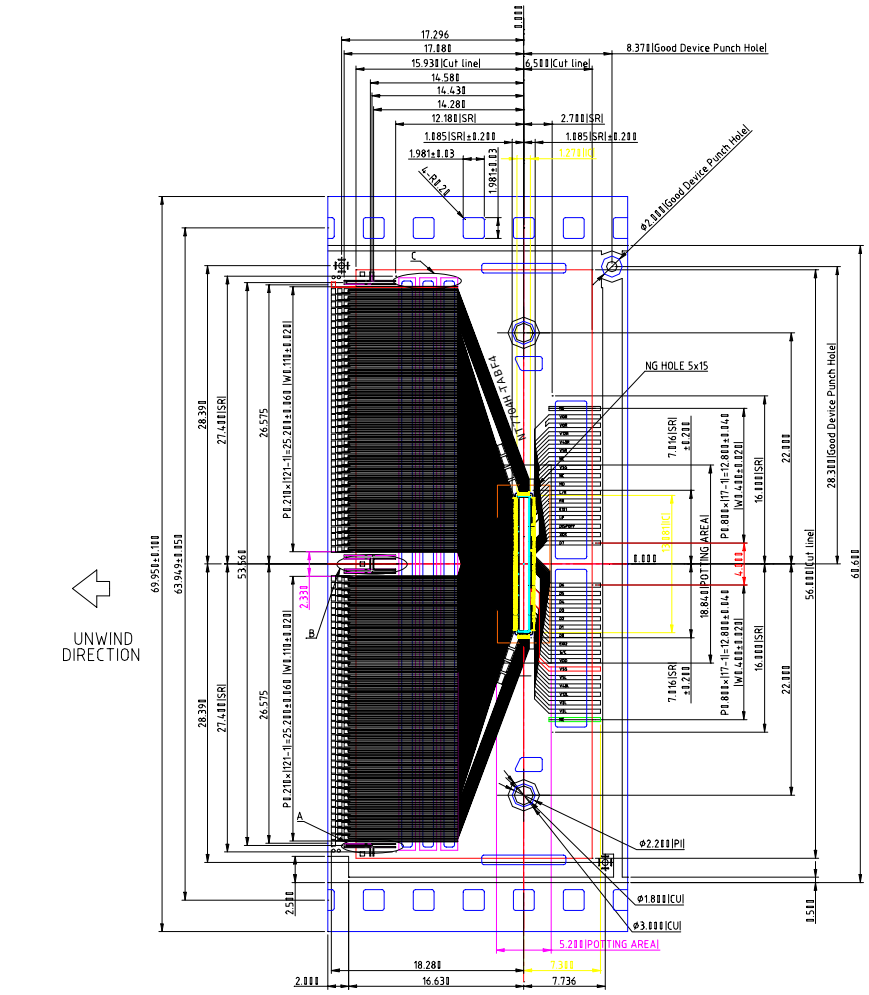
Symbol	Dimensions in um	Symbol	Dimensions in um
A1	204	H	51
A2	54	J	166
B	264	m1	39
C1	64	m2	55
C2	55	m3	38
C3	63	n1	72
D1	70	n2	90
D2	60	r	35

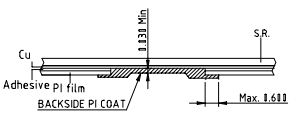
TCP Pin Layout



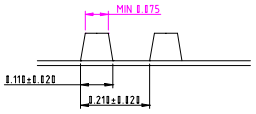
(COPPER SIDE VIEW)

External View of TCP Pins

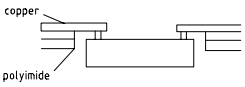




Detail of flex



FINISH VALUE
|OUTPUT|



Show the IC side

NOTE:

1.GENERAL TOLERANCE: ±0.050MM

2.ALL CHAMFER IS R0.200

3.MATERIAL

PI: UPILEX-S 75±6umTHICKNESS

ADHESIVE: TORAY #7100 12±2um THICKNESS

CU: FQ-VLP 25um

FLEX COATING: FS-100L

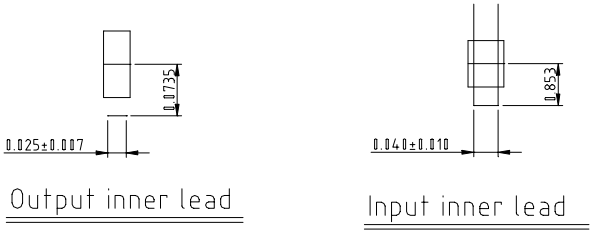
SOLDER RESIST :AE-70-M11 20±15um

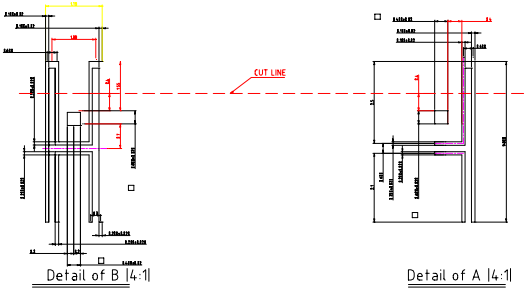
OTHER TOLERANCE IS±0.200mm

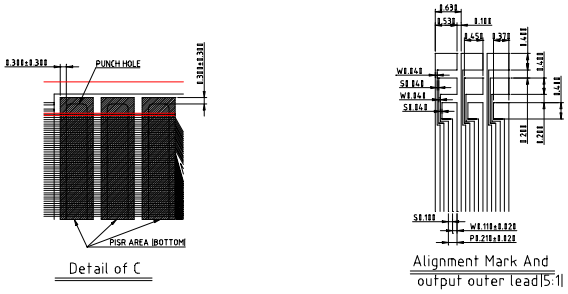
4.PLATING

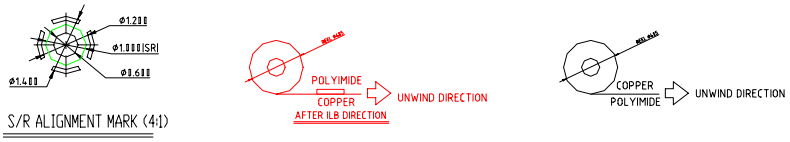
SN: 0.20±0.05um

5. 6 SPROCKET HOLES|28.5mm| FOR 1 TAPESITE









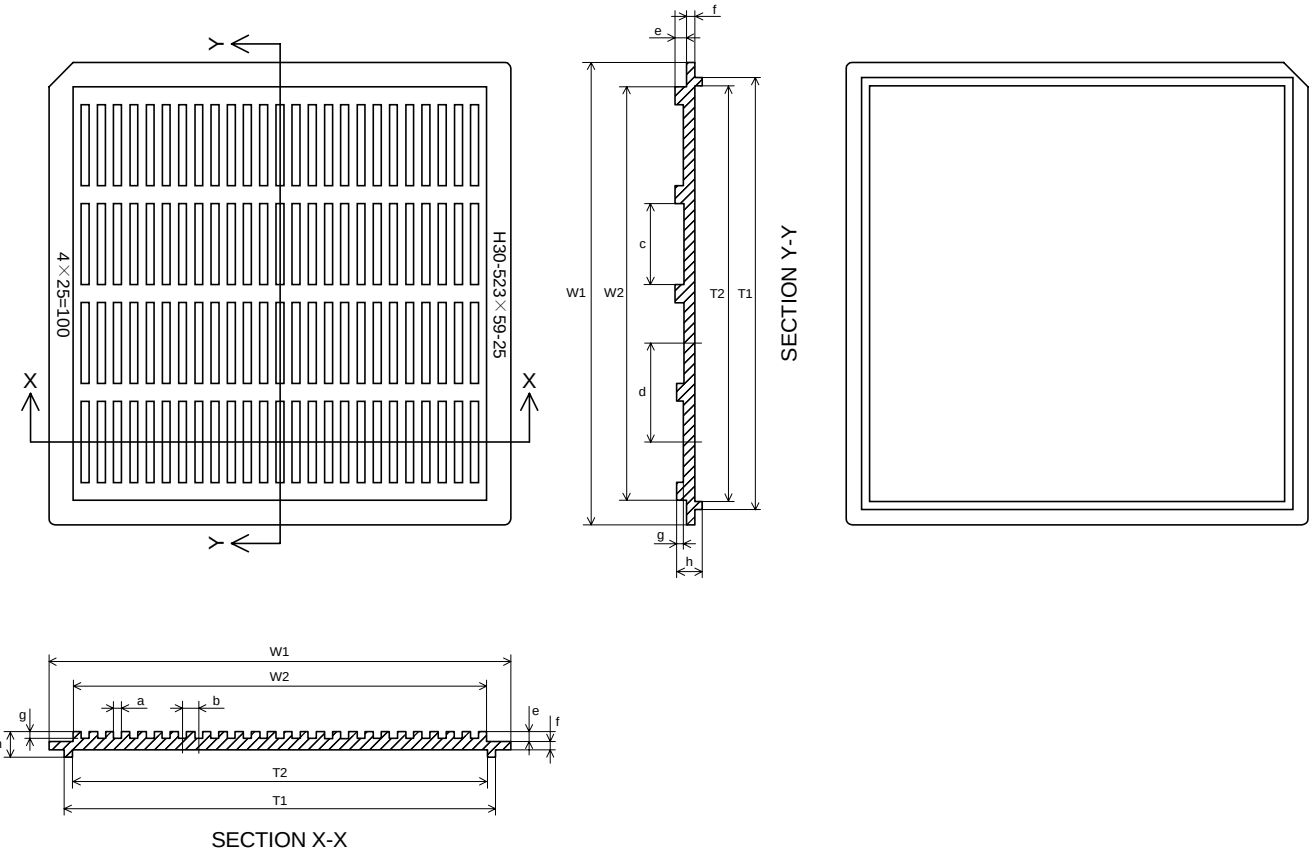
Cautions concerning storage:

1. When storing the product, it is recommended that it be left in its shipping package.
   After the seal of the packing bag has been broke, store the products in a nitrogen atmosphere.
2. Storage conditions :

Storage state	Storage conditions
unopened **(less than 90 days)**	Temperature: 5 to 30℃; humidity: 80%RH or less
After seal of broken **(less than 30 days)**	Room temperature, dry nitrogen atmosphere

3. Don't store in a location exposed to corrosive gas or excessive dust.
4. Don't store in a location exposed to direct sunlight of subject to sharp changes in temperature.
5. Don't store the product such that it is subjected to an excessive load weight, such as by stacking.
6. Deterioration of the plating may occur after long-term storage, so special care is required.
   It is recommended that the products be inspected before use.

Tray Information



Tray Outline Dimensions

unit: mm

Symbol	Dimensions in mm	Symbol	Dimensions in mm
a	1.30	g	0.64
b	2.67	h	4.20
c	13.30	W1	76.0
d	16.26	W2	68.0
e	1.60	T1	71.0
f	1.40	T2	68.3

Ordering Information

Part No.	Package
NT7704H-BDT	Au bump on chip tray
NT7704H-TABF4	TCP Form

Product Spec. Change Notice

NT7704 Specification Revision History		
Version	**Content**	**Date**
1.0	TCP and tray information addition (Page 36-39)	Dec. 2001
0.2	Gold Bump Size revision (Page 34) m1: 45 → 39, m2: 58 → 55	Sep. 2001
0.1	Pad Location Addition	Nov. 2000
0.0	Original	Nov. 2000