SMP60N06-18

Siliconix

N-Channel Enhancement-Mode Transistor, 18-mΩ $r_{DS(on)}$
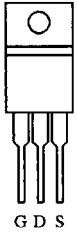
175°C Maximum Junction Temperature[a]

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.018	60

See lower-cost version: SUP50N06-18

TO-220AB

DRAIN connected to TAB

G D S

Top View
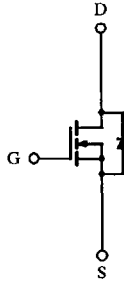
N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	T_C = 25°C	I_D	60	A
	T_C = 100°C		41	
Pulsed Drain Current		I_{DM}	240	
Avalanche Current		I_{AR}	60	
Avalanche Energy	L = 0.1 mH	I_{AR}	180	mJ
Repetitive Avalanche Energy[a]	L = 0.1 mH	E_{AR}	90	
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		62	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C
Lead Temperature (1/16" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		80	°C/W
Junction-to-Case	R_{thJC}		1.2	
Case-to-Sink	R_{thCS}	1.0		

Notes:
a.   Duty cycle ≤1%

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Specifications ($T_J = 25°C$ Unless Otherwise Noted)

| Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0 V$, $I_D = 250 \mu A$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_{DS} = 1 mA$	2.0		4.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 V$, $V_{GS} = \pm 20 V$			± 500	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 48 V$, $V_{GS} = 0 V$			25	μA
		$V_{DS} = 48 V$, $V_{GS} = 0 V$, $T_J = 125°C$			250	
		$V_{DS} = 48 V$, $V_{GS} = 0 V$, $T_J = 175°C$			500	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} = 10 V$, $V_{GS} = 10 V$	60			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	$V_{GS} = 10 V$, $I_D = 30 A$		0.013	0.018	Ω
		$V_{GS} = 10 V$, $I_D = 30 A$, $T_J = 125°C$		0.023	0.030	
		$V_{GS} = 10 V$, $I_D = 30 A$, $T_J = 175°C$		0.026	0.036	
Forward Transconductance[b]	g_{fs}	$V_{DS} = 15 V$, $I_D = 30 A$		45		S
Dynamic						
Input Capacitance	C_{iss}			2600		pF
Output Capacitance	C_{oss}	$V_{GS} = 0 V$, $V_{DS} = 25 V$, $f = 1 MHz$		800		
Reversen Transfer Capacitance	C_{rss}			200		
Total Gate Charge[c]	Q_g			85	100	nC
Gate-Source Charge[c]	Q_{gs}	$V_{DS} = 30 V$, $V_{GS} = 10 V$, $I_D = 60 A$		15	20	
Gate-Drain Charge[c]	Q_{gd}			35	50	
Turn-On Delay Time[c]	$t_{d(on)}$			15	30	ns
Rise Time[c]	t_r	$V_{DD} = 30 V$, $R_L = 1 \Omega$		20	35	
Turn-Off Delay Time[c]	$t_{d(off)}$	$I_D \approx 30 A$, $V_{GEN} = 10 V$, $R_G = 2.5 \Omega$		50	65	
Fall Time[c]	t_f			20	30	
Source-Drain Diode Ratings and Characteristics ($T_C = 25°C$)						
Continuous Current	I_s				60	A
Pulsed Current	I_{SM}				240	
Forward Voltage[b]	V_{SD}	$I_F = 60 A$, $V_{GS} = 0 V$			2.0	V
Reverse Recovery Time	t_{rr}			160		ns
Peak Reverse Recovery Current	$I_{RM(REC)}$	$I_F = 60 A$, $dI_F/dt = 100 A/\mu s$		13		A
Reverse Recovery Charge	Q_{rr}			1.0		μC

Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width $\leq 300 \mu s$, duty cycle $\leq 2\%$.
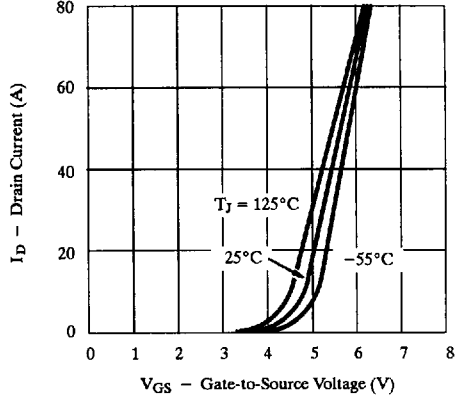c. Independent of operating temperature.
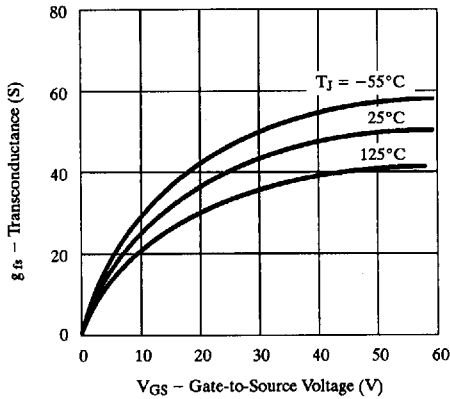
Typical Characteristics (25°C Unless Otherwise Noted)
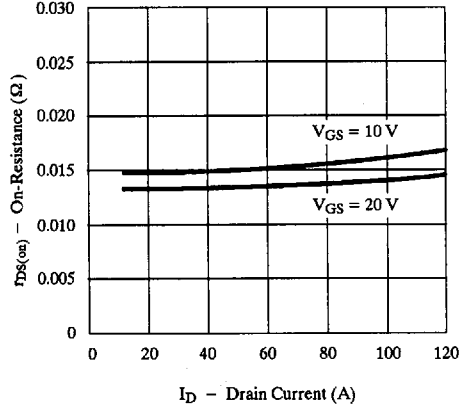

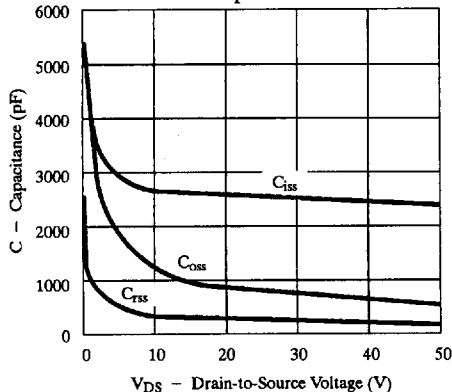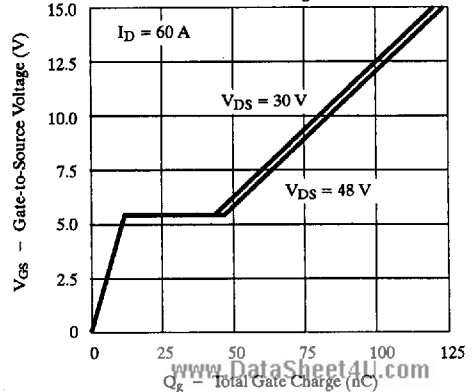Output Characteristics
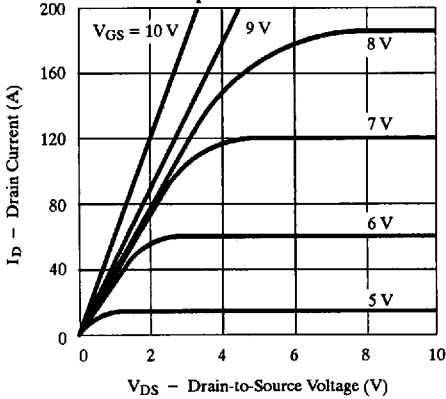
Transfer Characteristics

Transconductance
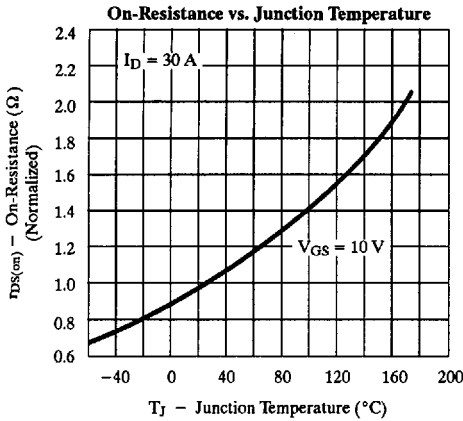

On-Resistance vs. Drain Current

Capacitance

Gate Charge

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Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

Source-Drain Diode Forward Voltage

Thermal Ratings

Maximum Avalanche and Drain Current vs. Case Temperature

Safe Operating Area

Normalized Thermal Transient Impedance, Junction-to-Case