

RoHS Compliant Product

Description

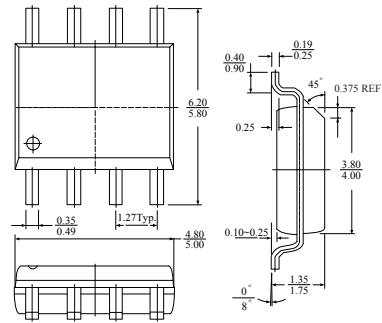
The SSG4503 provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOP-8 package is universally preferred for all commercial industrial surface mount application and suited for low voltage applications such as DC/DC converters.

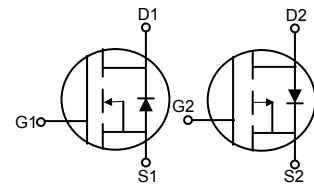
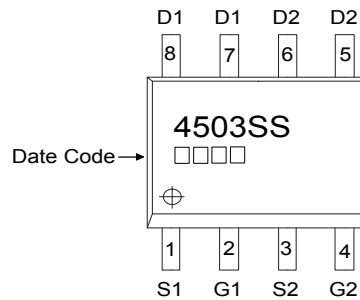
Features

- * Simple Drive Requirement
- * Lower On-Resistance
- * Fast Switching Performance

SOP-8



Dimensions in millimeters



Absolute Maximum Ratings

Parameter	Symbol	Ratings		Unit
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current ³	$I_D @ T_A = 25^\circ C$	6.9	-6.3	A
Continuous Drain Current ³	$I_D @ T_A = 70^\circ C$	5.5	-5	A
Pulsed Drain Current ¹	I_{DM}	30	-30	A
Total Power Dissipation	$P_D @ T_A = 25^\circ C$	2.0		W
Linear Derating Factor		0.016		W/ $^\circ C$
Operating Junction and Storage Temperature Range	T_j, T_{stg}	-55~+150		$^\circ C$

Thermal Data

Parameter	Symbol	Ratings	Unit
Thermal Resistance Junction-ambient ³	R_{thj-a}	62.5	$^\circ C/W$

Electrical Characteristics N Channel(Tj=25°C Unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	$V_{GS}=0V, I_D=250\mu A$
Breakdown Voltage Temp. Coefficient	$\Delta BV_{DS}/\Delta T_J$	-	0.005	-	V/°C	Reference to 25°C, $I_D=1mA$
Gate Threshold Voltage	$V_{GS(th)}$	1.0	-	3.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	$V_{GS}=\pm 20V$
Drain-Source Leakage Current (Tj=25°C)	I_{DSS}	-	-	1	uA	$V_{DS}=30V, V_{GS}=0$
Drain-Source Leakage Current (Tj=70°C)		-	-	25	uA	$V_{DS}=24V, V_{GS}=0$
Static Drain-Source On-Resistance ²	$R_{DS(ON)}$	-	-	28	m Ω	$V_{GS}=10V, I_D=6A$
		-	-	42		$V_{GS}=4.5V, I_D=4A$
Total Gate Charge ²	Q_g	-	9	15	nC	$I_D=6A$ $V_{DS}=24V$ $V_{GS}=4.5V$
Gate-Source Charge	Q_{gs}	-	2	-		
Gate-Drain ("Miller") Charge	Q_{gd}	-	6	-		
Turn-on Delay Time ²	$T_{d(ON)}$	-	8	-	nS	$V_{DD}=15V$ $I_D=1A$ $V_{GS}=10V$ $R_G=3.3\Omega$ $R_D=15\Omega$
Rise Time	T_r	-	7	-		
Turn-off Delay Time	$T_{d(OFF)}$	-	19	-		
Fall Time	T_f	-	6	-		
Input Capacitance	C_{iss}	-	610	970	pF	$V_{GS}=0V$ $V_{DS}=25V$ $f=1.0MHz$
Output Capacitance	C_{oss}	-	160	-		
Reverse Transfer Capacitance	C_{rss}	-	120	-		
Forward Transconductance	G_{fs}	-	5.7	-	S	$V_{DS}=10V, I_D=6A$

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Forward On Voltage ²	V_{SD}	-	-	1.2	V	$I_S=6A, V_{GS}=0V, T_J=25^\circ C$
Reverse Recovery Time	T_{rr}	-	18	-	nS	$I_S=6A, V_{GS}=0V$ $di/dt=100A/\mu s$
Reverse Recovery Charge	Q_{rr}	-	11	-	nC	

Notes: 1.Pulse width limited by Max. junction temperature.

2.Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

3.Surface mounted on 1 inch² copper pad of FR4 board; 135 °C/W when mounted on min. copper pad.

Electrical Characteristics P-Channel(T_j=25°C Unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain-Source Breakdown Voltage	BV _{DSS}	-30	-	-	V	V _{GS} =0V, I _D =-250uA
Breakdown Voltage Temp. Coefficient	ΔBV _{DSS} /ΔT _j	-	-0.004	-	V/°C	Reference to 25°C, I _D =-1mA
Gate Threshold Voltage	V _{GS(th)}	-1.0	-	-3.0	V	V _{DS} =V _{GS} , I _D =-250uA
Gate-Source Leakage Current	I _{GSS}	-	-	±100	nA	V _{GS} =± 20V
Drain-Source Leakage Current (T _j =25°C)	I _{DSS}	-	-	-1	uA	V _{DS} =-30V, V _{GS} =0
Drain-Source Leakage Current (T _j =70°C)		-	-	-25	uA	V _{DS} =-24V, V _{GS} =0
Static Drain-Source On-Resistance ²	R _{DS(ON)}	-	-	36	mΩ	V _{GS} =-10V, I _D =-6A
		-	-	55		V _{GS} =-4.5V, I _D =-4A
Total Gate Charge ²	Q _g	-	15	24	nC	I _D =-6A V _{DS} =-24V V _{GS} =-4.5V
Gate-Source Charge	Q _{gs}	-	3	-		
Gate-Drain ("Miller") Charge	Q _{gd}	-	9	-		
Turn-on Delay Time ²	T _{d(ON)}	-	12	-	nS	V _{DS} =-15V I _D =-1A V _{GS} =-10V R _G =3.3Ω R _D =15 Ω
Rise Time	T _r	-	8	-		
Turn-off Delay Time	T _{d(OFF)}	-	42	-		
Fall Time	T _f	-	34	-		
Input Capacitance	C _{iss}	-	960	1540	pF	V _{GS} =0V V _{DS} =-25V f=1.0MHz
Output Capacitance	C _{oss}	-	300	-		
Reverse Transfer Capacitance	C _{rss}	-	220	-		
Forward Transconductance	G _{fs}	-	5.8	-	S	V _{DS} =-10V, I _D =-6A

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Forward On Voltage ²	V _{SD}	-	-	-1.2	V	I _S =-6A, V _{GS} =0V, T _j =25°C
Reverse Recovery Time	T _{rr}	-	24	-	nS	I _S =-6A, V _{GS} =0V dI/dt=100A/us
Reverse Recovery Charge	Q _{rr}	-	18	-	nC	

Notes: 1.Pulse width limited by Max. junction temperature.

2.Pulse width ≤300us, dutycycle ≤2%.

3.Surface mounted on 1 inch² copper pad of FR4 board;135 °C/W when mounted on min. copper pad.

Characteristics Curve N-Channel

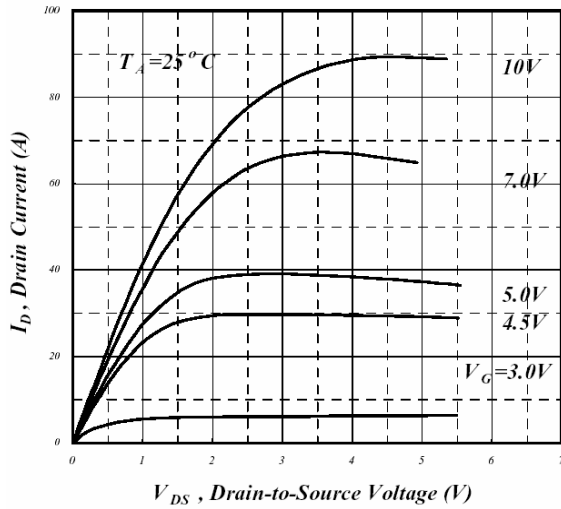


Fig 1. Typical Output Characteristics

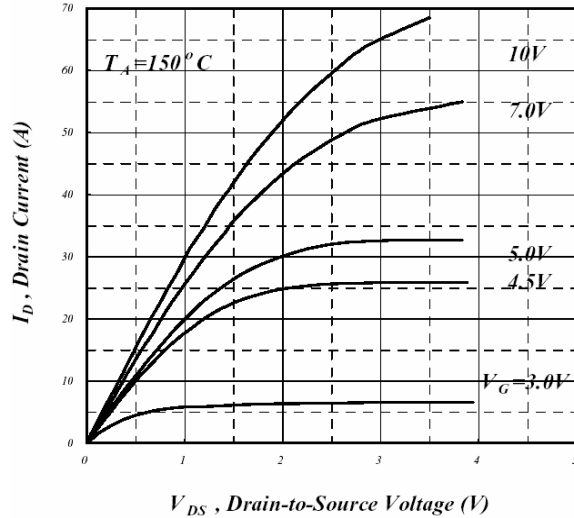


Fig 2. Typical Output Characteristics

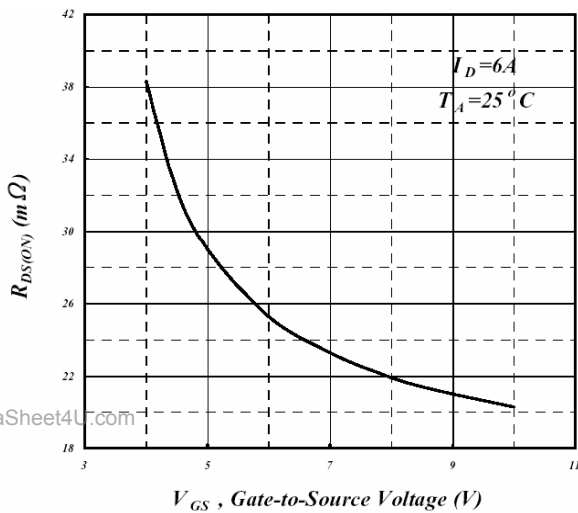


Fig 3. On-Resistance v.s. Gate Voltage

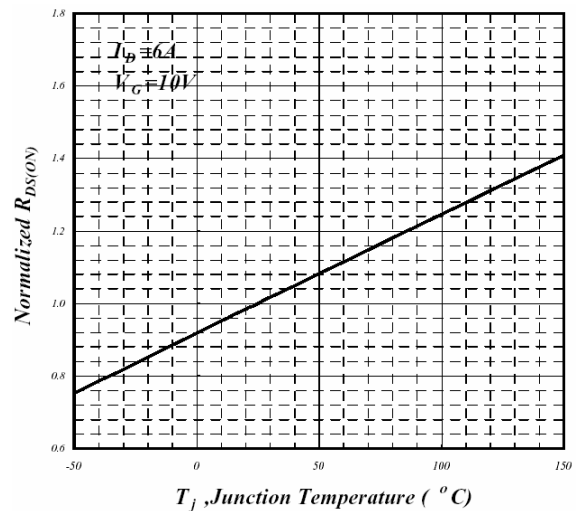


Fig 4. Normalized On-Resistance v.s. Junction Temperature

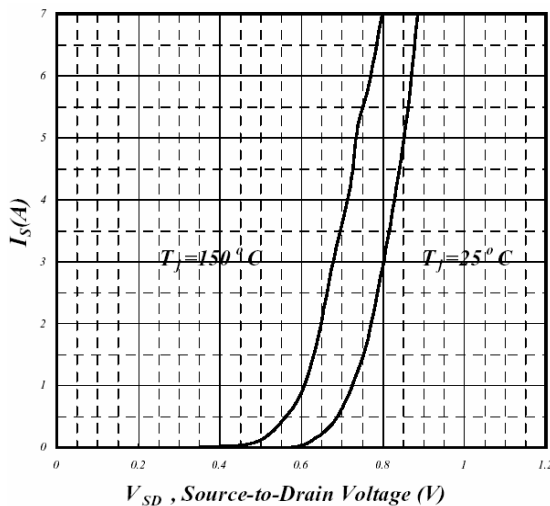


Fig 5. Forward Characteristics of Reverse Diode

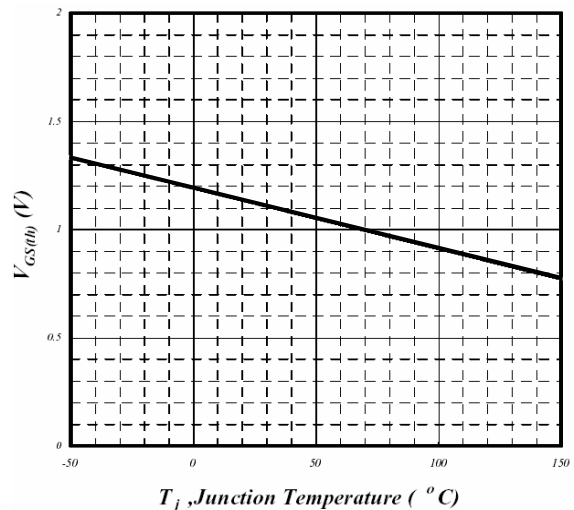


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

N-Channel

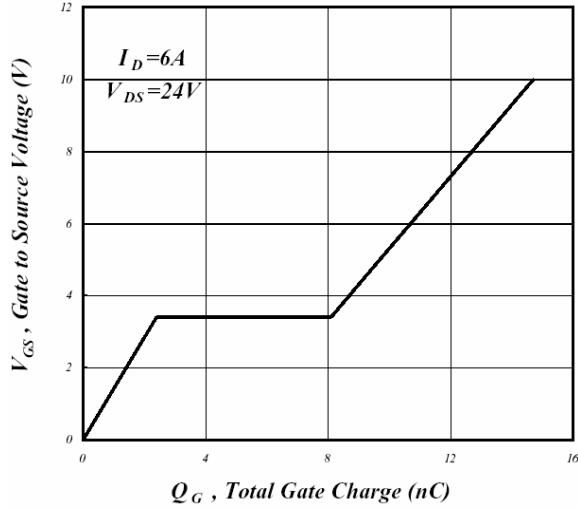


Fig 7. Gate Charge Characteristics

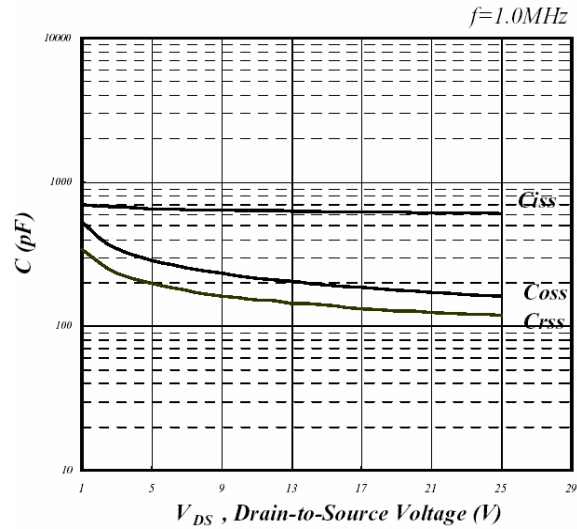


Fig 8. Typical Capacitance Characteristics

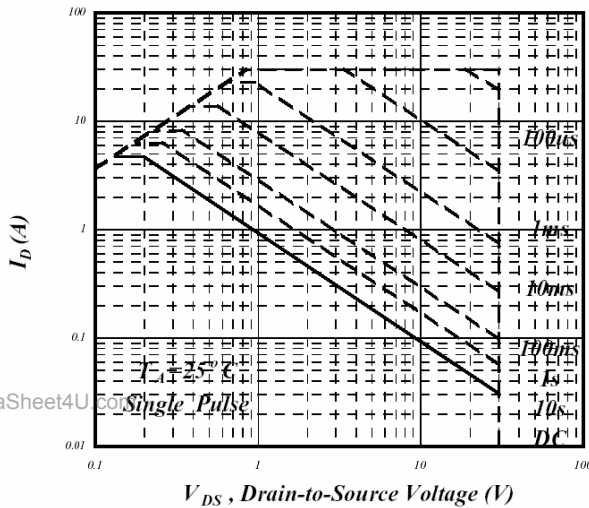


Fig 9. Maximum Safe Operating Area

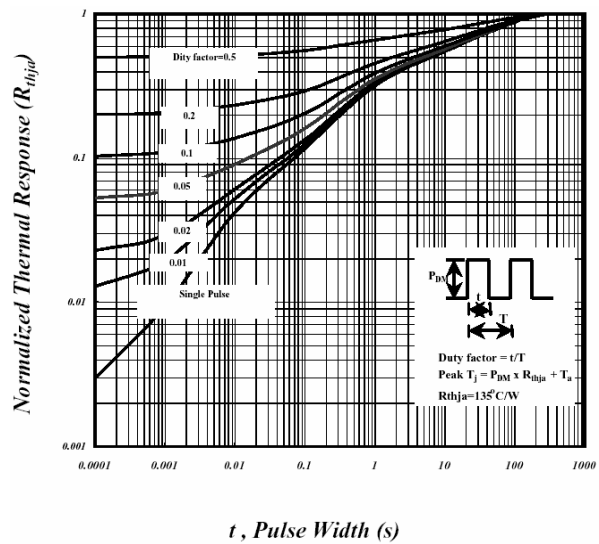


Fig 10. Effective Transient Thermal Impedance

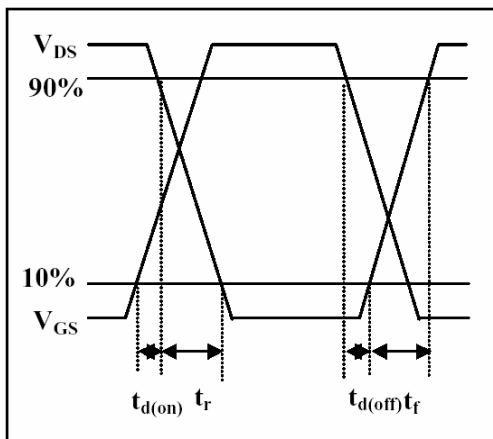


Fig 11. Switching Time Waveform

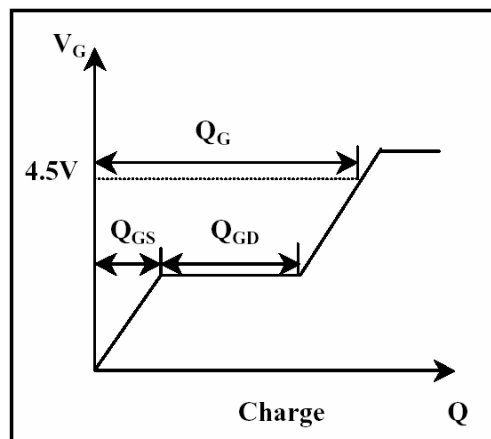


Fig 12. Gate Charge Waveform

P-Channel

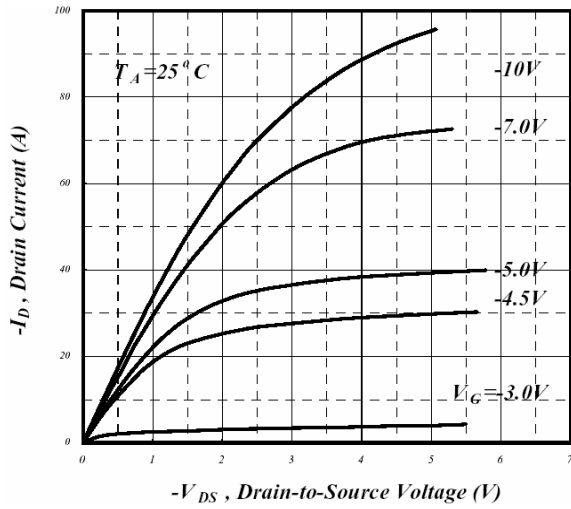


Fig 1. Typical Output Characteristics

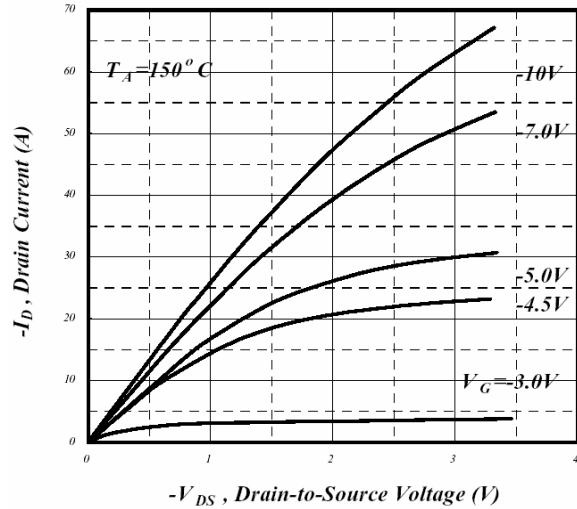


Fig 2. Typical Output Characteristics

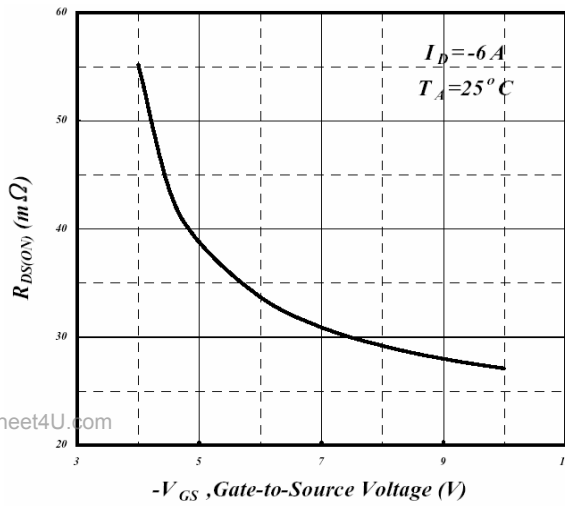


Fig 3. On-Resistance v.s. Gate Voltage

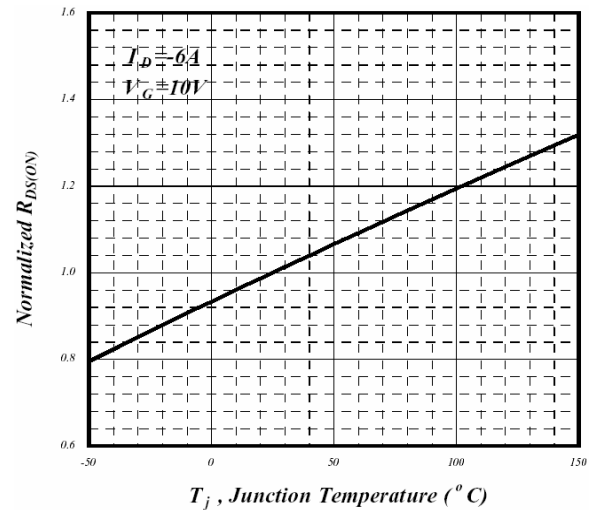


Fig 4. Normalized On-Resistance v.s. Junction Temperature

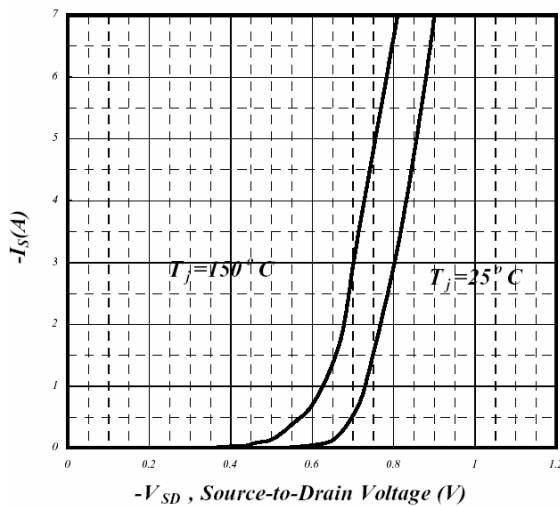


Fig 5. Forward Characteristics of Reverse Diode

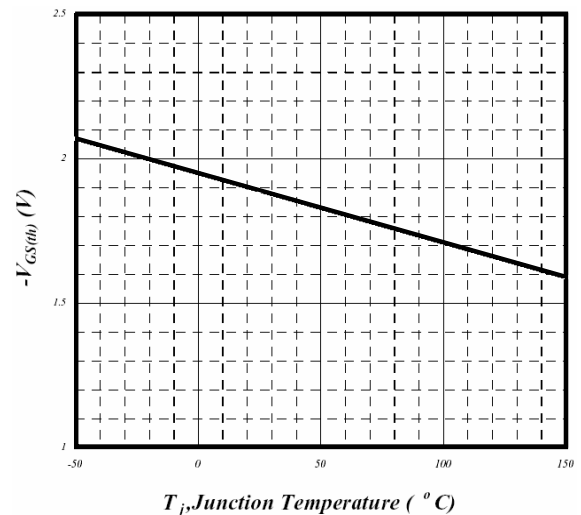


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

SSG4503

N Channel 6.9A, 30V, $R_{DS(ON)}$ 28m Ω
P Channel -6.3A, -30V, $R_{DS(ON)}$ 36m Ω

Enhancement Mode Power Mos.FET

P-Channel

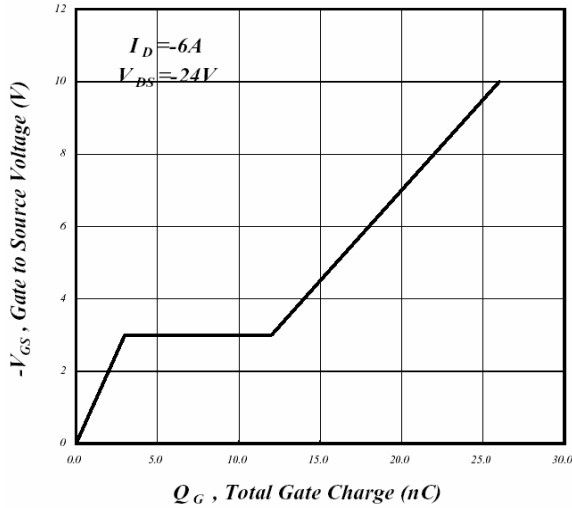


Fig 7. Gate Charge Characteristics

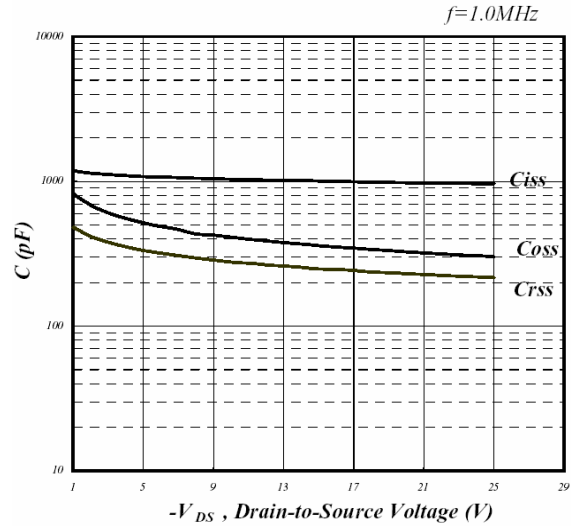


Fig 8. Typical Capacitance Characteristics

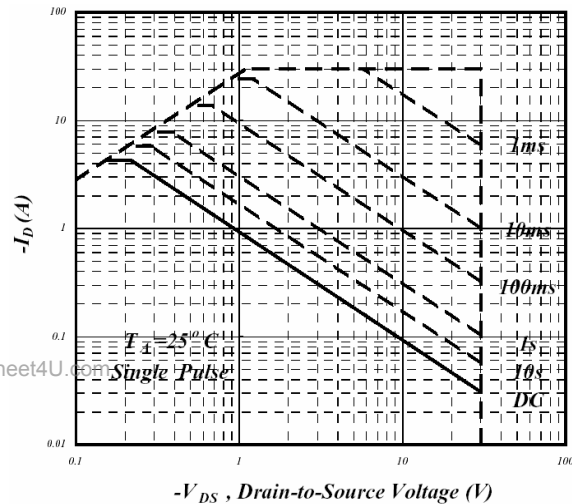


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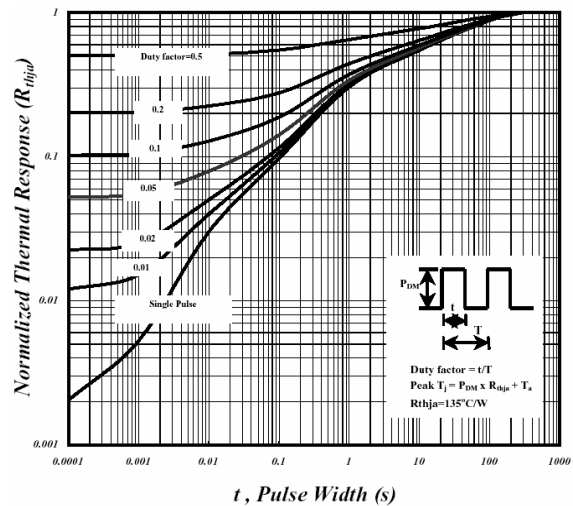


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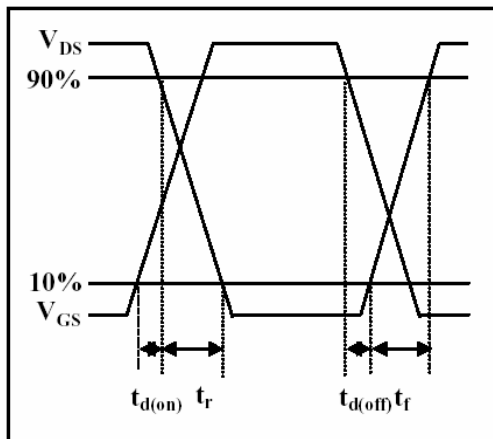


Fig 11. Switching Time Waveform

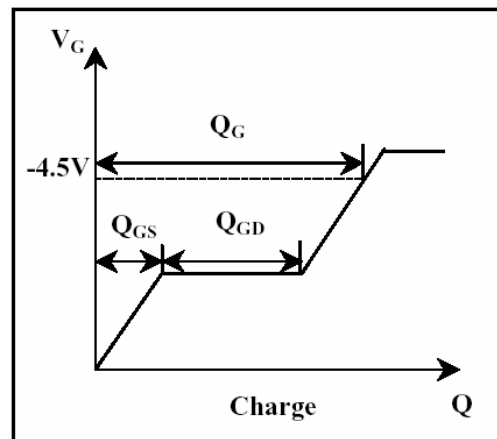


Fig 12. Gate Charge Waveform