DATA SHEET

TDA4856

I^{2}C-bus autosync deflection controller for PC monitors

Product specification
Supersedes data of 1998 Oct 02
File under Integrated Circuits, IC02

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FEATURES

Concept features

- Full horizontal plus vertical autosync capability
- Extended horizontal frequency range from 15 to 130 kHz
- Comprehensive set of I^{2}C-bus driven geometry adjustments and functions, including standby mode
- Very good vertical linearity
- Moire cancellation
- Start-up and switch-off sequence for safe operation of all power components
- X-ray protection
- Power dip recognition
- Flexible switched mode B+ supply function block for feedback and feed forward converter
- Internally stabilized voltage reference
- Drive signal for focus amplifiers with combined horizontal and vertical parabola waveforms
- DC controllable inputs for Extremely High Tension (EHT) compensation
- SDIP32 package.

Synchronization

- Can handle all sync signals (horizontal, vertical, composite and sync-on-video)
- Output for video clamping (leading/trailing edge selectable by the I^{2}C-bus), vertical blanking and protection blanking
- Output for fast unlock status of horizontal synchronization and blanking on grid 1 of picture tube.

Horizontal section

- I^{2}C-bus controllable wide range linear picture position, pin unbalance and parallelogram correction via horizontal phase
- Frequency-locked loop for smooth catching of horizontal frequency
- Simple frequency preset of f_{min} and f_{max} by external resistors
- Low jitter
- Soft start for horizontal and B+ control drive signals.

Vertical section

- I^{2}C-bus controllable vertical picture size, picture position, linearity (S-correction) and linearity balance
- Output for the I^{2}C-bus controllable vertical sawtooth and parabola (for pin unbalance and parallelogram)
- Vertical picture size independent of frequency
- Differential current outputs for DC coupling to vertical booster
- 50 to 160 Hz vertical autosync range.

East-West (EW) section

- I^{2}C-bus controllable output for horizontal pincushion, horizontal size, corner and trapezium correction
- Optional tracking of EW drive waveform with line frequency selectable by the I^{2}C-bus.

Focus section

- I^{2}C-bus controllable output for horizontal and vertical parabolas
- Vertical parabola is independent of frequency and tracks with vertical adjustments
- Horizontal parabola independent of frequency
- Adjustable pre-correction of delay in focus output stage.

GENERAL DESCRIPTION

The TDA4856 is a high performance and efficient solution for autosync monitors. All functions are controllable by the I^{2}C-bus.

The TDA4856 provides synchronization processing, horizontal and vertical synchronization with full autosync capability and very short settling times after mode changes. External power components are given a great deal of protection. The IC generates the drive waveforms for DC-coupled vertical boosters such as the TDA486x and TDA835x.

The TDA4856 provides extended functions e.g. as a flexible B+ control, an extensive set of geometry control facilities, and a combined output for horizontal and vertical focus signals.

Together with the I^{2}C-bus driven Philips TDA488x video processor family, a very advanced system solution is offered.

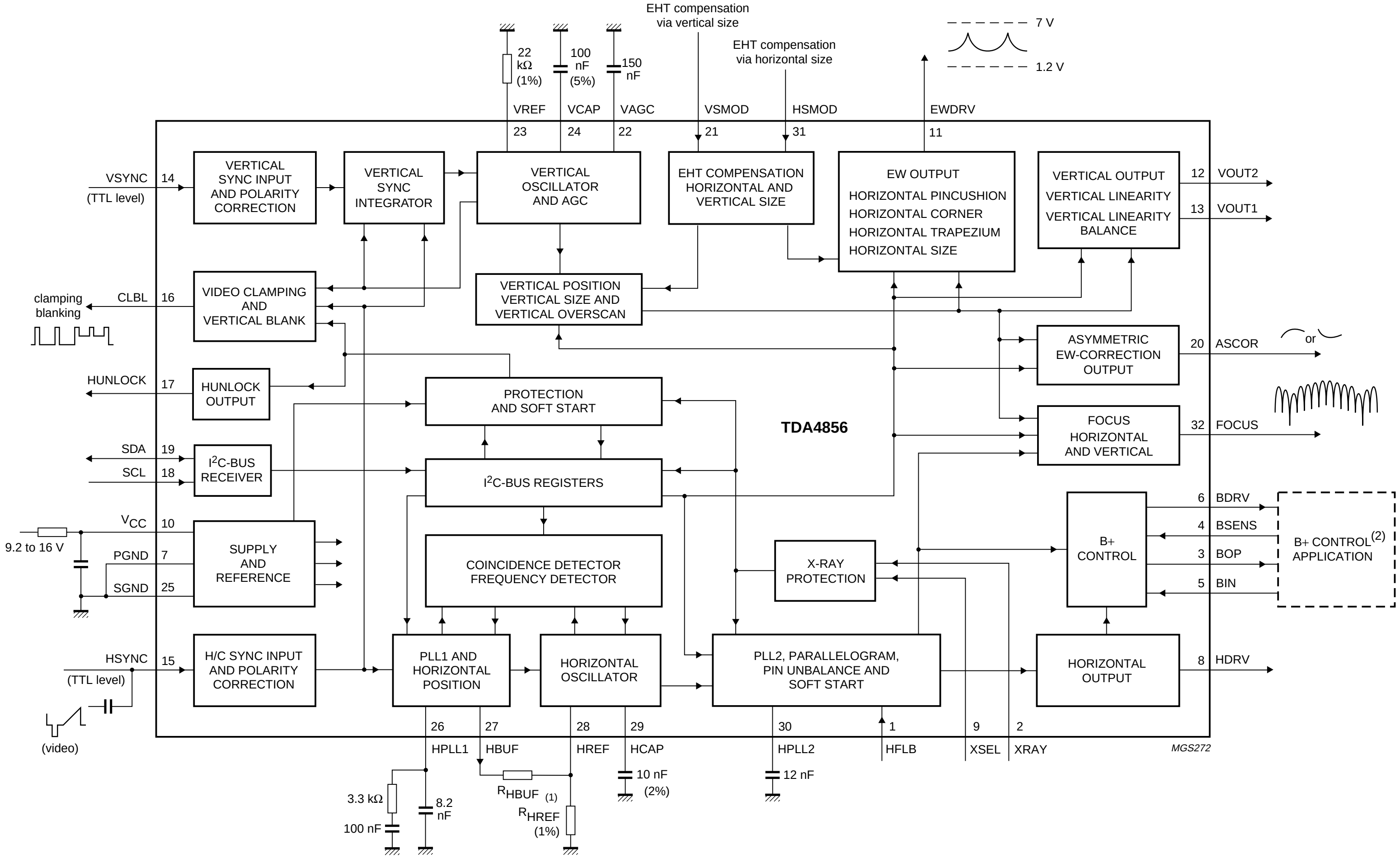
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	9.2	–	16	V
I_{CC}	supply current	–	70	–	mA
$I_{CC(stb)}$	supply current during standby mode	–	9	–	mA
VSIZE	vertical size	60	–	100	%
VGA	VGA overscan for vertical size	–	16.8	–	%
VPOS	vertical position	–	±11.5	–	%
VLIN	vertical linearity (S-correction)	–2	–	–46	%
VLINBAL	vertical linearity balance	–	±1.25	–	%
V_{HSIZE}	horizontal size	0.13	–	3.6	V
V_{HPIN}	horizontal pincushion (EW parabola)	0.04	–	1.42	V
V_{HEHT}	horizontal size modulation	0.02	–	0.69	V
V_{HTRAP}	horizontal trapezium correction	–	±0.5	–	V
V_{HCORT}	horizontal corner correction at top of picture	–0.64	–	+0.2	V
V_{HCORB}	horizontal corner correction at bottom of picture	–0.64	–	+0.2	V
HPOS	horizontal position	–	±13	–	%
HPARAL	horizontal parallelogram	–	±1.5	–	%
HPINBAL	EW pin unbalance	–	±1.5	–	%
T_{amb}	operating ambient temperature	–20	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4856	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1

BLOCK DIAGRAM



(1) For the calculation of f_H range see Section “Calculation of line frequency range”.

(2) See Figs 22 and 23.

Fig.1 Block diagram and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
HFLB	1	horizontal flyback input
XRAY	2	X-ray protection input
BOP	3	B+ control OTA output
BSENS	4	B+ control comparator input
BIN	5	B+ control OTA input
BDRV	6	B+ control driver output
PGND	7	power ground
HDRV	8	horizontal driver output
XSEL	9	select input for X-ray reset
V_{CC}	10	supply voltage
EWDRV	11	EW waveform output
VOUT2	12	vertical output 2 (ascending sawtooth)
VOUT1	13	vertical output 1 (descending sawtooth)
VSYNC	14	vertical synchronization input
HSYNC	15	horizontal/composite synchronization input
CLBL	16	video clamping pulse/vertical blanking output
HUNLOCK	17	horizontal synchronization unlock/protection/vertical blanking output
SCL	18	I^2C-bus clock input
SDA	19	I^2C-bus data input/output
ASCOR	20	output for asymmetric EW corrections
VSMOD	21	input for EHT compensation (via vertical size)
VAGC	22	external capacitor for vertical amplitude control
VREF	23	external resistor for vertical oscillator
VCAP	24	external capacitor for vertical oscillator
SGND	25	signal ground
HPLL1	26	external filter for PLL1
HBUF	27	buffered f/v voltage output
HREF	28	reference current for horizontal oscillator
HCAP	29	external capacitor for horizontal oscillator
HPLL2	30	external filter for PLL2/soft start
HSMOD	31	input for EHT compensation (via horizontal size)
FOCUS	32	output for horizontal and vertical focus

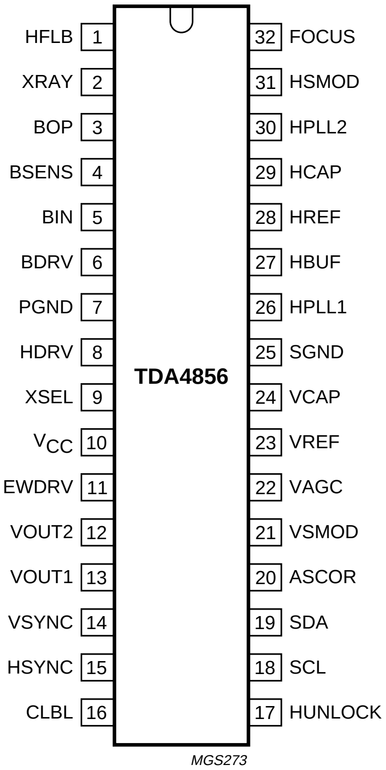


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Horizontal sync separator and polarity correction

HSYNC (pin 15) is the input for horizontal synchronization signals, which can be DC-coupled TTL signals (horizontal or composite sync) and AC-coupled negative-going video sync signals. Video syncs are clamped to 1.28 V and sliced at 1.4 V. This results in a fixed absolute slicing level of 120 mV related to top sync.

For DC-coupled TTL signals the input clamping current is limited. The slicing level for TTL signals is 1.4 V.

The separated sync signal (either video or TTL) is integrated on an internal capacitor to detect and normalize the sync polarity.

Normalized horizontal sync pulses are used as input signals for the vertical sync integrator, the PLL1 phase detector and the frequency-locked loop.

Vertical sync integrator

Normalized composite sync signals from HSYNC are integrated on an internal capacitor in order to extract vertical sync pulses. The integration time is dependent on the horizontal oscillator reference current at HREF (pin 28). The integrator output directly triggers the vertical oscillator.

Vertical sync slicer and polarity correction

Vertical sync signals (TTL) applied to VSYNC (pin 14) are sliced at 1.4 V. The output signal of the sync slicer is integrated on an internal capacitor to detect and normalize the sync polarity. The output signals of vertical sync integrator and sync normalizer are disjuncted before they are fed to the vertical oscillator.

Video clamping/vertical blanking generator

The video clamping/vertical blanking signal at CLBL (pin 16) is a two-level sandcastle pulse which is especially suitable for video ICs such as the TDA488x family, but also for direct applications in video output stages.

The upper level is the video clamping pulse, which is triggered by the horizontal sync pulse. Either the leading or trailing edge can be selected by setting control bit CLAMP via the I²C-bus. The width of the video clamping pulse is determined by an internal single-shot multivibrator.

The lower level of the sandcastle pulse is the vertical blanking pulse, which is derived directly from the internal oscillator waveform. It is started by the vertical sync and stopped with the start of the vertical scan. This results in optimum vertical blanking. Two different vertical blanking times are accessible, by control bit VBLK, via the I²C-bus.

Blanking will be activated continuously if one of the following conditions is true:

- Soft start of horizontal and B+ drive [voltage at HPLL2 (pin 30) pulled down externally or by the I²C-bus]
- PLL1 is unlocked while frequency-locked loop is in search mode
- No horizontal flyback pulses at HFLB (pin 1)
- X-ray protection is activated
- Supply voltage at V_{CC} (pin 10) is low (see Fig.24).

Horizontal unlock blanking can be switched off, by control bit BLKDIS, via the I²C-bus while vertical blanking is maintained.

Frequency-locked loop

The frequency-locked loop can lock the horizontal oscillator over a wide frequency range. This is achieved by a combined search and PLL operation. The frequency range is preset by two external resistors and the recommended maximum ratio is $\frac{f_{max}}{f_{min}} = \frac{6.5}{1}$

This can, for instance, be a range from 15.625 to 90 kHz with all tolerances included.

Without a horizontal sync signal the oscillator will be free-running at f_{min}. Any change of sync conditions is detected by the internal coincidence detector. A deviation of more than 4% between horizontal sync and oscillator frequency switches the horizontal section into search mode. This means that PLL1 control currents are switched off immediately. The internal frequency detector then starts tuning the oscillator. Very small DC currents at HPLL1 (pin 26) are used to perform this tuning with a well defined change rate. When coincidence between horizontal sync and oscillator frequency is detected, the search mode is first replaced by a soft-lock mode which lasts for the first part of the next vertical period.
The soft-lock mode is then replaced by a normal PLL operation. This operation ensures smooth tuning and avoids fast changes of horizontal frequency during catching.

In this concept it is not allowed to load HPLL1.
The frequency dependent voltage at this pin is fed internally to HBUF (pin 27) via a sample-and-hold and buffer stage. The sample-and-hold stage removes all disturbances caused by horizontal sync or composite vertical sync from the buffered voltage. An external resistor connected between pins HBUF and HREF defines the frequency range.

Out-of-lock indication (pin HUNLOCK)

Pin HUNLOCK is floating during search mode, or if a protection condition is true. All this can be detected by the microcontroller if a pull-up resistor is connected to its own supply voltage.

For an additional fast vertical blanking at grid 1 of the picture tube a 1 V signal referenced to ground is available at this output. The continuous protection blanking (see Section “Video clamping/vertical blanking generator”) is also available at this pin. Horizontal unlock blanking can be switched off, by control bit BLKDIS via the I^2C-bus while vertical blanking is maintained.

Horizontal oscillator

The horizontal oscillator is of the relaxation type and requires a capacitor of 10 nF at HCAP (pin 29).
For optimum jitter performance the value of 10 nF must not be changed.

The minimum oscillator frequency is determined by a resistor from HREF to ground. A resistor connected between pins HREF and HBUF defines the frequency range.

The reference current at pin HREF also defines the integration time constant of the vertical sync integration.

Calculation of line frequency range

The oscillator frequencies f_{min} and f_{max} must first be calculated. This is achieved by adding the spread of the relevant components to the highest and lowest sync frequencies $f_{sync(min)}$ and $f_{sync(max)}$. The oscillator is driven by the currents in R_{HREF} and R_{HBUF}.

The following example is a 31.45 to 90 kHz application:

Table 1 Calculation of total spread

spread of	for f_{max}	for f_{min}
IC	±3%	±5%
C_{HCAP}	±2%	±2%
R_{HREF}, R_{HBUF}	±2%	±2%
Total	±7%	±9%

Thus the typical frequency range of the oscillator in this example is:

$$f_{max} = f_{sync(max)} \times 1.07 = 96.3\ \text{kHz}$$

$$f_{min} = \frac{f_{sync(min)}}{1.09} = 28.4\ \text{kHz}$$

The resistors R_{HREF} and $R_{HBUFpar}$ can be calculated using the following formulae:

$$R_{HREF} = \frac{78 \times \text{kHz} \times \text{k}\Omega}{f_{min} + 0.0012 \times f_{min}^2[\text{kHz}]} = 2.61\ \text{k}\Omega$$

$$R_{HBUFpar} = \frac{78 \times \text{kHz} \times \text{k}\Omega}{f_{max} + 0.0012 \times f_{max}^2[\text{kHz}]} = 726\ \Omega\ .$$

The resistor $R_{HBUFpar}$ is calculated as the value of R_{HREF} and R_{HBUF} in parallel.

The formulae for R_{HBUF} also takes into account the voltage swing across this resistor:

$$R_{HBUF} = \frac{R_{HREF} \times R_{HBUFpar}}{R_{HREF} - R_{HBUFpar}} \times 0.8 = 805\ \Omega$$

PLL1 phase detector

The phase detector is a standard type using switched current sources, which are independent of horizontal frequency. It compares the middle of horizontal sync with a fixed point on the oscillator sawtooth voltage. The PLL1 loop filter is connected to HPLL1 (pin 26).

See also Section “Horizontal position adjustment and corrections”.

Horizontal position adjustment and corrections

A linear adjustment of the relative phase between the horizontal sync and the oscillator sawtooth (in PLL1 loop) is achieved via register HPOS. Once adjusted, the relative phase remains constant over the whole frequency range.

Correction of pin unbalance and parallelogram is achieved by modulating the phase between oscillator sawtooth and horizontal flyback (in loop PLL2) via registers HPARAL and HPINBAL. If those asymmetric EW corrections are performed in the deflection stage, both registers can be disconnected from the horizontal phase via control bit ACD. This does not change the output at pin ASCOR.

Horizontal moire cancellation

To achieve a cancellation of horizontal moire (also known as ‘video moire’), the horizontal frequency is divided-by-two to achieve a modulation of the horizontal phase via PLL2. The amplitude is controlled by register HMOIRE. To avoid a visible structure on screen the polarity changes with half of the vertical frequency. Control bit MOD disables the moire cancellation function.

PLL2 phase detector

The PLL2 phase detector is similar to the PLL1 detector and compares the line flyback pulse at HFLB (pin 1) with the oscillator sawtooth voltage. The control currents are independent of the horizontal frequency. The PLL2 detector thus compensates for the delay in the external horizontal deflection circuit by adjusting the phase of the HDRV (pin 8) output pulse.

An external modulation of the PLL2 phase is not allowed, because this would disturb the pre-correction of the horizontal focus parabola.

Soft start and standby

If HPLL2 is pulled to ground, either by an external DC current or by resetting register SOFTST, the horizontal output pulses and B+ control driver pulses will be inhibited. This means that HDRV (pin 8) and BDRV (pin 6) are floating in this state. In both cases PLL2 and the frequency-locked loop are disabled, and CLBL (pin 16) provides a continuous blanking signal and HUNLOCK (pin 17) is floating.

This option can be used for soft start, protection and power-down modes. When pin HPLL2 is released again, an automatic soft start sequence on the horizontal drive as well as on the B-drive output will be performed (see Fig.24).

A soft start can only be performed if the supply voltage for the IC is a minimum of 8.6 V.

The soft start timing is determined by the filter capacitor at HPLL2 (pin 30), which is charged with a constant current during soft start. In the beginning the horizontal driver stage generates very small output pulses. The width of these pulses increases with the voltage at HPLL2 until the final duty cycle is reached. The voltage at HPLL2 increases further and performs a soft start at BDRV (pin 6) as well. After BDRV has reached full duty cycle, the voltage at HPLL2 continues to rise until HPLL2 enters its normal operating range. The internal charge current is now disabled. Finally PLL2 and the frequency-locked loop are activated. If both functions reach normal operation, HUNLOCK (pin 17) switches from the floating status to normal vertical blanking, and continuous blanking at CLBL (pin 16) is removed.

Output stage for line drive pulses [HDRV (pin 8)]

An open-collector output stage allows direct drive of an inverting driver transistor because of a low saturation voltage of 0.3 V at 20 mA. To protect the line deflection transistor, the output stage is disabled (floating) for a low supply voltage at V_{CC} (see Fig.23).

The duty cycle of line drive pulses is slightly dependent on the actual horizontal frequency. This ensures optimum drive conditions over the whole frequency range.

X-ray protection

The X-ray protection input XRAY (pin 2) provides a voltage detector with a precise threshold. If the input voltage at XRAY exceeds this threshold for a certain time, then control bit SOFTST is reset, which switches the IC into protection mode. In this mode several pins are forced into defined states:

HUNLOCK (pin 17) is floating

The capacitor connected to HPLL2 (pin 30) is discharged

Horizontal output stage (HDRV) is floating

B+ control driver stage (BDRV) is floating

CLBL provides a continuous blanking signal.

There are two different methods of restarting ways the IC:

1. XSEL (pin 9) is open-circuit or connected to ground. The control bit SOFTST must be set to logic 1 via the I^2C-bus. Then the IC returns to normal operation via soft start.
2. XSEL (pin 9) is connected to V_{CC} via an external resistor. The supply voltage of the IC must be switched off for a certain period of time, before the IC can be restarted again using the standard power-on procedure.

Vertical oscillator and amplitude control

This stage is designed for fast stabilization of vertical size after changes in sync frequency conditions.
The free-running frequency $f_{fr(V)}$ is determined by the resistor R_{VREF} connected to pin 23 and the capacitor C_{VCAP} connected to pin 24. The value of R_{VREF} is not only optimized for noise and linearity performance in the whole vertical and EW section, but also influences several internal references. Therefore the value of R_{VREF} must not be changed. Capacitor C_{VCAP} should be used to select the free-running frequency of the vertical oscillator in accordance with the following formula:

$$f_{fr(V)} = \frac{1}{10.8 \times R_{VREF} \times C_{VCAP}}$$

To achieve a stabilized amplitude the free-running frequency $f_{fr(V)}$, without adjustment, should be at least 10% lower than the minimum trigger frequency.
The contributions shown in Table 2 can be assumed.

Table 2 Calculation of $f_{fr(V)}$ total spread

Contributing elements	
Minimum frequency offset between $f_{fr(V)}$ and lowest trigger frequency	10%
Spread of IC	±3%
Spread of R_{VREF}	±1%
Spread of C_{VCAP}	±5%
Total	19%

Result for 50 to 160 Hz application:

$$f_{fr(V)} = \frac{50\ Hz}{1.19} = 42\ Hz$$

The AGC of the vertical oscillator can be disabled by setting control bit AGCDIS via the I^2C-bus. A precise external current has to be injected into VCAP (pin 24) to obtain the correct vertical size. This special application mode can be used when the vertical sync pulses are serrated (shifted); this condition is found in some display modes, e.g. when using a 100 Hz up converter for video signals.

Application hint: VAGC (pin 22) has a high input impedance during scan. Therefore, the pin must not be loaded externally otherwise non-linearities in the vertical output currents may occur due to the changing charge current during scan.

Adjustment of vertical size, VGA overscan and EHT compensation

There are four different ways to adjust the amplitude of the differential output currents at VOUT1 and VOUT2.

1. Register VGAIN changes the vertical size without affecting any other output signal of the IC. This adjustment is meant for factory alignments.
2. Register VSIZE changes not only the vertical size, but also provides the correct tracking of all other related waveforms (see Section “Tracking of vertical adjustments”). This register should be used for user adjustments.
3. For the VGA350 mode register VOVSCN can activate a +17% step in vertical size.
4. VSMOD (pin 21) can be used for a DC controlled EHT compensation of vertical size by correcting the differential output currents at VOUT1 and VOUT2. The EW waveforms, vertical focus, pin unbalance and parallelogram corrections are not affected by VSMOD.

Adjustment of vertical position, vertical linearity and vertical linearity balance

Register VOFFS provides a DC shift at the sawtooth outputs VOUT1 and VOUT2 (pins 13 and 12) without affecting any other output waveform. This adjustment is meant for factory alignments.

Register VPOS provides a DC shift at the sawtooth output VOUT1 and VOUT2 with correct tracking of all other related waveforms (see Section “Tracking of vertical adjustments”). This register should be used for user adjustments. Due to the tracking the whole picture moves vertically while maintaining the correct geometry.

Register VLIN is used to adjust the amount of the vertical S-correction in the output signal. This function can be switched off by control bit VSC.

Register VLINBAL is used to correct the unbalance of vertical S-correction in the output signal.

Tracking of vertical adjustments

The adjustments via registers VSIZE, VOVSCN and VPOS also affect the waveforms of horizontal pincushion, vertical linearity (S-correction), vertical linearity balance, focus parabola, pin unbalance and parallelogram correction. The result of this interaction is that no readjustment of these parameters is necessary after an user adjustment of vertical picture size and vertical picture position.

Adjustment of vertical moire cancellation

To achieve a cancellation of vertical moire (also known as ‘scan moire’) the vertical picture position can be modulated by half the vertical frequency. The amplitude of the modulation is controlled by register VMOIRE and can be switched off via control bit MOD.

Horizontal pincushion (including horizontal size, corner correction and trapezium correction)

EWDRV (pin 11) provides a complete EW drive waveform. The components horizontal pincushion, horizontal size, corner correction and trapezium correction are controlled by the registers HPIN, HSIZE, HCORT, HCORB and HTRAP.

The corner correction can be adjusted separately for the top (HCORT) and bottom (HCORB) part of the picture.

The pincushion (EW parabola) amplitude, corner and trapezium correction track with the vertical picture size (VSIZE) and also with the adjustment for vertical picture position (VPOS). The corner correction does not track with the horizontal pincushion (HPIN).

Further the horizontal pincushion amplitude, corner and trapezium correction track with the horizontal picture size, which is adjusted via register HSIZE and the analog modulation input HSMOD. If the DC component in the EWDRV output signal is increased via HSIZE or I_{HSMOD}, the pincushion, corner and trapezium component of the EWDRV output will be reduced by a factor of

$$1 - \frac{V_{HSIZE} + V_{HEHT}\left(1 - \frac{V_{HSIZE}}{14.4\ V}\right)}{14.4\ V}$$

The value 14.4 V is a virtual voltage for calculation only. The output pin can not reach this value, but the gain (and DC bias) of the external application should be such that the horizontal deflection is reduced to zero when EWDRV reaches 14.4 V.

HSMOD (pin 31) can be used for a DC controlled EHT compensation by correcting horizontal size, horizontal pincushion, corner and trapezium. The control range at this pin tracks with the actual value of HSIZE. For an increasing DC component V_{HSIZE} in the EWDRV output signal, the DC component V_{HEHT} caused by I_{HSMOD} will be reduced by a factor of $1 - \frac{V_{HSIZE}}{14.4\ V}$ as shown in the equation above.

The whole EWDRV voltage is calculated as follows: $V_{EWDRV} = 1.2\ V + [V_{HSIZE} + V_{HEHT} \times f(HSIZE) + (V_{HPIN} + V_{HCOR} + V_{HTRAP}) \times g(HSIZE, HSMOD)] \times h(I_{HREF})$

Where:

$$V_{HEHT} = \frac{I_{HSMOD}}{120\ \mu A} \times 0.69$$

$$f(HSIZE) = 1 - \frac{V_{HSIZE}}{14.4\ V}$$

$$g(HSIZE, HSMOD) = 1 - \frac{V_{HSIZE} + V_{HEHT}\left(1 - \frac{V_{HSIZE}}{14.4\ V}\right)}{14.4\ V}$$

$$h(I_{HREF}) = \frac{I_{HREF}}{I_{HREF}\,|_{f = 70kHz}}$$

Two different modes of operation can be chosen for the EW output waveform via control bit FHMULT:

1. Mode 1

   Horizontal size is controlled via register HSIZE and causes a DC shift at the EWDRV output. The complete waveform is also multiplied internally by a signal proportional to the line frequency [which is detected via the current at HREF (pin 28)]. This mode is to be used for driving EW diode modulator stages which require a voltage proportional to the line frequency.

2. Mode 2

   The EW drive waveform does not track with the line frequency. This mode is to be used for driving EW modulators which require a voltage independent of the line frequency.

Output stage for asymmetric correction waveforms [ASCOR (pin 20)]

This output is designed as a voltage output for superimposed waveforms of vertical parabola and sawtooth. The amplitude and polarity of both signals can be changed by registers HPARAL and HPINBAL via the I²C-bus.

Application hint: The TDA4856 offers two possibilities to control registers HPINBAL and HPARAL.

1. Control bit ACD = 1

   The two registers now control the horizontal phase by means of internal modulation of the PLL2 horizontal phase control. The ASCOR output (pin 20) can be left unused, but it will always provide an output signal because the ASCOR output stage is not influenced by the control bit ACD.

2. Control bit ACD = 0

   The internal modulation via PLL2 is disconnected. In order to obtain the required effect on the screen, pin ASCOR must now be fed to the DC amplifier which controls the DC shift of the horizontal deflection. This option is useful for applications which already use a DC shift transformer.

If the tube does not need HPINBAL and HPARAL, then pin ASCOR can be used for other purposes, i.e. for a simple dynamic convergence.

Dynamic focus section [FOCUS (pin 32)]

This section generates a complete drive signal for dynamic focus applications. The amplitude of the horizontal parabola is internally stabilized, thus it is independent of the horizontal frequency. The amplitude can be adjusted via register HFOCUS. Changing horizontal size may require a correction of HFOCUS. To compensate for the delay in external focus amplifiers a ‘pre-correction’ for the phase of the horizontal parabola has been implemented (see Fig.28). The amount of this pre-correction can be adjusted via register HFOCAD. The amplitude of the vertical parabola is independent of frequency and tracks with all vertical adjustments. The amplitude can be adjusted via register VFOCUS.

FOCUS (pin 32) is designed as a voltage output for the superimposed vertical and horizontal parabolas.

B+ control function block

The B+ control function block of the TDA4856 consists of an Operational Transconductance Amplifier (OTA), a voltage comparator, a flip-flop and a discharge circuit. This configuration allows easy applications for different B+ control concepts. See also Application Note AN96052: *“B+ converter Topologies for Horizontal Deflection and EHT with TDA4855/58”*.

GENERAL DESCRIPTION

The non-inverting input of the OTA is connected internally to a high precision reference voltage. The inverting input is connected to BIN (pin 5). An internal clamping circuit limits the maximum positive output voltage of the OTA.
The output itself is connected to BOP (pin 3) and to the inverting input of the voltage comparator.
The non-inverting input of the voltage comparator can be accessed via BSENS (pin 4).

B+ drive pulses are generated by an internal flip-flop and fed to BDRV (pin 6) via an open-collector output stage. This flip-flop is set at the rising edge of the signal at HDRV (pin 8). The falling edge of the output signal at BDRV has a defined delay of $t_{d(BDRV)}$ to the rising edge of the HDRV pulse. When the voltage at BSENS exceeds the voltage at BOP, the voltage comparator output resets the flip-flop and, therefore, the open-collector stage at BDRV is floating again.

An internal discharge circuit allows a well defined discharge of capacitors at BSENS. BDRV is active at a LOW-level output voltage (see Figs 22 and 23), thus it requires an external inverting driver stage.

The B+ function block can be used for B+ deflection modulators in many different ways. Two popular application combinations are as follows:

- Boost converter in feedback mode (see Fig.22)

  In this application the OTA is used as an error amplifier with a limited output voltage range. The flip-flop is set on the rising edge of the signal at HDRV. A reset will be generated when the voltage at BSENS, taken from the current sense resistor, exceeds the voltage at BOP.

  If no reset is generated within a line period, the rising edge of the next HDRV pulse forces the flip-flop to reset. The flip-flop is set immediately after the voltage at BSENS has dropped below the threshold voltage $V_{RESTART(BSENS)}$.

- Buck converter in feed forward mode (see Fig.23)

  This application uses an external RC combination at BSENS to provide a pulse width which is independent from the horizontal frequency. The capacitor is charged via an external resistor and discharged by the internal discharge circuit. For normal operation the discharge circuit is activated when the flip-flop is reset by the internal voltage comparator. The capacitor will now be discharged with a constant current until the internally controlled stop level $V_{STOP(BSENS)}$ is reached. This level will be maintained until the rising edge of the next HDRV pulse sets the flip-flop again and disables the discharge circuit.

  If no reset is generated within a line period, the rising edge of the next HDRV pulse automatically starts the discharge sequence and resets the flip-flop. When the voltage at BSENS reaches the threshold voltage $V_{RESTART(BSENS)}$, the discharge circuit will be disabled automatically and the flip-flop will be set immediately. This behaviour allows a definition of the maximum duty cycle of the B+ control drive pulse by the relationship of charge current to discharge current.

Supply voltage stabilizer, references, start-up procedures and protection functions

The TDA4856 provides an internal supply voltage stabilizer for excellent stabilization of all internal references. An internal gap reference, especially designed for low-noise, is the reference for the internal horizontal and vertical supply voltages. All internal reference currents and drive current for the vertical output stage are derived from this voltage via external resistors.

If either the supply voltage is below 8.3 V or no data from the I²C-bus has been received after power-up, the internal soft start and protection functions do not allow any of those outputs [HDRV, BDRV, VOUT1, VOUT2 and HUNLOCK (see Fig.24)] to be active.

For supply voltages below 8.3 V the internal I²C-bus will not generate an acknowledge and the IC is in standby mode. This is because the internal protection circuit has generated a reset signal for the soft start register SOFTST. Above 8.3 V data is accepted and all registers can be loaded. If the register SOFTST has received a set from the I²C-bus, the internal soft start procedure is released, which activates all above mentioned outputs.

If during normal operation the supply voltage has dropped below 8.1 V, the protection mode is activated and HUNLOCK (pin 17) changes to the protection status and is floating. This can be detected by the microcontroller.

This protection mode has been implemented in order to protect the deflection stages and the picture tube during start-up, shut-down and fault conditions. This protection mode can be activated as shown in Table 3.

Table 3 Activation of protection mode

ACTIVATION	RESET
Low supply voltage at pin 10	increase supply voltage; reload registers; soft start via I^2C-bus
Power dip, below 8.1 V	reload registers; soft start via I^2C-bus or via supply voltage
X-ray protection XRAY (pin 2) triggered	reload registers; soft start via I^2C-bus
HPLL2 (pin 30) externally pulled to ground	release pin 30

When the protection mode is active, several pins of the TDA4856 are forced into a defined state:

HDRV (horizontal driver output) is floating

BDRV (B+ control driver output) is floating

HUNLOCK (indicates, that the frequency-to-voltage converter is out of lock) is floating (HIGH-level via external pull-up resistor)

CLBL provides a continuous blanking signal

The capacitor at HPLL2 is discharged.

If the soft start procedure is activated via the I^2C-bus, all of these actions will be performed in a well defined sequence (see Figs 24 and 25).

Power dip recognition

In standby mode the I^2C-bus will only answer with an acknowledge, when data is sent to control register with subaddress 1AH. This register contains the standby and soft start control bit.

If the I^2C-bus master transmits data to another register, an aknowledge is given after the chip address and the subaddress; an acknowledge is not given after the data. This indicates that only in soft start mode data can be stored into normal registers.

If the supply voltage dips under 8.1 V the TDA4856 leaves normal operation mode and changes into standby mode. The microcontroller can check this state by sending data into a register with the subaddress 0XH. The acknowledge will only be given on the data if the TDA4856 is active.

Due to this behaviour the start-up of the TDA4856 is defined as follows. The first data that is transferred to the TDA4856 must be sent to the control register with subaddress 1AH. Any other subaddress will not lead to an acknowledge. This is a limitation in checking the I^2C-busses of the monitor during start-up.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); all voltages measured with respect to ground.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+16	V
$V_{i(n)}$	input voltage on pins:				
	BIN		–0.5	+6.0	V
	HSYNC, VSYNC, VREF, HREF, VSMOD and HSMOD		–0.5	+6.5	V
	SDA and SCL		–0.5	+8.0	V
	XRAY		–0.5	+8.0	V
$V_{o(n)}$	output voltage on pins:				
	VOUT2, VOUT1 and HUNLOCK		–0.5	+6.5	V
	BDRV and HDRV		–0.5	+16	V
$V_{I/O(n)}$	input/output voltages at pins BOP and BSENS		–0.5	+6.0	V
$I_{o(HDRV)}$	horizontal driver output current		–	100	mA
$I_{i(HFLB)}$	horizontal flyback input current		–10	+10	mA
$I_{o(CLBL)}$	video clamping pulse/vertical blanking output current		–	–10	mA
$I_{o(BOP)}$	B+ control OTA output current		–	1	mA
$I_{o(BDRV)}$	B+ control driver output current		–	50	mA
$I_{o(EWDRV)}$	EW driver output current		–	–5	mA
$I_{o(FOCUS)}$	focus driver output current		–	–5	mA
T_{amb}	operating ambient temperature		–20	+70	°C
T_j	junction temperature		–	150	°C
T_{stg}	storage temperature		–55	+150	°C
V_{ESD}	electrostatic discharge for all pins	note 1	–150	+150	V
		note 2	–2000	+2000	V

Notes

1. Machine model: 200 pF; 0.75 µH; 10 Ω.
2. Human body model: 100 pF; 7.5 µH; 1500 Ω.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	55	K/W

QUALITY SPECIFICATION

In accordance with *"URF-4-2-59/601"*; EMC emission/immunity test in accordance with *"DIS 1000 4.6"* (IEC 801.6).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EMC}	emission test	note 1	–	1.5	–	mV
	immunity test	note 1	–	2.0	–	V

Note

1. Tests are performed with application reference board. Tests with other boards will have different results.

CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; peripheral components in accordance with Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Horizontal sync separator						
INPUT CHARACTERISTICS FOR DC-COUPLED TTL SIGNALS: PIN HSYNC						
$V_{i(HSYNC)}$	sync input signal voltage		1.7	–	–	V
$V_{HSYNC(sl)}$	slicing voltage level		1.2	1.4	1.6	V
$t_{r(HSYNC)}$	rise time of sync pulse		10	–	500	ns
$t_{f(HSYNC)}$	fall time of sync pulse		10	–	500	ns
$t_{W(HSYNC)(min)}$	minimum width of sync pulse		0.7	–	–	µs
$I_{i(HSYNC)}$	input current	V_{HSYNC} = 0.8 V	–	–	–200	µA
		V_{HSYNC} = 5.5 V	–	–	10	µA
INPUT CHARACTERISTICS FOR AC-COUPLED VIDEO SIGNALS (SYNC-ON-VIDEO, NEGATIVE SYNC POLARITY)						
V_{HSYNC}	sync amplitude of video input signal voltage	R_{source} = 50 Ω	–	300	–	mV
$V_{HSYNC(sl)}$	slicing voltage level (measured from top sync)	R_{source} = 50 Ω	90	120	150	mV
$V_{clamp(HSYNC)}$	top sync clamping voltage level	R_{source} = 50 Ω	1.1	1.28	1.5	V
$I_{ch(HSYNC)}$	charge current for coupling capacitor	$V_{HSYNC} > V_{clamp(HSYNC)}$	1.7	2.4	3.4	µA
$t_{W(HSYNC)(min)}$	minimum width of sync pulse		0.7	–	–	µs
$R_{source(max)}$	maximum source resistance	duty cycle = 7%	–	–	1500	Ω
$R_{i(diff)(HSYNC)}$	differential input resistance	during sync	–	80	–	Ω
Automatic polarity correction for horizontal sync						
$\frac{t_{P(H)}}{t_H}$	horizontal sync pulse width related to line period		–	–	25	%
$t_{d(HPOL)}$	delay time for changing polarity		0.3	–	1.8	ms
Vertical sync integrator						
$t_{int(V)}$	integration time for generation of a vertical trigger pulse	f_H = 15.625 kHz; I_{HREF} = 0.52 mA	14	20	26	µs
		f_H = 31.45 kHz; I_{HREF} = 1.052 mA	7	10	13	µs
		f_H = 64 kHz; I_{HREF} = 2.141 mA	3.9	5.7	6.5	µs
		f_H = 100 kHz; I_{HREF} = 3.345 mA	2.5	3.8	4.5	µs
Vertical sync slicer (DC-coupled, TTL compatible): pin VSYNC						
$V_{i(VSYNC)}$	sync input signal voltage		1.7	–	–	V
$V_{VSYNC(sl)}$	slicing voltage level		1.2	1.4	1.6	V
$I_{i(VSYNC)}$	input current	0 V < V_{SYNC} < 5.5 V	–	–	±10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Automatic polarity correction for vertical sync						
$t_{W(VSYNC)(max)}$	maximum width of vertical sync pulse		–	–	400	µs
$t_{d(VPOL)}$	delay for changing polarity		0.45	–	1.8	ms
Video clamping/vertical blanking output: pin CLBL						
$t_{clamp(CLBL)}$	width of video clamping pulse	measured at V_{CLBL} = 3 V	0.6	0.7	0.8	µs
$V_{clamp(CLBL)}$	top voltage level of video clamping pulse		4.32	4.75	5.23	V
TC_{clamp}	temperature coefficient of $V_{clamp(CLBL)}$		–	4	–	mV/K
$STPS_{clamp}$	steepness of slopes for clamping pulse	R_L = 1 MΩ; C_L = 20 pF	–	50	–	ns/V
$t_{d(HSYNCt-CLBL)}$	delay between trailing edge of horizontal sync and start of video clamping pulse	clamping pulse triggered on trailing edge of horizontal sync; control bit CLAMP = 0; measured at V_{CLBL} = 3 V	–	130	–	ns
$t_{clamp1(max)}$	maximum duration of video clamping pulse referenced to end of horizontal sync		–	–	1.0	µs
$t_{d(HSYNCl-CLBL)}$	delay between leading edge of horizontal sync and start of video clamping pulse	clamping pulse triggered on leading edge of horizontal sync; control bit CLAMP = 1; measured at V_{CLBL} = 3 V	–	300	–	ns
$t_{clamp2(max)}$	maximum duration of video clamping pulse referenced to end of horizontal sync		–	–	0.15	µs
$V_{blank(CLBL)}$	top voltage level of vertical blanking pulse	notes 1 and 2	1.7	1.9	2.1	V
$t_{blank(CLBL)}$	width of vertical blanking pulse at pins CLBL and HUNLOCK	control bit VBLK = 0	220	260	300	µs
		control bit VBLK = 1	305	350	395	µs
TC_{blank}	temperature coefficient of $V_{blank(CLBL)}$		–	2	–	mV/K
$V_{scan(CLBL)}$	output voltage during vertical scan	I_{CLBL} = 0	0.59	0.63	0.67	V
TC_{scan}	temperature coefficient of $V_{scan(CLBL)}$		–	–2	–	mV/K
$I_{sink(CLBL)}$	internal sink current		2.4	–	–	mA
$I_{L(CLBL)}$	external load current		–	–	–3.0	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Horizontal oscillator: pins HCAP and HREF						
$f_{fr(H)}$	free-running frequency without PLL1 action (for testing only)	$R_{HBUF} = \infty$; $R_{HREF} = 2.4\ k\Omega$; $C_{HCAP} = 10\ nF$; note 3	30.53	31.45	32.39	kHz
$\Delta f_{fr(H)}$	spread of free-running frequency (excluding spread of external components)		–	–	±3.0	%
TC_{fr}	temperature coefficient of free-running frequency		–100	0	+100	$10^{-6}/K$
$f_{H(max)}$	maximum oscillator frequency		–	–	130	kHz
V_{HREF}	voltage at input for reference current		2.43	2.55	2.68	V
Unlock blanking detection: pin HUNLOCK						
$V_{scan(HUNLOCK)}$	low level of HUNLOCK	saturation voltage in case of locked PLL1; internal sink current = 1 mA	–	–	250	mV
$V_{blank(HUNLOCK)}$	blanking level of HUNLOCK	external load current = 0	0.9	1	1.1	V
TC_{blank}	temperature coefficient of $V_{blank(HUNLOCK)}$		–	–0.9	–	mV/K
TC_{sink}	temperature coefficient of $I_{sink(HUNLOCK)}$		–	0.15	–	%/K
$I_{sink(int)}$	internal sink current	for blanking pulses; PLL1 locked	1.4	2.0	2.6	mA
$I_{L(HUNLOCK)}$	maximum external load current	$V_{HUNLOCK} = 1\ V$	–	–	–2	mA
I_L	leakage current	$V_{HUNLOCK} = 5\ V$ in case of unlocked PLL1 and/or protection active	–	–	±5	μA
PLL1 phase comparator and frequency-locked loop: pins HPLL1 and HBUF						
$t_{W(HSYNC)(max)}$	maximum width of horizontal sync pulse (referenced to line period)		–	–	25	%
$t_{lock(HPLL1)}$	total lock-in time of PLL1		–	40	80	ms
$I_{ctrl(HPLL1)}$	control currents	notes 4 and 5				
		locked mode; level 1	–	15	–	μA
		locked mode; level 2	–	145	–	μA
V_{HBUF}	buffered f/v voltage at HBUF (pin 27)	minimum horizontal frequency	–	2.55	–	V
		maximum horizontal frequency	–	0.5	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Phase adjustments and corrections via PLL1 and PLL2						
HPOS	horizontal position (referenced to horizontal period)	register HPOS = 0	–	–13	–	%
		register HPOS = 127	–	0	–	%
		register HPOS = 255	–	13	–	%
HPINBAL	horizontal pin unbalance correction via HPLL2 (referenced to horizontal period)	register HPINBAL = 0; note 6	–	–1.2	–	%
		register HPINBAL = 63; note 6	–	1.2	–	%
		register HPINBAL = 32; note 6	–	0.02	–	%
HPARAL	horizontal parallelogram correction (referenced to horizontal period)	register HPARAL = 0; note 6	–	–1.2	–	%
		register HPARAL = 63; note 6	–	1.2	–	%
		register HPARAL = 32; note 6	–	0.02	–	%
HMOIRE	relative modulation of horizontal position by $0.5f_H$; phase alternates with $0.5f_V$	register HMOIRE = 0; control bit MOD = 0	–	0	–	%
		register HMOIRE = 63; control bit MOD = 0	–	0.07	–	%
$HMOIRE_{off}$	moire cancellation off	control bit MOD = 1	–	0	–	%
PLL2 phase detector: pins HFLB and HPLL2						
ϕ_{PLL2}	PLL2 control (advance of horizontal drive with respect to middle of horizontal flyback)	maximum advance; register HPINBAL = 32; register HPARAL = 32	36	–	–	%
		minimum advance; register HPINBAL = 32; register HPARAL = 32	–	7	–	%
$I_{ctrl(PLL2)}$	PLL2 control current		–	75	–	μA
Φ_{PLL2}	relative sensitivity of PLL2 phase shift related to horizontal period		–	28	–	mV/%
$V_{PROT(HPLL2)(max)}$	maximum voltage for PLL2 protection mode/soft start		–	4.6	–	V
$I_{ch(HPLL2)}$	charge current for external capacitor during soft start	$V_{HPLL2} < 3.7$ V	–	1	–	μA
$I_{dch(HPLL2)}$	discharge current for external capacitor during soft down	$V_{HPLL2} < 3.7$ V	–	–1	–	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
HORIZONTAL FLYBACK INPUT: PIN HFLB						
$V_{pos(HFLB)}$	positive clamping level	I_{HFLB} = 5 mA	–	5.5	–	V
$V_{neg(HFLB)}$	negative clamping level	I_{HFLB} = –1 mA	–	–0.75	–	V
$I_{pos(HFLB)}$	positive clamping current		–	–	6	mA
$I_{neg(HFLB)}$	negative clamping current		–	–	–2	mA
$V_{sl(HFLB)}$	slicing level		–	2.8	–	V
Output stage for line driver pulses: pin HDRV						
OPEN-COLLECTOR OUTPUT STAGE						
$V_{sat(HDRV)}$	saturation voltage	I_{HDRV} = 20 mA	–	–	0.3	V
		I_{HDRV} = 60 mA	–	–	0.8	V
$I_{LO(HDRV)}$	output leakage current	V_{HDRV} = 16 V	–	–	10	μA
AUTOMATIC VARIATION OF DUTY CYCLE						
$t_{HDRV(OFF)}/t_H$	relative t_{OFF} time of HDRV output; measured at V_{HDRV} = 3 V; HDRV duty cycle is modulated by the relation I_{HREF}/I_{VREF}	I_{HDRV} = 20 mA; f_H = 31.45 kHz; see Fig.16	42	45	48	%
		I_{HDRV} = 20 mA; f_H = 58 kHz; see Fig.16	45.5	48.5	51.5	%
		I_{HDRV} = 20 mA; f_H = 110 kHz; see Fig.16	49	52	55	%
X-ray protection: pin XRAY						
$V_{XRAY(sl)}$	slicing voltage level for latch		6.22	6.39	6.56	V
$t_{W(XRAY)(min)}$	minimum width of trigger pulse		–	–	30	μs
$R_{i(XRAY)}$	input resistance at XRAY (pin 2)	V_{XRAY} < 6.38 V + V_{BE}	500	–	–	kΩ
		V_{XRAY} > 6.38 V + V_{BE}	–	5	–	kΩ
		standby mode	–	5	–	kΩ
$XRAY_{rst}$	reset of X-ray latch	pin 9 open-circuit or connected to GND	set control bit SOFTST via I^{2}C-bus			
		pin 9 connected to V_{CC} via R_{XSEL}	switch off V_{CC}, then re-apply V_{CC}			
$V_{CC(XRAY)(min)}$	minimum supply voltage for correct function of the X-ray latch	pin 9 connected to V_{CC} via R_{XSEL}	–	–	4	V
$V_{CC(XRAY)(max)}$	maximum supply voltage for reset of the X-ray latch	pin 9 connected to V_{CC} via R_{XSEL}	2	–	–	V
R_{XSEL}	external resistor at pin 9	no reset via I^{2}C-bus	56	–	130	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical oscillator [oscillator frequency in application without adjustment of free-running frequency $f_{fr(V)}$]						
$f_{fr(V)}$	free-running frequency	R_{VREF} = 22 kΩ; C_{VCAP} = 100 nF	40	42	43.3	Hz
$f_{cr(V)}$	vertical frequency catching range	constant amplitude; note 7	50	–	160	Hz
V_{VREF}	voltage at reference input for vertical oscillator		–	3.0	–	V
$t_{d(scan)}$	delay between trigger pulse and start of ramp at VCAP (pin 24) (width of vertical blanking pulse)	control bit VBLK = 0	220	260	300	μs
		control bit VBLK = 1	305	350	395	μs
I_{VAGC}	currents of amplitude control	control bit AGCDIS = 0	±120	±200	±300	μA
		control bit AGCDIS = 1	–	0	–	μA
C_{VAGC}	external capacitor at VAGC (pin 22)		150	–	220	nF
Differential vertical current outputs						
ADJUSTMENT OF VERTICAL SIZE INCLUDING VGA AND EHT COMPENSATION; see Figs 3 and 4						
VGAIN	vertical size (gain) without VGA overscan (referenced to nominal vertical size)	register VGAIN = 0; register VSIZE = 127; bit VOVSCN = 0; note 8	–	70	–	%
		register VGAIN = 63; register VSIZE = 127; bit VOVSCN = 0; note 8	–	100	–	%
VSIZE	vertical size (size) without VGA overscan (referenced to nominal vertical size)	register VSIZE = 0; register VGAIN = 63; bit VOVSCN = 0; note 8	–	60	–	%
		register VSIZE = 127; register VGAIN = 63; bit VOVSCN = 0; note 8	–	100	–	%
$VSIZE_{VGA}$	vertical size with VGA overscan (referenced to nominal vertical size)	register VSIZE = 0; register VGAIN = 63; bit VOVSCN = 1; note 8	–	70	–	%
		register VSIZE = 127; register VGAIN = 63; bit VOVSCN = 1; note 8	115.9	116.8	117.7	%
$VSMOD_{EHT}$	EHT compensation on vertical size via VSMOD (pin 21) (referenced to 100% vertical size)	I_{VSMOD} = 0	–	0	–	%
		I_{VSMOD} = –120 μA	–	–7	–	%
$I_{i(VSMOD)}$	input current (pin 21)	VSMOD = 0	–	0	–	μA
		VSMOD = –7%	–	–120	–	μA
$R_{i(VSMOD)}$	input resistance		300	–	500	Ω
$V_{ref(VSMOD)}$	reference voltage at input		–	5.0	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$f_{ro(VSMOD)}$	roll-off frequency (–3 dB)	I_{VSMOD} = –60 µA + 15 µA (RMS value)	1	–	–	MHz
ADJUSTMENT OF VERTICAL POSITION (see Fig.5)						
VOFFS	vertical position (referenced to 100% vertical size)	register VOFFS = 0	–	–4	–	%
		register VOFFS = 15	–	4	–	%
		register VOFFS = 8	–	0.25	–	%
VPOS	vertical position (referenced to 100% vertical size)	register VPOS = 0	–	–11.5	–	%
		register VPOS = 127	–	11.5	–	%
		register VPOS = 64	–	0.09	–	%
ADJUSTMENT OF VERTICAL LINEARITY; see Fig.6						
VLIN	vertical linearity (S-correction)	register VLIN = 0; control bit VSC = 0; note 8	–	2	–	%
		register VLIN = 15; control bit VSC = 0; note 8	–	46	–	%
		register VLIN = X; control bit VSC = 1; note 8	–	0	–	%
δVLIN	symmetry error of S-correction	maximum VLIN	–	–	±0.7	%
ADJUSTMENT OF VERTICAL LINEARITY BALANCE; see Fig.7						
VLINBAL	vertical linearity balance (referenced to 100% vertical size)	register VLINBAL = 0; note 8	–1.85	–1.40	–0.95	%
		register VLINBAL = 15; note 8	0.95	1.40	1.85	%
		register VLINBAL = 8; note 8	–	0.08	–	%
VMOIRE	modulation of vertical picture position by ½ vertical frequency (related to 100% vertical size)	register VMOIRE = 0; control bit MOD = 0	–	0	–	%
		register VMOIRE = 63; control bit MOD = 0	–	0.08	–	%
	moire cancellation off	control bit MOD = 1	–	0	–	%
Vertical output stage: pins VOUT1 and VOUT2; see Fig.27						
$\Delta I_{VOUT(nom)(p-p)}$	nominal differential output current (peak-to-peak value)	$\Delta I_{VOUT} = I_{VOUT1} - I_{VOUT2}$; nominal settings; note 8	0.76	0.85	0.94	mA
$I_{o(VOUT)(max)}$	maximum output current at pins VOUT1 and VOUT2	control bit VOVSCN = 1	0.54	0.6	0.66	mA
V_{VOUT}	allowed voltage at outputs		0	–	4.2	V
$\delta I_{os(vert)(max)}$	maximum offset error of vertical output currents	nominal settings; note 8	–	–	±2.5	%
$\delta I_{lin(vert)(max)}$	maximum linearity error of vertical output currents	nominal settings; note 8	–	–	±1.5	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EW drive output						
EW DRIVE OUTPUT STAGE: pin EWDRV; see Figs 8 to 11						
$V_{const(EWDRV)}$	bottom output voltage at pin EWDRV (internally stabilized)	register HPIN = 0; register HTRAP = 32; register HSIZE = 255; control bit VSC = 1	1.05	1.2	1.35	V
$V_{o(EWDRV)(max)}$	maximum output voltage	note 9	7.0	–	–	V
$I_{L(EWDRV)}$	load current		–	–	±2	mA
TC_{EWDRV}	temperature coefficient of output signal		–	–	600	10^{-6}/K
$V_{HPIN(EWDRV)}$	horizontal pincushion	register HPIN = 0; control bit VSC = 1; note 8	–	0.04	–	V
		register HPIN = 63; control bit VSC = 1; note 8	–	1.42	–	V
$V_{HCORT(EWDRV)}$	horizontal corner correction at top of picture	register HCORT = 0; control bit VSC = 0; note 8	–	0.2	–	V
		register HCORT = 63; control bit VSC = 0; note 8	–	–0.64	–	V
		register HCORT = X; control bit VSC = 1; note 8	–	0	–	V
$V_{HCORB(EWDRV)}$	horizontal corner correction at bottom of picture	register HCORB = 0; control bit VSC = 0; note 8	–	0.2	–	V
		register HCORB = 63; control bit VSC = 0; note 8	–	–0.64	–	V
		register HCORB = X; control bit VSC = 1; note 8	–	0	–	V
$V_{HTRAP(EWDRV)}$	horizontal trapezium correction	register HTRAP = 63; note 8	–	–0.5	–	V
		register HTRAP = 0; note 8	–	0.5	–	V
		register HTRAP = 32; note 8	–	–0.01	–	V
$V_{HSIZE(EWDRV)}$	horizontal size	register HSIZE = 255; note 8	–	0.13	–	V
		register HSIZE = 0; note 8	–	3.6	–	V
$V_{HEHT(EWDRV)}$	EHT compensation on horizontal size via HSMOD (pin 31)	I_{HSMOD} = 0; note 8	–	0.02	–	V
		I_{HSMOD} = –120 μA; note 8	–	0.69	–	V
$I_{i(HSMOD)}$	input current (pin 31)	V_{HEHT} = 0.02 V	–	0	–	μA
		V_{HEHT} = 0.69 V	–	–120	–	μA
$R_{i(HSMOD)}$	input resistance		300	–	500	Ω
$V_{ref(HSMOD)}$	reference voltage at input	I_{HSMOD} = 0	–	5.0	–	V
$f_{ro(HSMOD)}$	roll-off frequency (–3 dB)	I_{HSMOD} = –60 μA + 15 μA (RMS)	1	–	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TRACKING OF EWDRV OUTPUT SIGNAL WITH HORIZONTAL FREQUENCY PROPORTIONAL VOLTAGE						
$f_{H(MULTI)}$	horizontal frequency range for tracking		15	–	80	kHz
$V_{PAR(EWDRV)}$	parabola amplitude at EWDRV (pin 11)	I_{HREF} = 1.052 mA; f_H = 31.45 kHz; control bit FHMULT = 1; note 10	–	0.72	–	V
		I_{HREF} = 2.341 mA; f_H = 70 kHz; control bit FHMULT = 1; note 10	–	1.42	–	V
		function disabled; control bit FHMULT = 0; note 10	–	1.42	–	V
LE_{EWDRV}	linearity error of horizontal frequency tracking		–	–	8	%
Output for asymmetric EW corrections: pin ASCOR						
$V_{HPARAL(ASCOR)}$	vertical sawtooth voltage for EW parallelogram correction	register HPARAL = 0; note 8	–	–0.825	–	V
		register HPARAL = 63; note 8	–	0.825	–	V
		register HPARAL = 32; note 8	–	0.05	–	V
$V_{HPINBAL(ASCOR)}$	vertical parabola for pin unbalance correction	register HPINBAL = 0; note 8	–	–1.0	–	V
		register HPINBAL = 63; note 8	–	1.0	–	V
		register HPINBAL = 32; note 8	–	0.05	–	V
$V_{o(ASCOR)(max)(p-p)}$	maximum output voltage swing (peak-to-peak value)		–	4	–	V
$V_{o(ASCOR)(max)}$	maximum output voltage		–	6.5	–	V
$V_{c(ASCOR)}$	centre voltage		–	4.0	–	V
$V_{o(ASCOR)(min)}$	minimum output voltage		–	1.9	–	V
$I_{o(ASCOR)(max)}$	maximum output current	$V_{ASCOR} \geq 1.9$ V	–	–1.5	–	mA
$I_{o(sink)(ASCOR)(max)}$	maximum output sink current	$V_{ASCOR} \geq 1.9$ V	–	50	–	µA
Focus section: pin FOCUS; see Figs 15 and 28						
t_{precor}	pre-correction of phase for horizontal focus parabola	register HFOCAD = 0	–	300	–	ns
		register HFOCAD = 1	–	350	–	ns
		register HFOCAD = 2	–	400	–	ns
		register HFOCAD = 3	–	450	–	ns
$t_{W(hfb)(min)}$	minimum horizontal flyback pulse width		1.9	–	–	µs
$t_{W(hfb)(max)}$	maximum horizontal flyback pulse width		–	–	5.5	µs

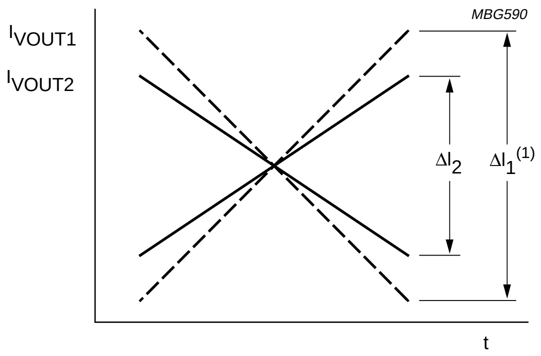
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{W(hfb)(off)}$	minimum width of horizontal flyback pulse for operation without pre-correction		–	7.5	–	μs
$V_{HFOCUS(p-p)}$	amplitude of horizontal focus parabola (peak-to-peak value)	register HFOCUS = 0	–	0.06	–	V
		register HFOCUS = 31	–	3.3	–	V
$V_{VFOCUS(p-p)}$	amplitude of vertical parabola (peak-to-peak value)	register VFOCUS = 0; note 8	–	0.02	–	V
		register VFOCUS = 15; note 8	–	1.1	–	V
$V_{o(FOCUS)(max)}$	maximum output voltage	$I_{FOCUS} = 0$	6.15	6.4	6.65	V
$V_{o(FOCUS)(min)}$	minimum output voltage	$I_{FOCUS} = 0$	1.0	1.3	1.6	V
$I_{o(FOCUS)(max)}$	maximum output current		±1.5	–	–	mA
$C_{L(FOCUS)(max)}$	maximum capacitive load		–	–	20	pF
B+ control section; see Figs 22 and 23						
TRANSCONDUCTANCE AMPLIFIER: PINS BIN AND BOP						
$V_{i(BIN)}$	input voltage		0	–	5.25	V
$I_{i(BIN)(max)}$	maximum input current		–	–	±1	μA
$V_{ref(int)}$	reference voltage at internal non-inverting input of OTA		2.37	2.5	2.58	V
$V_{o(BOP)(min)}$	minimum output voltage		–	–	0.5	V
$V_{o(BOP)(max)}$	maximum output voltage	$I_{BOP} < 1$ mA	5.0	5.3	5.6	V
$I_{o(BOP)(max)}$	maximum output current		–	±500	–	μA
$g_{m(OTA)}$	transconductance of OTA	note 11	30	50	70	mS
$G_{v(ol)}$	open-loop voltage gain	note 12	–	86	–	dB
$C_{BOP(min)}$	minimum value of capacitor at BOP		10	–	–	nF
VOLTAGE COMPARATOR: PIN BSENS						
$V_{i(BSENS)}$	voltage range of positive comparator input		0	–	5	V
$V_{i(BOP)}$	voltage range of negative comparator input		0	–	5	V
$I_{L(BSENS)(max)}$	maximum leakage current	discharge disabled	–	–	–2	μA
OPEN-COLLECTOR OUTPUT STAGE: PIN BDRV						
$I_{o(BDRV)(max)}$	maximum output current	note 13	20	–	–	mA
$I_{LO(BDRV)}$	output leakage current	$V_{BDRV} = 16$ V	–	–	3	μA
$V_{sat(BDRV)}$	saturation voltage	$I_{BDRV} < 20$ mA	–	–	300	mV
$t_{off(BDRV)(min)}$	minimum off-time		–	250	–	ns
$t_{d(BDRV-HDRV)}$	delay between BDRV pulse and HDRV pulse	measured at $V_{HDRV} = V_{BDRV} = 3$ V	–	500	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BSENS DISCHARGE CIRCUIT: PIN BSENS						
$V_{STOP(BSENS)}$	discharge stop level	capacitive load; I_{BSENS} = 0.5 mA	0.85	1.0	1.15	V
$I_{dch(BSENS)}$	discharge current	V_{BSENS} > 2.5 V	4.5	6.0	7.5	mA
$V_{th(BSENS)(restart)}$	threshold voltage for restart	fault condition	1.2	1.3	1.4	V
$C_{BSENS(min)}$	minimum value of capacitor at BSENS (pin 4)		2	–	–	nF
Internal reference, supply voltage, soft start and protection						
$V_{CC(stab)}$	external supply voltage for complete stabilization of all internal references		9.2	–	16	V
I_{CC}	supply current		–	70	–	mA
$I_{CC(stb)}$	standby supply current	STDBY = 1; V_{PLL2} < 1 V; 3.5 V < V_{CC} < 16 V	–	9	–	mA
PSRR	power supply rejection ratio of internal supply voltage	f = 1 kHz	50	–	–	dB
$V_{CC(blank)}$	supply voltage level for activation of continuous blanking	V_{CC} decreasing from 12 V	8.2	8.6	9.0	V
$V_{CC(blank)(min)}$	minimum supply voltage level for function of continuous blanking	V_{CC} decreasing from 12 V	2.5	3.5	4.0	V
$V_{on(VCC)}$	supply voltage level for activation of HDRV, BDRV, VOUT1, VOUT2 and HUNLOCK	V_{CC} increasing from below typical 8.1 V	7.9	8.3	8.7	V
$V_{off(VCC)}$	supply voltage level for deactivation of BDRV, VOUT1, VOUT2 and HUNLOCK; also sets register SOFTST	V_{CC} decreasing from above typical 8.3 V	7.7	8.1	8.5	V
THRESHOLDS DERIVED FROM HPLL2 VOLTAGE						
$V_{HPLL2(blank)(ul)}$	upper limit voltage for continuous blanking		–	4.6	–	V
$V_{HPLL2(bduty)(ul)}$	upper limit voltage for variation of BDRV duty cycle		–	4.0	–	V
$V_{HPLL2(bduty)(ll)}$	lower limit voltage for variation of BDRV duty cycle		–	3.2	–	V
$V_{HPLL2(hduty)(ul)}$	upper limit voltage for variation of HDRV duty cycle		–	3.2	–	V
$V_{HPLL2(hduty)(ll)}$	lower limit voltage for variation of HDRV duty cycle		–	1.8	–	V
$V_{HPLL2(stb)(ul)}$	upper limit voltage for standby voltage		–	1	–	V

Notes

1. For duration of vertical blanking pulse see subheading 'Vertical oscillator [oscillator frequency in application without adjustment of free-running frequency $f_{fr(V)}$]'.
2. Continuous blanking at CLBL (pin 16) will be activated, if one of the following conditions is true:
   a) No horizontal flyback pulses at HFLB (pin 1) within a line
   b) X-ray protection is triggered
   c) Voltage at HPLL2 (pin 30) is low during soft start
   d) Supply voltage at V_{CC} (pin 10) is low
   e) PLL1 unlocked while frequency-locked loop is in search mode.
3. Oscillator frequency is f_{min} when no sync input signal is present (continuous blanking at pins 16 and 17).
4. Loading of HPLL1 (pin 26) is not allowed.
5. Voltage at HPLL1 (pin 26) is fed to HBUF (pin 27) via a buffer. Disturbances caused by horizontal sync are removed by an internal sample-and-hold circuit.
6. All vertical and EW adjustments according note 8, but VSIZE = 80% (register VSIZE = 63, VGAIN = 63 and control bit VOVSCN = 0).
7. Value of resistor at VREF (pin 23) may not be changed.
8. All vertical and EW adjustments are specified at nominal vertical settings; unless otherwise specified, which means:
   a) VSIZE = 100% (register VSIZE = 127, VGAIN = 63 and control bit VOVSCN = 0)
   b) VSMOD = 0 (no EHT compensation)
   c) VPOS centred (register VPOS = 64)
   d) VLIN = 0 (register VLIN = X and control bit VSC = 1)
   e) VLINBAL = 0 (register VLINBAL = 8)
   f) FHMULT = 0
   g) HPARAL = 0 (register HPARAL = 32)
   h) HPINBAL = 0 (register HPINBAL = 32)
   i) Vertical oscillator synchronized.
9. The output signal at EWDRV (pin 11) may consist of horizontal pincushion + corner correction + DC shift + trapezium correction. If the control bit VOVSCN is set, and the VPOS adjustment is set to an extreme value, the tip of the parabola may be clipped at the upper limit of the EWDRV output voltage range. The waveform of corner correction will clip if the vertical sawtooth adjustment exceeds 110% of the nominal setting.
10. If f_H tracking is enabled, the amplitude of the complete EWDRV output signal (horizontal pincushion + corner correction + DC shift + trapezium) will be changed proportional to I_{HREF}. The EWDRV low level of 1.2 V remains fixed.
11. First pole of transconductance amplifier is 5 MHz without external capacitor (will become the second pole, if the OTA operates as an integrator).
12. Open-loop gain is $\frac{V_{BOP}}{V_{BIN}}$ at f = 0 with no resistive load and C_{BOP} = 10 nF [from BOP (pin 3) to GND].
13. The recommended value for the pull-up resistor BDRV (pin 6) is 1 kΩ.

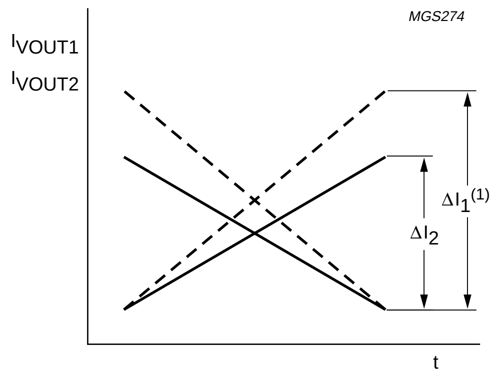
Vertical and EW adjustments



(1) ΔI_1 is the maximum amplitude setting at register VSIZE = 127, register VGAIN = 63, control bit VOVSCN = 0.

$$VSIZE = \frac{\Delta I_2}{\Delta I_1} \times 100\%, \quad VSMOD = \frac{\Delta I_2}{\Delta I_1} \times 100\%$$

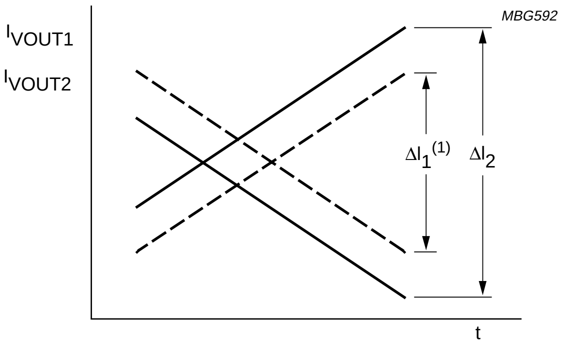
Fig.3 Adjustment of vertical size (VSIZE).



(1) ΔI_1 is the maximum amplitude setting at register VSIZE = 127, register VGAIN = 63, control bit VOVSCN = 0.

$$VGAIN = \frac{\Delta I_2}{\Delta I_1} \times 100\%$$

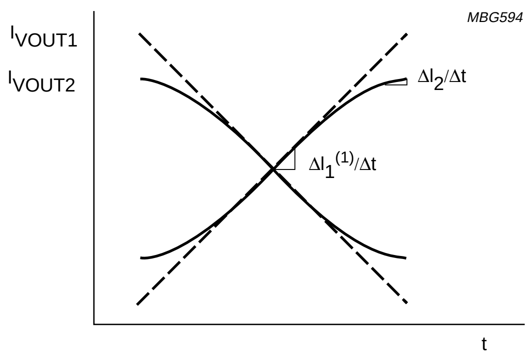
Fig.4 Adjustment of vertical size (VGAIN).



(1) ΔI_1 is the maximum amplitude setting at register VSIZE = 127 and register VGAIN = 63.

$$VPOS = \frac{\Delta I_2 - \Delta I_1}{2 \times \Delta I_1} \times 100\%, \quad VOFFS = \frac{\Delta I_2 - \Delta I_1}{2 \times \Delta I_1} \times 100\%$$

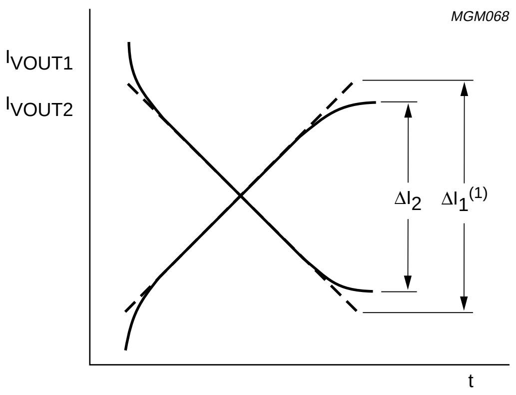
Fig.5 Adjustment of vertical position.



(1) ΔI_1 is the maximum amplitude setting at register VSIZE = 127 and VLIN = 0%.

$$VLIN = \frac{\Delta I_1 - \Delta I_2}{\Delta I_1} \times 100\%$$

Fig.6 Adjustment of vertical linearity (vertical S-correction).



(1) ΔI_1 is the maximum amplitude setting at register VSIZE = 127 and register VOVSCN = 0.

$$VLINBAL = \frac{\Delta I_1 - \Delta I_2}{2 \times \Delta I_1} \times 100\%$$

Fig.7 Adjustment of vertical linearity balance.

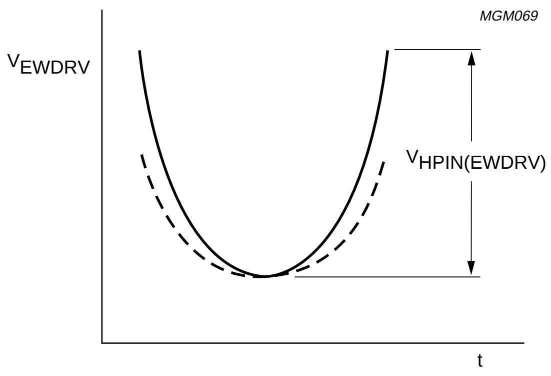


Fig.8 Adjustment of parabola amplitude at pin EWDRV.

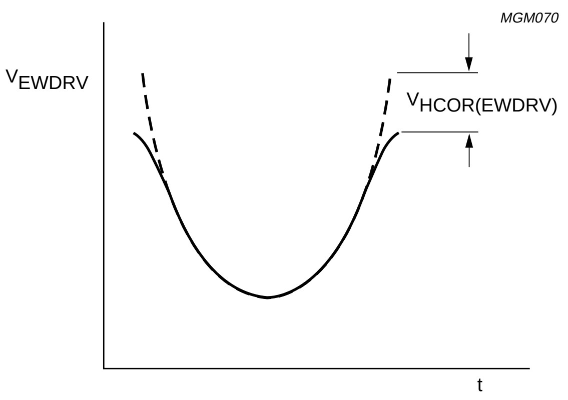


Fig.9 Influence of corner correction at pin EWDRV.

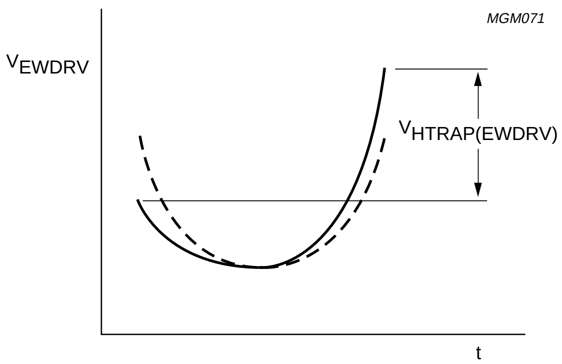


Fig.10 Influence of trapezium at pin EWDRV.

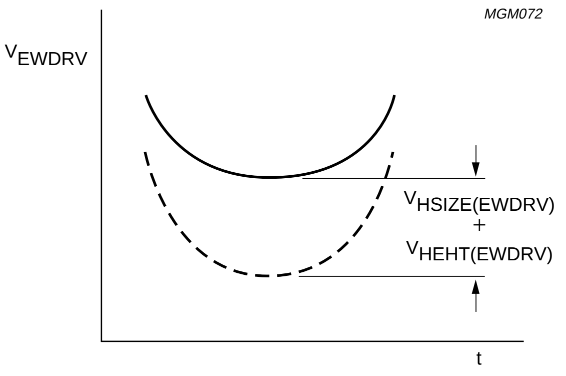


Fig.11 Influence of HSIZE and EHT compensation at pin EWDRV.

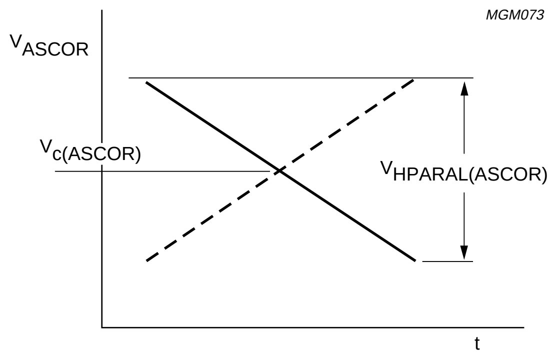


Fig.12 Adjustment of parallelogram at pin ASCOR.

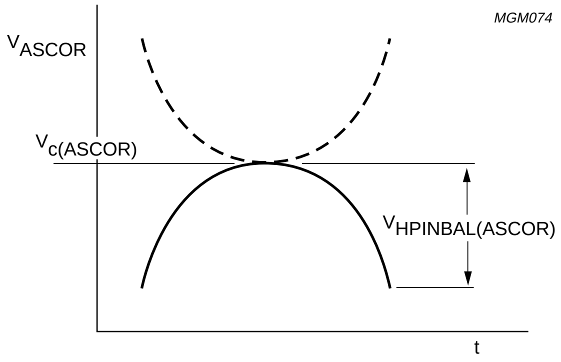


Fig.13 Adjustment of pin balance at pin ASCOR.

Pulse diagrams

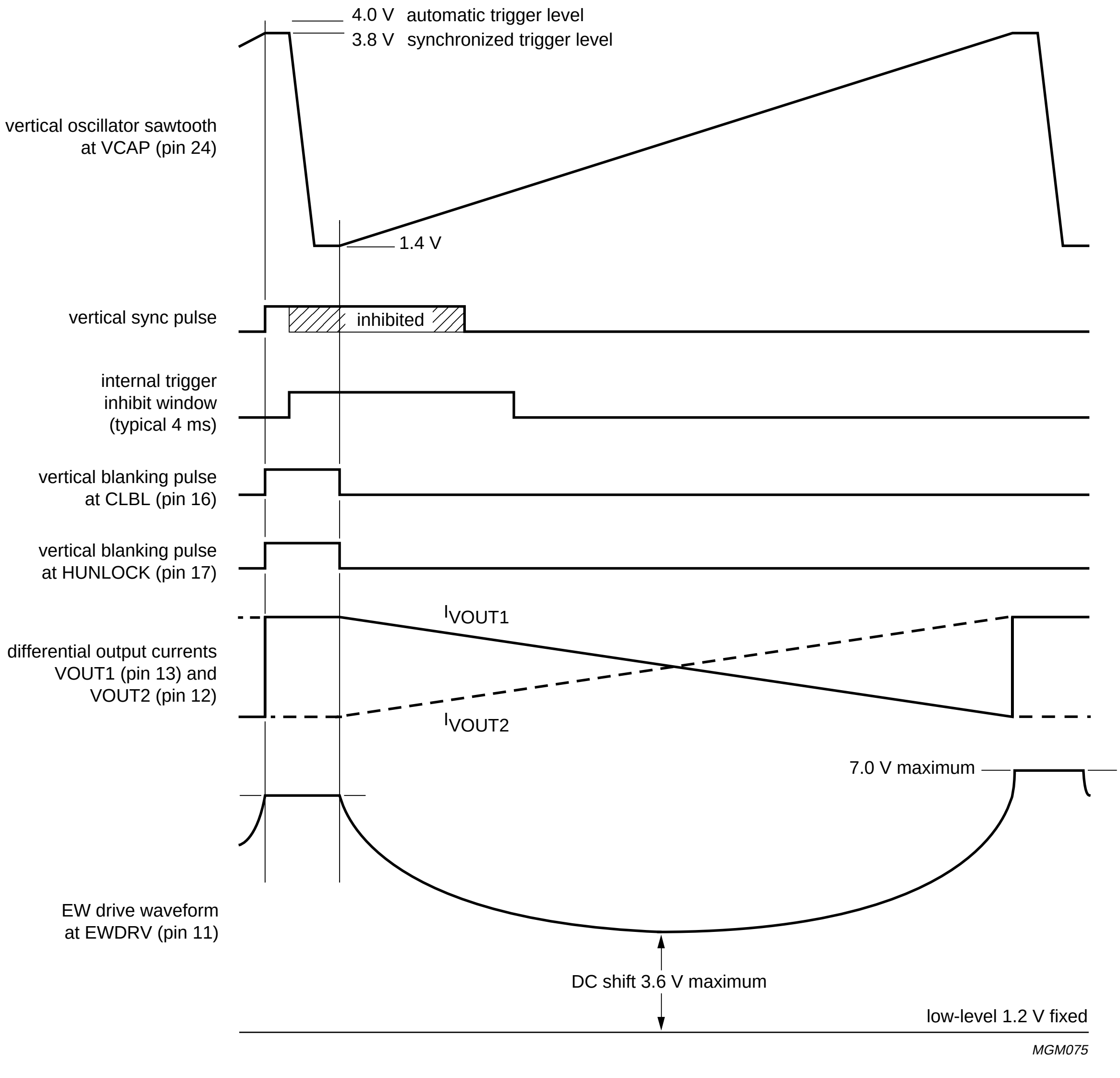


Fig.14 Pulse diagram for vertical part.

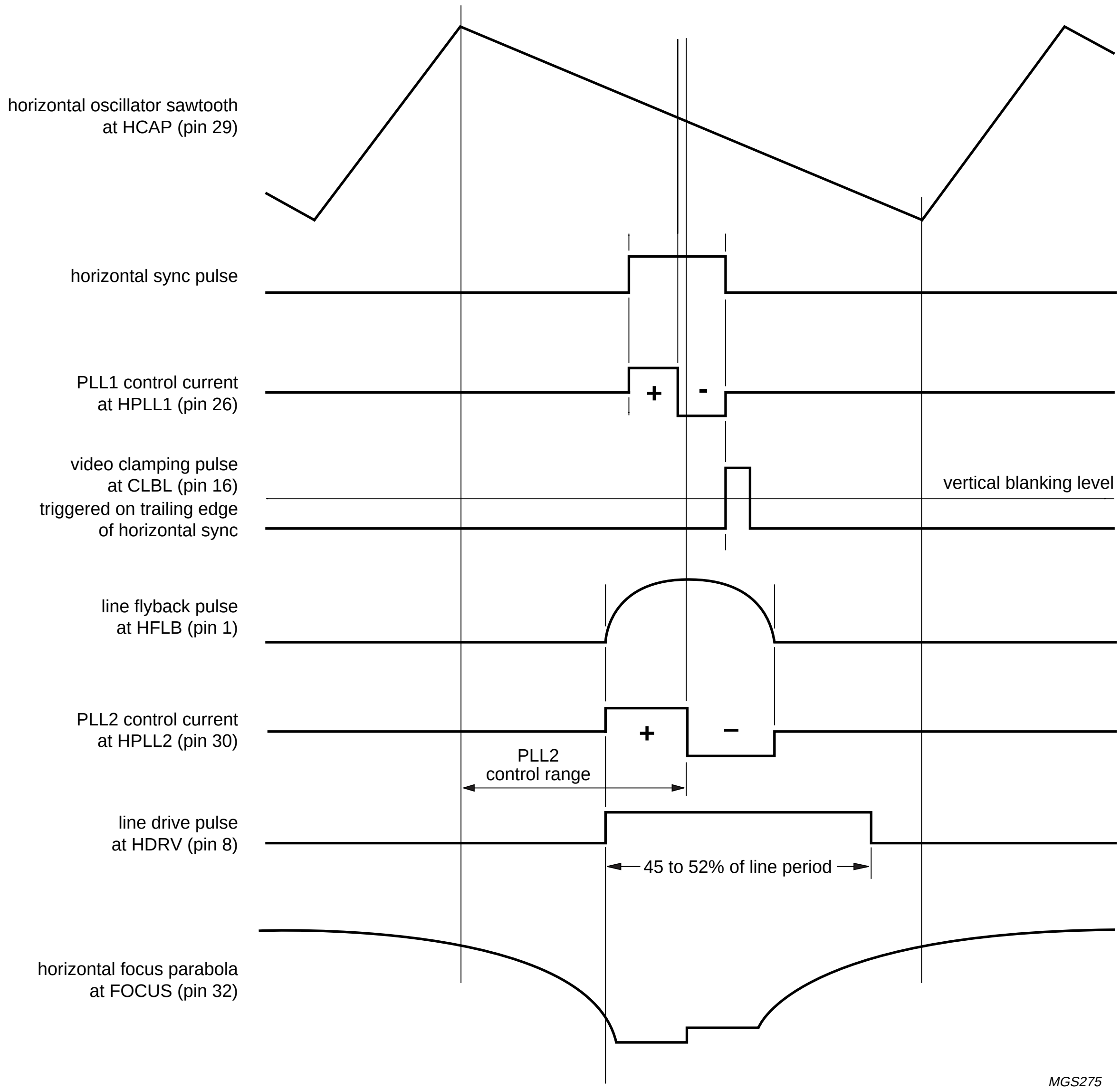


Fig.15 Pulse diagram for horizontal part.

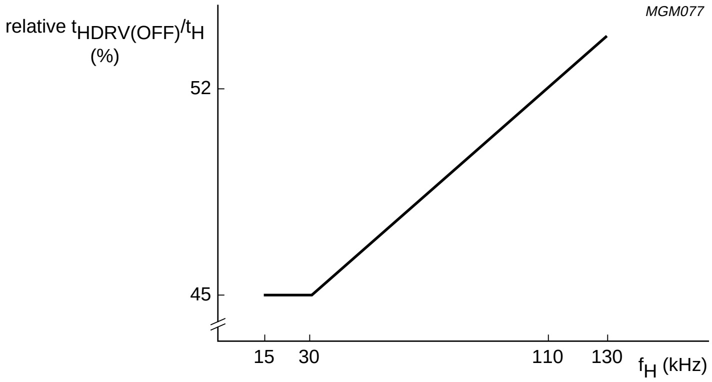
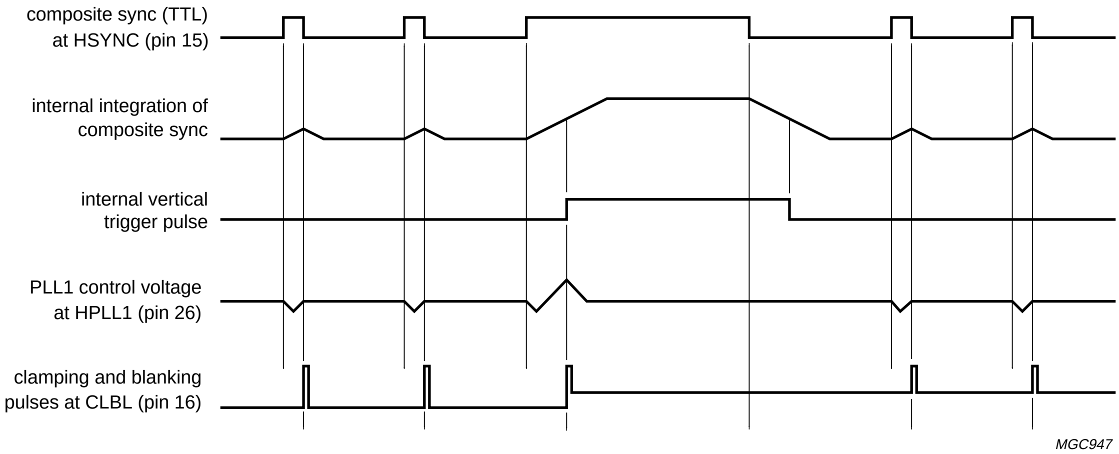
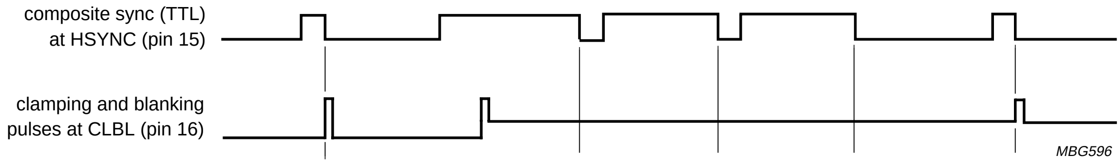


Fig.16 Relative t_{OFF} time of HDRV versus H-frequency.



a. Reduced influence of vertical sync on horizontal phase.



b. Generation of video clamping pulses during vertical sync with serration pulses.

Fig.17 Pulse diagrams for composite sync applications.

I^2C-BUS PROTOCOL

Data format

Table 4 Data format

S[(1)]	SLAVE ADDRESS[(2)]	A[(3)]	SUB-ADDRESS[(4)]	A[(3)]	DATA[(5)]	A[(3)]	P[(6)]

Notes

1. S = START condition.
2. SLAVE ADDRESS (MAD) = 1000 1100.
3. A = acknowledge, generated by the slave. No acknowledge, if the supply voltage is below 8.2 V for start-up and 8.0 V for shut-down procedure.
4. SUBADDRESS (SAD).
5. DATA byte. If more than 1 byte of DATA is transmitted, then **no** auto-increment of the significant subaddress is performed.
6. P = STOP condition.

It should be noted that clock pulses according to the 400 kHz specification are accepted for 3.3 and 5 V applications (reference level = 1.8 V).

Default register values after power-up are random. All registers have to be preset via software before the soft start is enabled.

Important: If register contents are changed during the vertical scan, this might result in a visible interference on the screen. The cause for this interference is the abrupt change of picture geometry which takes effect at random locations within the visible picture. To avoid this kind of interference, at least the adjustment of some critical geometry parameters should be synchronized with the vertical flyback. The TDA4856 offers a feature to synchronize any I^2C-bus adjustment with the internal vertical flyback pulse. For this purpose the IC offers two different modes for the handling of I^2C-bus data:

- Direct mode
- Buffered mode.

Direct mode

The direct mode is selected by setting the MSB of the I^2C-bus register subaddress to logic 0.

Any I^2C-bus command is executed immediately after it was received, so the adjustment takes effect immediately after the end of I^2C-bus transmission.

This mode should be used if many register values have to be changed subsequently, i.e. during start-up, mode change, etc., and while there is no picture visible on the screen (blanked). The number of transmissions per V-period is not limited.

Buffered mode

The buffered mode is selected by setting the MSB of the I^2C-bus register subaddress to logic 1.

This mode is designed to avoid visible interferences on the screen during the I^2C-bus adjustments. This mode should be used, if a single register has to be changed while the picture is visible, so i.e. for user adjustments.

One received I^2C-bus data byte is stored in an internal 8-bit buffer before it is passed to the DAC section. The first internal vertical blanking pulse (VBL) after end of transmission is used to synchronize the adjustment change with the vertical flyback. So the actual change of the picture size, position, geometry, etc. will take place during the vertical flyback period, and will thus be invisible.

The IC gives acknowledge for chip address, subaddress and data of a buffered transmission. Only one I^2C-bus transmission is accepted after each vertical blank. After one buffered transmission, the IC gives no acknowledge for further transmissions until next VBL pulse has occurred. The buffered mode is disabled while the IC is in standby mode.

List of I²C-bus controlled switches

I²C-bus data can be transmitted in direct or buffered mode and is defined by the MSB of the register subaddress:

- SAD1 is the register subaddress to be used for transmissions in direct mode
- SAD2 is the register subaddress to be used for transmissions in buffered mode.

Table 5 Controlled switches; notes 1 and 2

CONTROL BIT	FUNCTION	SAD1 (HEX)	SAD2 (HEX)	REGISTER ASSIGNMENT							
				D7	D6	D5	D4	D3	D2	D1	D0
BLKDIS	0: vertical, protection and horizontal unlock blanking available on pins CLBL and HUNLOCK	0A	8A	X	D6	#	#	#	#	#	#
	1: only vertical and protection blanking available on pins CLBL and HUNLOCK										
AGCDIS	0: AGC in vertical oscillator active	0B	8B	#	D6	#	#	#	#	#	#
	1: AGC in vertical oscillator inhibited										
FHMULT	0: EW output independent of horizontal frequency	0B	8B	D7	#	#	#	#	#	#	#
	1: EW output tracks with horizontal frequency										
VSC	0: VLIN, HCORT and HCORB adjustments enabled	02	82	X	D6	#	#	#	#	#	#
	1: VLIN, HCORT and HCORB adjustments forced to centre value										
MOD	0: horizontal and vertical moire cancellation enabled	08	88	D7	#	#	#	#	#	#	#
	1: horizontal and vertical moire cancellation disabled										
VOVSCN	0: vertical size 100%	0F	8F	X	D6	#	#	#	#	#	#
	1: vertical size 116.8% for VGA350										
CLAMP	0: trailing edge for horizontal clamp	09	89	#	D6	#	#	#	#	#	#
	1: leading edge for horizontal clamp										
VBLK	0: vertical blanking = 260 μs	09	89	D7	#	#	#	#	#	#	#
	1: vertical blanking = 340 μs										
ACD	0: ASCOR disconnected from PLL2	04	84	X	D6	#	#	#	#	#	#
	1: ASCOR internally connected with PLL2										
STDBY(3)	0: internal power supply enabled	1A	9A	#	X	X	X	X	X	#	D0
	1: internal power supply disabled										
SOFTST(3)	0: soft start not released (pin HPLL2 pulled to ground)	1A	9A	#	X	X	X	X	X	D1	#
	1: soft start is released (power-up via pin HPLL2)										

Notes

1. X = don't care.
2. # = this bit is occupied by another function. If the register is addressed, the bit values for both functions must be transferred.
3. Bits STDBY and SOFTST can be reset by the internal protection circuit.

List of I²C-bus controlled functions

I²C-bus data can be transmitted in direct or buffered mode and is defined by the MSB of the register subaddress:

- SAD1 is the register subaddress to be used for transmissions in direct mode
- SAD2 is the register subaddress to be used for transmissions in buffered mode.

Table 6 Controlled functions; notes 1 and 2

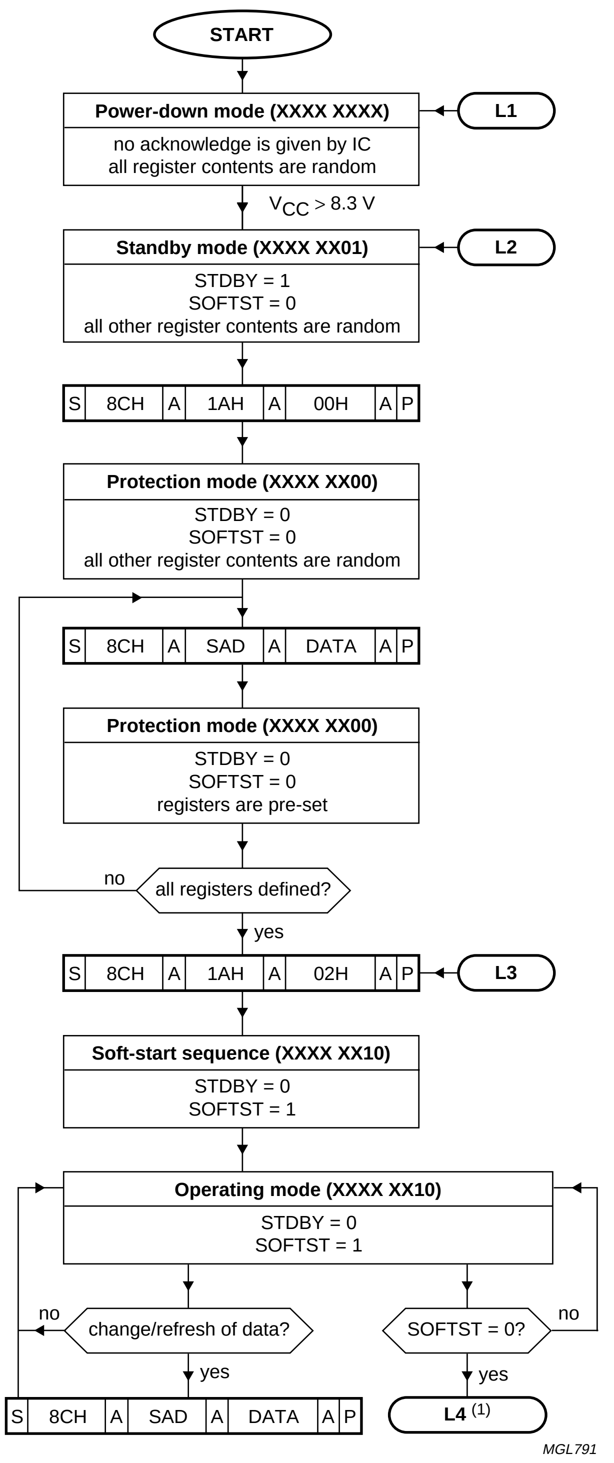
FUNCTION	NAME	BITS	SAD1 (HEX)	SAD2 (HEX)	REGISTER ASSIGNMENT								CONTROL BIT	RANGE	FUNCTION TRACKS WITH
					D7	D6	D5	D4	D3	D2	D1	D0			
Horizontal size	HSIZE	8	01	81	D7	D6	D5	D4	D3	D2	D1	D0	–	0.1 to 3.6 V	–
Horizontal position	HPOS	8	07	87	D7	D6	D5	D4	D3	D2	D1	D0	–	±13% of horizontal period	–
Horizontal pincushion	HPIN	6	0F	8F	X	#	D5	D4	D3	D2	D1	D0	–	0 to 1.42 V	VSIZE, VOVSCN, VPOS, HSIZE and HSMOD
Horizontal trapezium correction	HTRAP	6	03	83	X	X	D5	D4	D3	D2	D1	D0	–	±500 mV (p-p)	VSIZE, VOVSCN, VPOS, HSIZE and HSMOD
Horizontal corner correction at top of picture	HCORT	6	04	84	X	#	D5	D4	D3	D2	D1	D0	VSC	+15 to –46% of parabola amplitude	VSIZE, VOVSCN, VPOS, HSIZE and HSMOD
Horizontal corner correction at bottom of picture	HCORB	6	02	82	X	#	D5	D4	D3	D2	D1	D0	VSC	+15 to –46% of parabola amplitude	VSIZE, VOVSCN, VPOS, HSIZE and HSMOD
Horizontal parallelogram	HPARAL	6	09	89	#	#	D5	D4	D3	D2	D1	D0	ACD	±1.2% of horizontal period	VSIZE, VOVSCN and VPOS
EW pin balance	HPINBAL	6	0B	8B	#	#	D5	D4	D3	D2	D1	D0	ACD	±1.2% of horizontal period	VSIZE, VOVSCN and VPOS
Vertical size	VSIZE	7	08	88	#	D6	D5	D4	D3	D2	D1	D0	–	60 to 100%	VSMOD
Vertical position	VPOS	7	0D	8D	X	D6	D5	D4	D3	D2	D1	D0	–	±11.5%	VSMOD
Vertical gain	VGAIN	6	0A	8A	X	#	D5	D4	D3	D2	D1	D0	–	70 to 100%	–
Vertical offset	VOFFS	4	0E	8E	#	#	#	#	D3	D2	D1	D0	–	±4%	–
Vertical linearity	VLIN	4	05	85	D7	D6	D5	D4	#	#	#	#	VSC	–2 to –46%	VSIZE, VOVSCN, VPOS and VSMOD
Vertical linearity balance	VLINBAL	4	05	85	#	#	#	#	D3	D2	D1	D0	–	±1.4% of 100% vertical size	VSIZE, VOVSCN, VPOS and VSMOD

–

FUNCTION	NAME	BITS	SAD1 (HEX)	SAD2 (HEX)	REGISTER ASSIGNMENT								CONTROL BIT	RANGE	FUNCTION TRACKS WITH
					D7	D6	D5	D4	D3	D2	D1	D0			
Moire cancellation via vertical position	VMOIRE	6	00	80	X	X	D5	D4	D3	D2	D1	D0	MOD	0 to 0.08% of vertical amplitude	–
Moire cancellation via horizontal position	HMOIRE	6	06	86	X	X	D5	D4	D3	D2	D1	D0	MOD	0.07% of horizontal period	–
Vertical focus	VFOCUS	4	0E	8E	D7	D6	D5	D4	#	#	#	#	–	0 to 1.1 V	VSIZE, VOVSCN and VPOS
Horizontal focus	HFOCUS	5	0C	8C	#	#	X	D4	D3	D2	D1	D0	–	0 to 3.3 V	–
Horizontal focus pre-correction	HFOCAD	2	0C	8C	D7	D6	X	#	#	#	#	#	–	300 to 450 ns	–

Notes

1. X = don’t care.
2. # = this bit is occupied by another function. If the register is addressed, the bit values for both functions must be transferred.



(1) See Fig.19.

Fig.18 I^2C-bus flow for start-up.

Start-up procedure

V_{CC} < 8.3 V:

- As long as the supply voltage is too low for correct operation, the IC will give no acknowledge due to internal Power-on reset (POR)
- Supply current is 9 mA or less.

V_{CC} > 8.3 V:

- The internal POR has ended and the IC is in standby mode
- Control bits STDBY and SOFTST are reset to their start values
- All other register contents are random
- Pin HUNLOCK is at HIGH-level.

Setting control bit STDBY = 0:

- Enables internal power supply
- Supply current increases from 9 to 70 mA
- When V_{CC} < 8.6 V register SOFTST cannot be set by the I^2C-bus
- Output stages are disabled, except the vertical output
- Pin HUNLOCK is at HIGH-level.

Setting all registers to defined values:

- Due to the hardware configuration of the IC (no auto-increment) any register setting needs a complete 3-byte I^2C-bus data transfer as follows: START - IC address - subaddress - data - STOP.

Setting control bit SOFTST = 1:

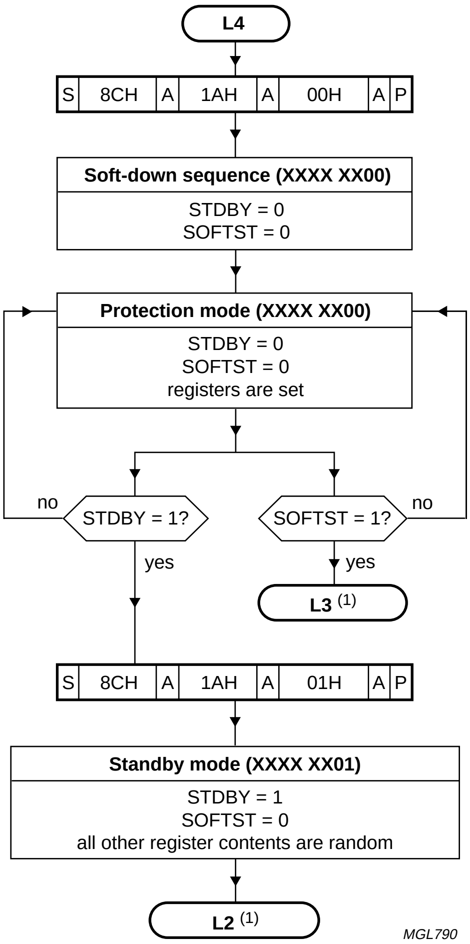
- Before starting the soft-start sequence a delay of minimum 80 ms is necessary to obtain correct function of the horizontal drive
- HDRV duty cycle increases
- BDRV duty cycle increases
- PLL1 and PLL2 are enabled.

IC in full operation:

- Pin HUNLOCK is at LOW-level when PLL1 is locked
- Any change of the register content will result in immediate change of the output behaviour
- Setting control bit SOFTST = 0 is the only way (except power-down via pin V_{CC}) to leave the operating mode.

Soft-down sequence:

- See **L4** of Fig.19 for starting the soft-down sequence.



(1) See Fig.18.

Fig.19 I^2C-bus flow for protection and standby mode.

Protection and standby mode

Soft-down sequence:

- Start the sequence by setting control bit SOFTST = 0
- BDRV duty cycle decreases
- HDRV duty cycle decreases.

Protection mode:

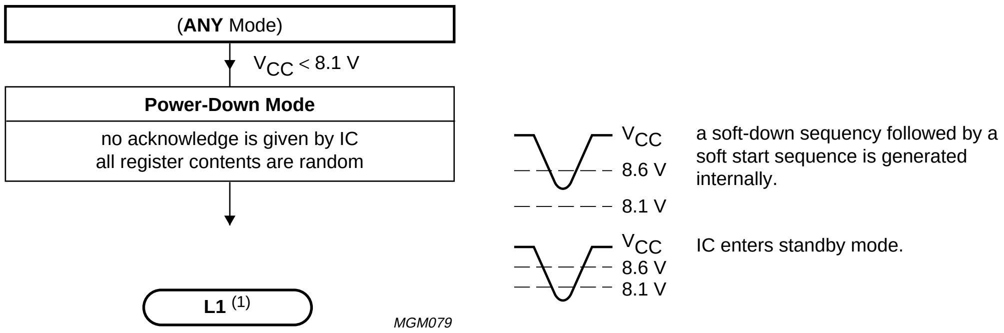
- Pins HDRV and BDRV are floating
- Continuous blanking at pin CLBL is active
- Pin HUNLOCK is floating
- PLL1 and PLL2 are disabled
- Register contents are kept in internal memory.

Protection mode can be left by 3 ways:

1. Entering standby mode by setting control bit SOFTST = 0 and control bit STDBY = 1
2. Starting the soft-start sequence by setting control bit SOFTST = 1 (bit STDBY = don't care); see **L3** of Fig.18 for continuation
3. Decreasing the supply voltage below 8.1 V.

Standby mode:

- Set control bit STDBY = 1
- Driver outputs are floating (same as protection mode)
- Supply current is 9 mA
- Only the I^2C-bus section and protection circuits are operative
- Contents of all registers except the value of bit STDBY and bit SOFTST are lost
- See **L2** of Fig.18 for continuation.



(1) See Fig.18.

Fig.20 I2C-bus flow for any mode.

Power-down mode

Power dip of V_{CC} < 8.6 V:

- The soft-down sequence is started first.
- Then the soft-start sequence is generated internally.

Power dip of V_{CC} < 8.1 V or V_{CC} shut-down:

- This function is independent from the operating mode, so it works under any condition.
- All driver outputs are immediately disabled
- IC enters standby mode.

Standby mode detection

Execute data transmission twice to assure that there was no data transfer error.

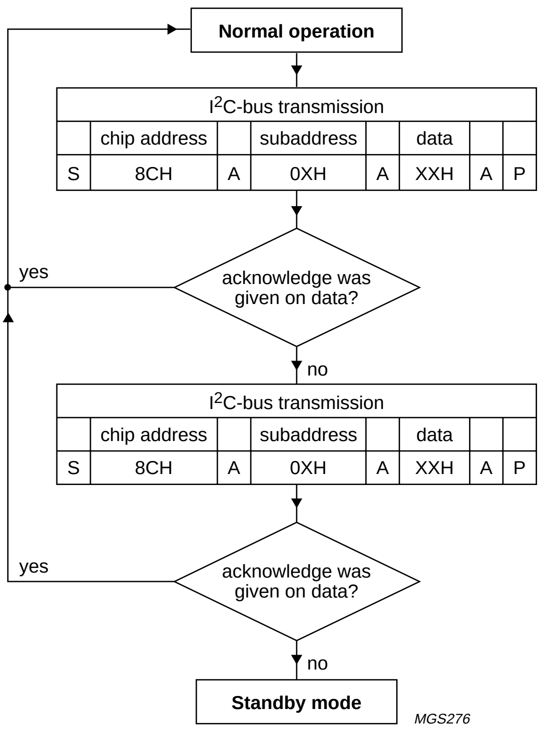
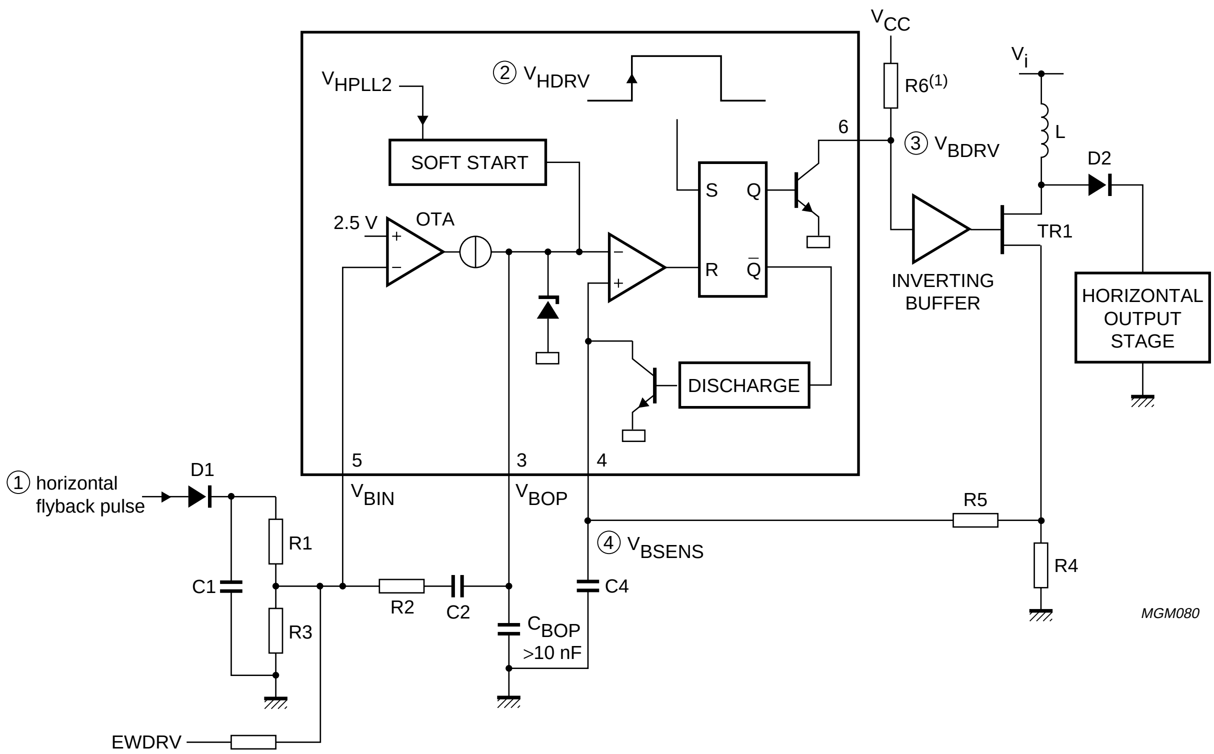


Fig.21 Possible standby mode detection.

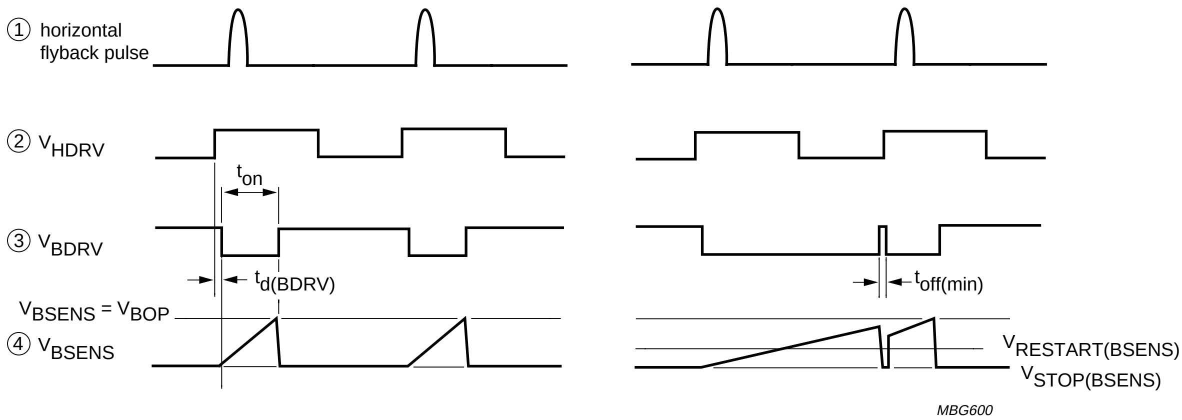
APPLICATION INFORMATION



For f < 50 kHz and C2 < 47 nF calculation formulas and behaviour of the OTA are the same as for an OP. An exception is the limited output current at BOP (pin 3). See Chapter “Characteristics”, Row Head “B+ control section; see Figs 22 and 23”.

(1) The recommended value for R6 is 1 kΩ.

a. Feedback mode application.



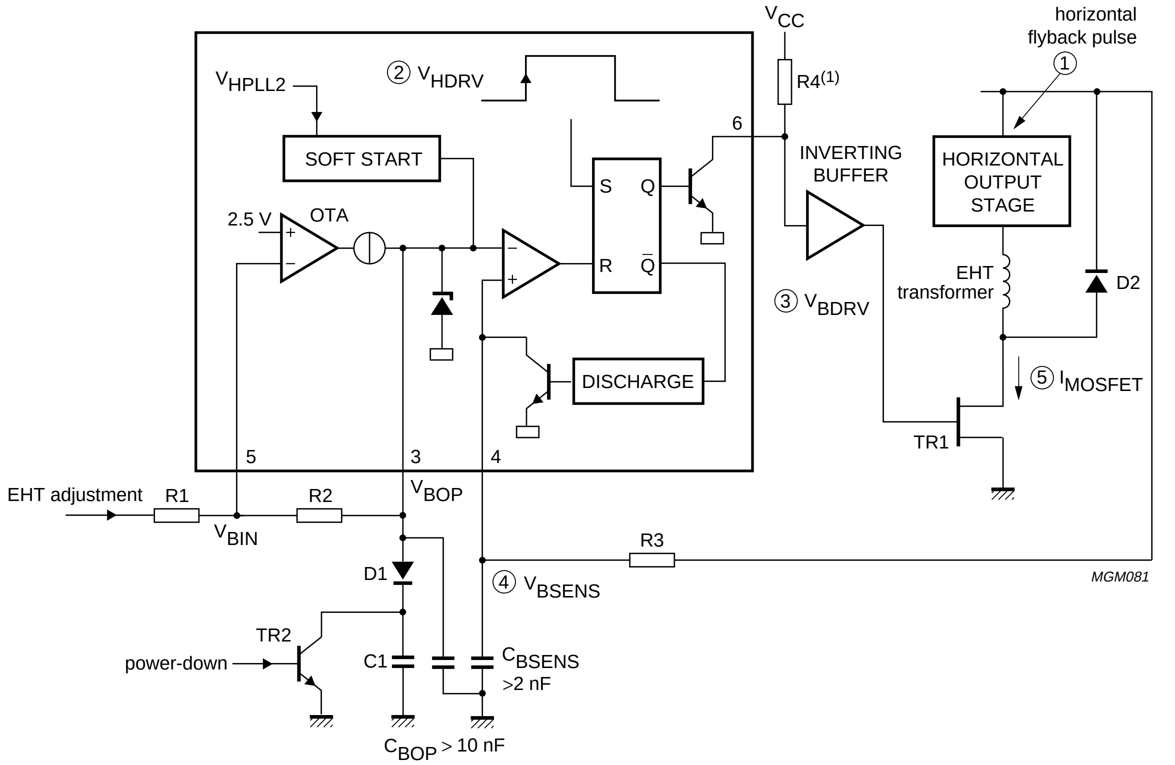
b. Waveforms for normal operation.

c. Waveforms for fault condition.

Fig.22 Application and timing for feedback mode.

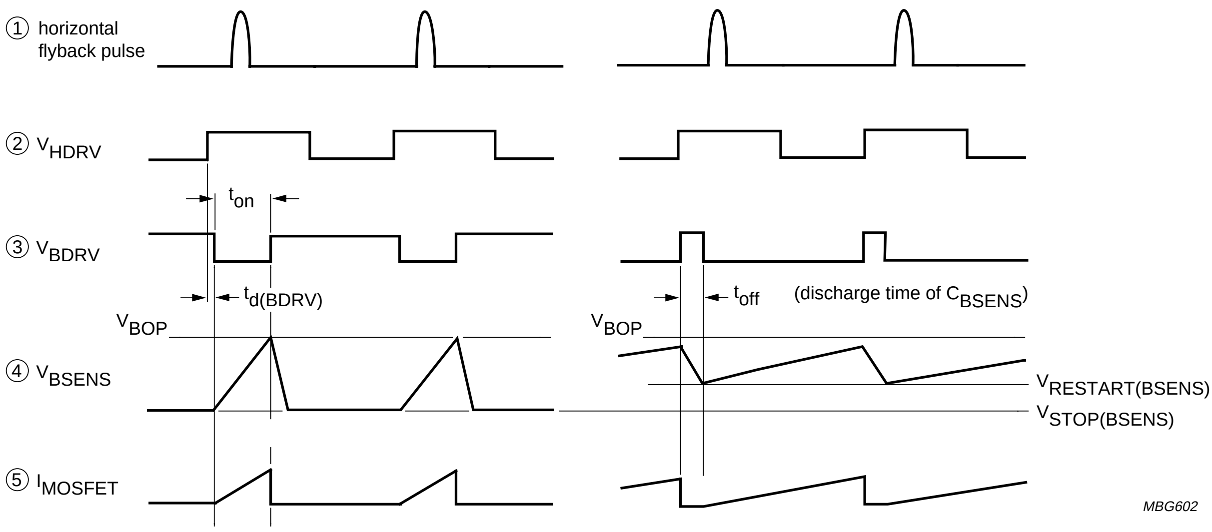
I²C-bus autosync deflection controller for PC monitors

TDA4856



(1) The recommended value for R4 is 1 kΩ.

a. Forward mode application.

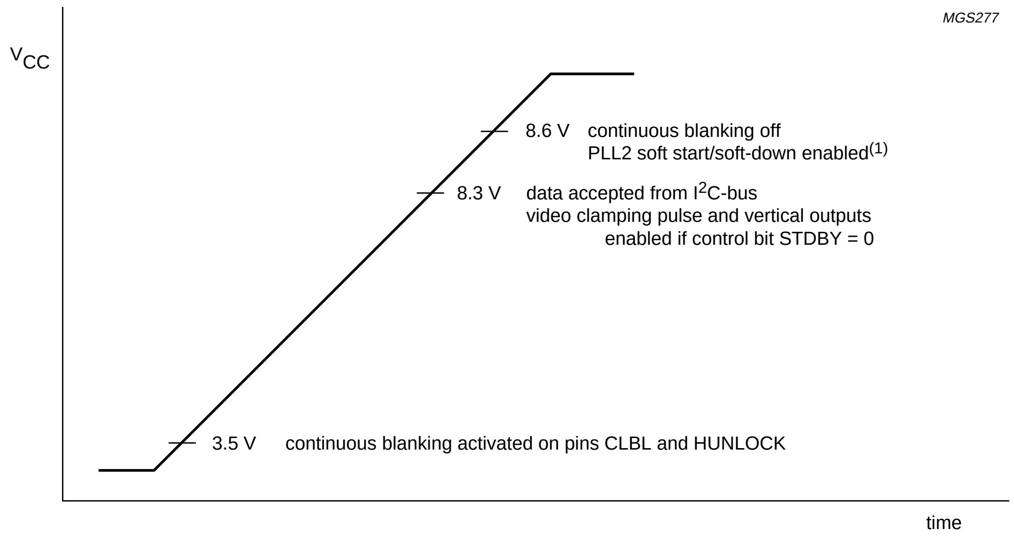


b. Waveforms for normal operation.

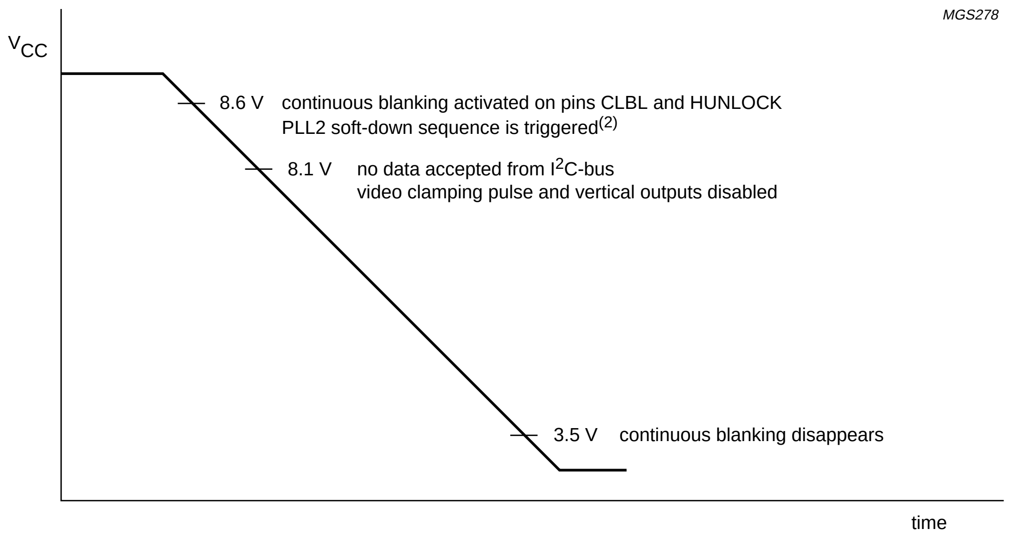
c. Waveforms for fault condition.

Fig.23 Application and timing for feed forward mode.

Start-up sequence and shut-down sequence



a. Start-up sequence.



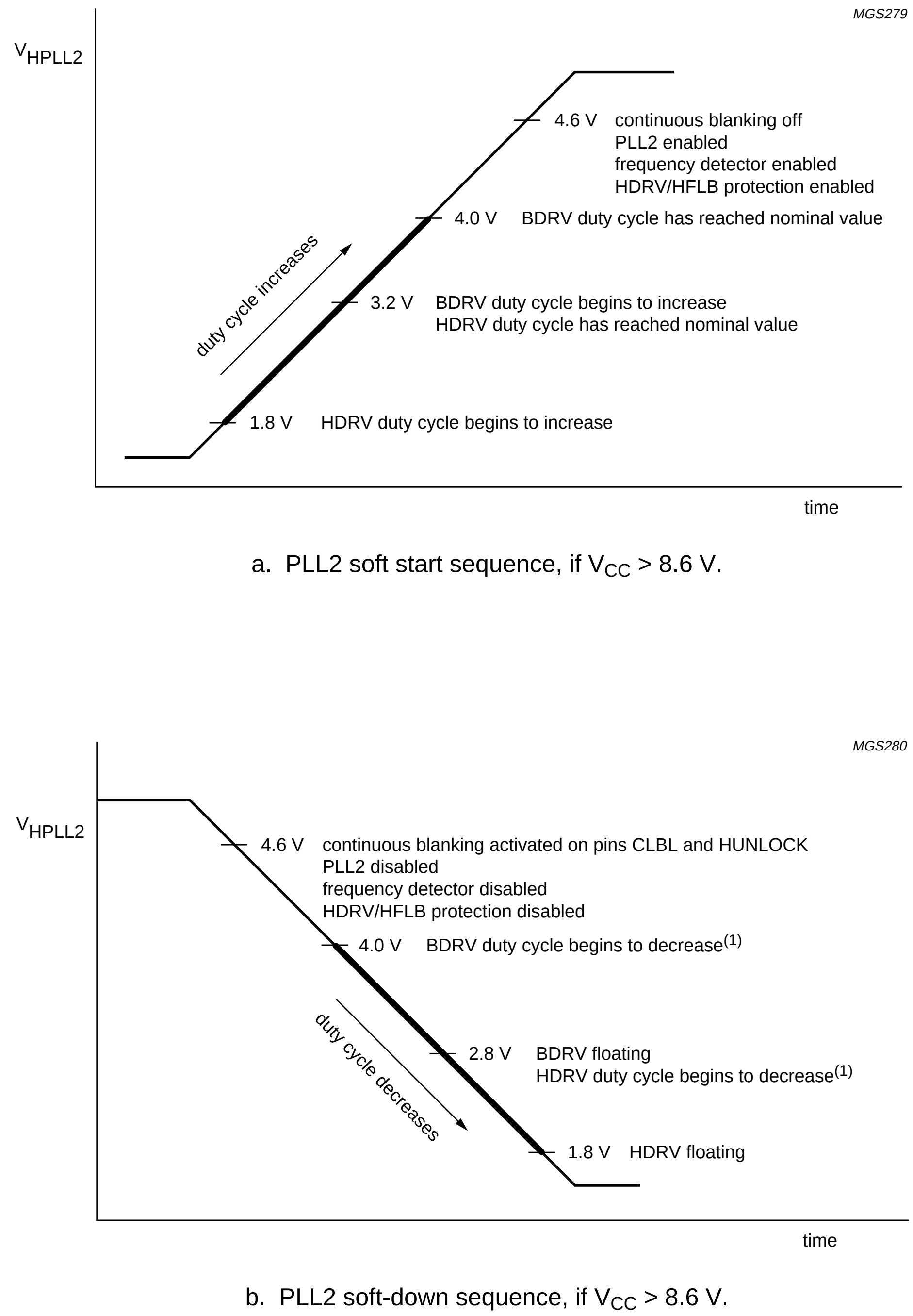
b. Shut-down sequence.

(1) See Fig.25a.

(2) See Fig.25b.

Fig.24 Activation of start-up sequence and shut-down sequence via supply voltage.

PLL2 soft start sequence and PLL2 soft-down sequence



(1) HDRV and BDRV are floating for V_{CC} < 8.6 V.

Fig.25 Activation of PLL2 soft-start sequence and PLL2 soft-down sequence via the I2C-bus.

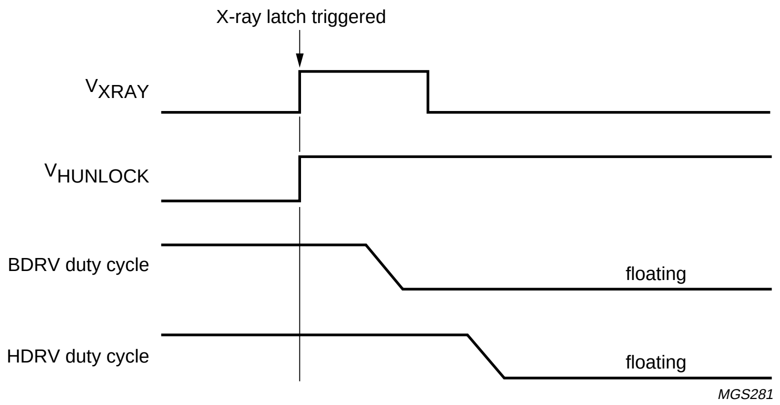
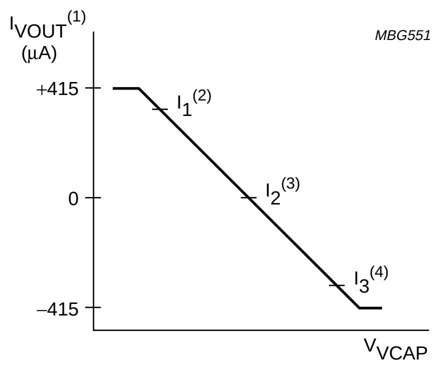


Fig.26 Activation of soft-down sequence via pin XRAY.

Vertical linearity error



(1) $I_{VOUT} = I_{VOUT1} - I_{VOUT2}$.

(2) $I_1 = I_{VOUT}$ at $V_{VCAP} = 1.9$ V.

(3) $I_2 = I_{VOUT}$ at $V_{VCAP} = 2.6$ V.

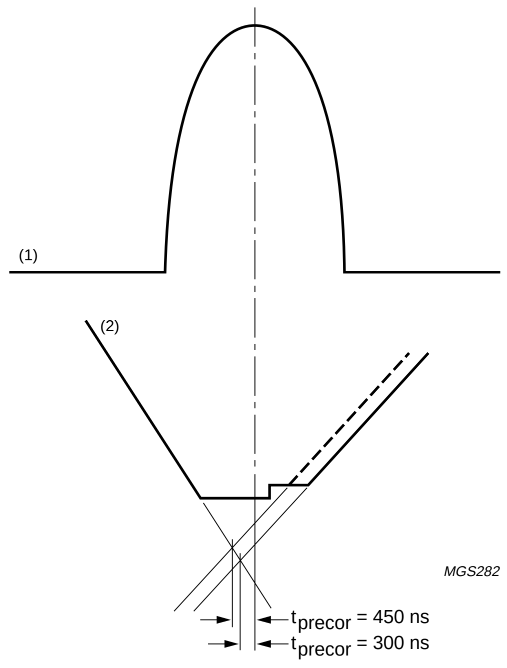
(4) $I_3 = I_{VOUT}$ at $V_{VCAP} = 3.3$ V.

Which means: $I_0 = \frac{I_1 - I_3}{2}$

Vertical linearity error = $1 - \max\left(\frac{I_1 - I_2}{I_0} \text{ or } \frac{I_2 - I_3}{I_0}\right)$

Fig.27 Definition of vertical linearity error.

Horizontal focus pre-correction

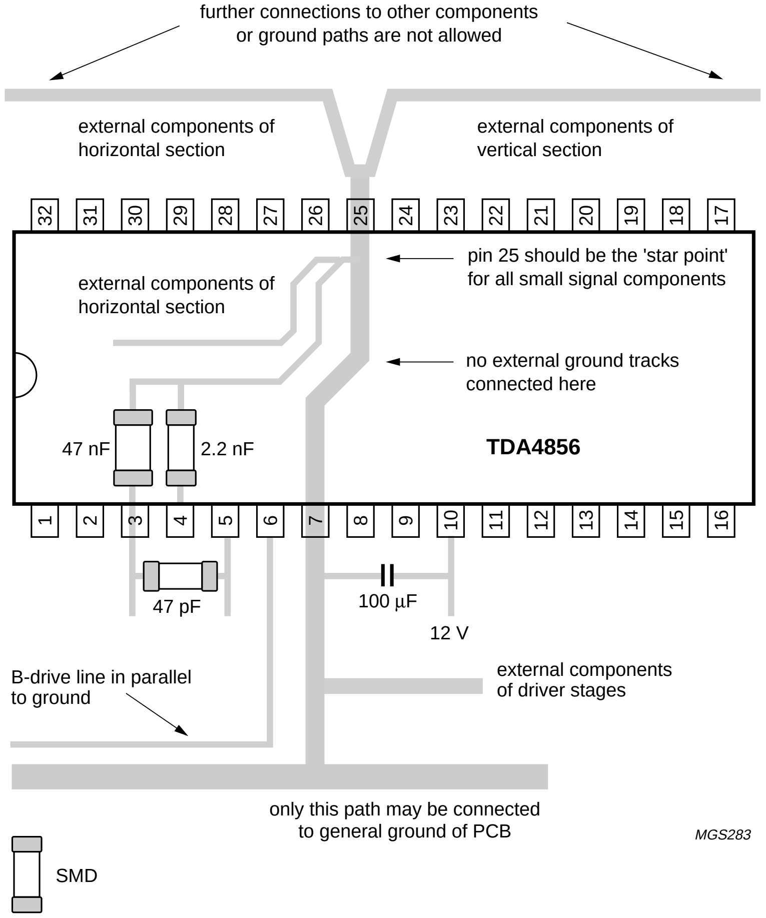


(1) Line flyback pulse at HFLB (pin 1).

(2) Horizontal focus parabola at FOCUS (pin 32).

Fig.28 Definition of horizontal focus pre-correction.

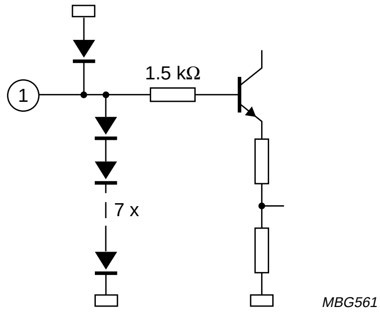
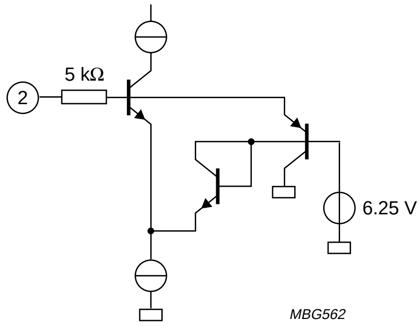
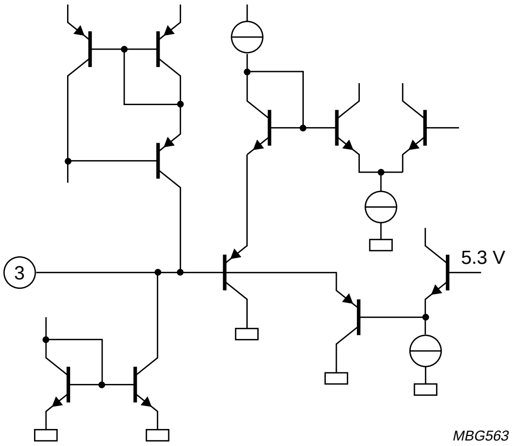
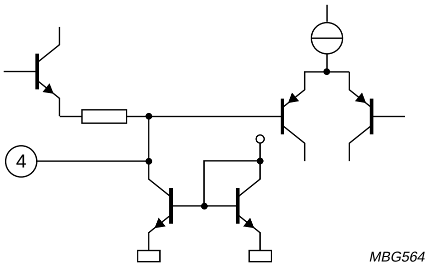
Printed-circuit board layout

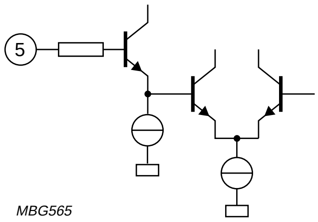
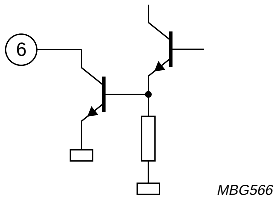
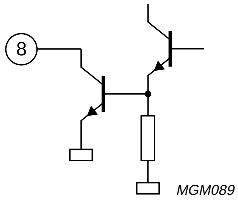
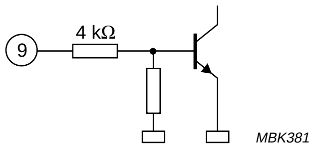
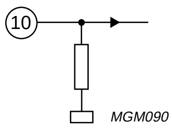
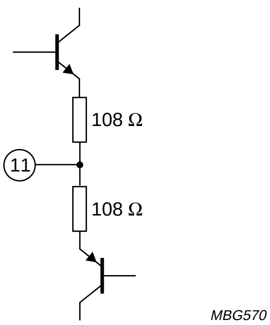


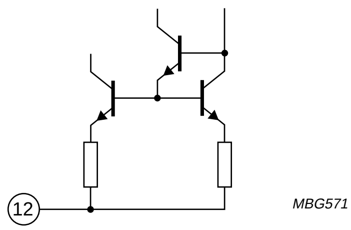
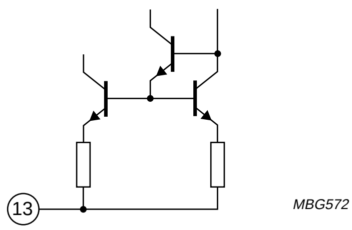
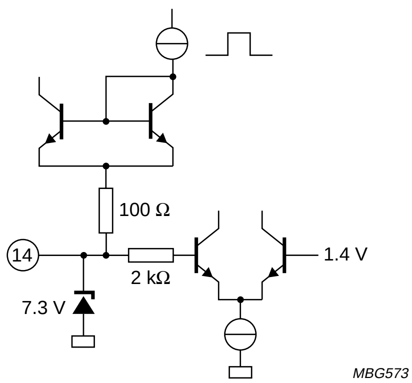
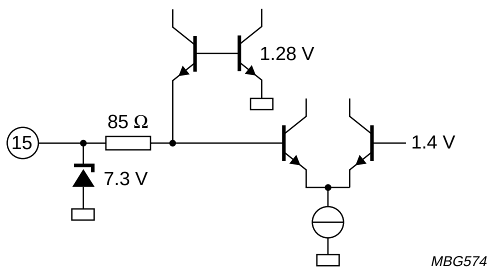
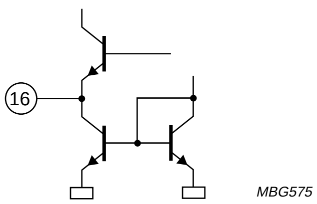
For optimum performance of the TDA4856 the ground paths must be routed as shown.
Only one connection to other grounds on the PCB is allowed.
Note: The tracks for HDRV and BDRV should be kept separate.

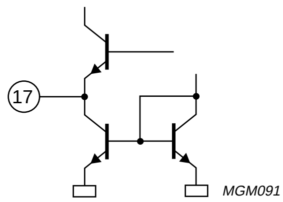
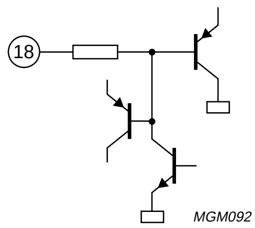
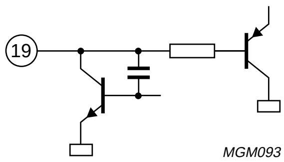
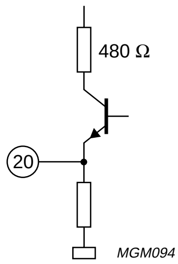
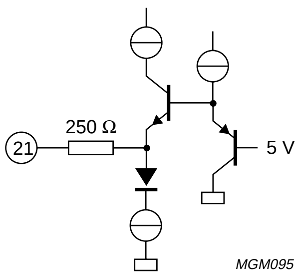
Fig.29 Hints for printed-circuit board (PCB) layout.

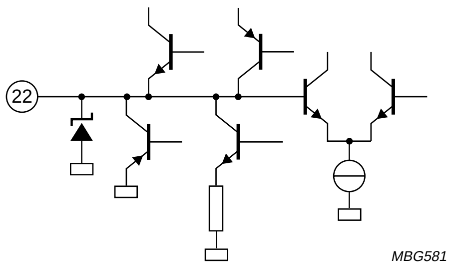
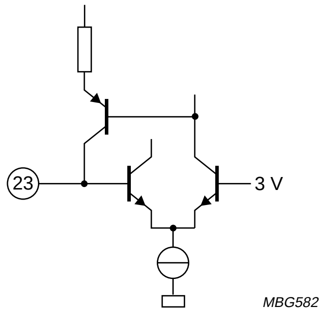
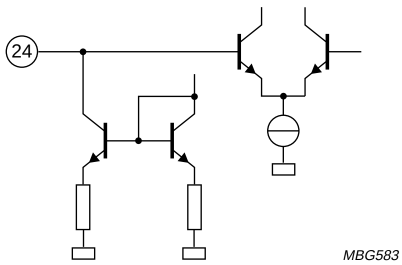
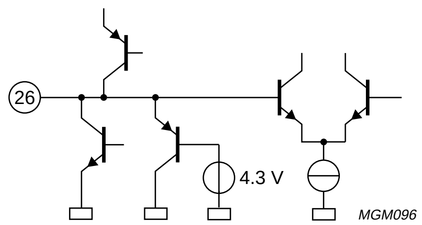
INTERNAL PIN CONFIGURATION

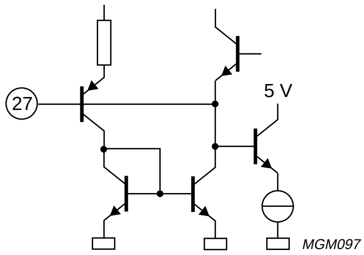
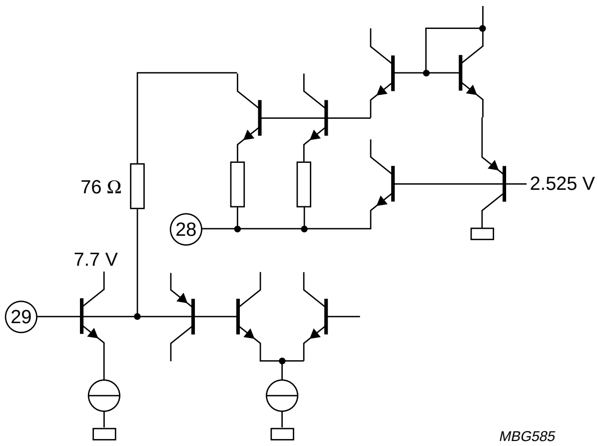
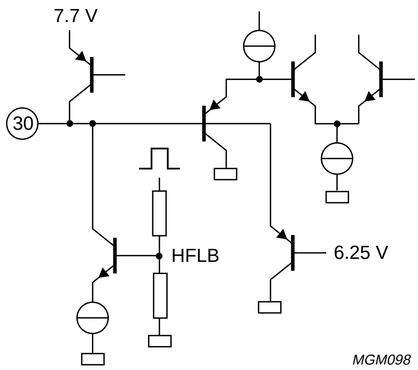
PIN	SYMBOL	INTERNAL CIRCUIT
1	HFLB	
2	XRAY	
3	BOP	
4	BSENS	

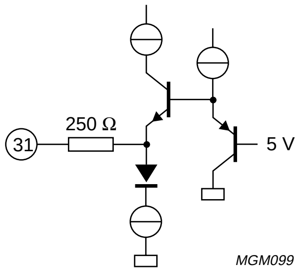
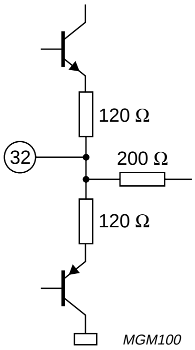
PIN	SYMBOL	INTERNAL CIRCUIT
5	BIN	
6	BDRV	
7	PGND	power ground, connected to substrate
8	HDRV	
9	XSEL	
10	V_{CC}	
11	EWDRV	

PIN	SYMBOL	INTERNAL CIRCUIT
12	VOUT2	
13	VOUT1	
14	VSYNC	
15	HSYNC	
16	CLBL	

PIN	SYMBOL	INTERNAL CIRCUIT
17	HUNLOCK	
18	SCL	
19	SDA	
20	ASCOR	
21	VSMOD	

PIN	SYMBOL	INTERNAL CIRCUIT
22	VAGC	
23	VREF	
24	VCAP	
25	SGND	signal ground
26	HPLL1	

PIN	SYMBOL	INTERNAL CIRCUIT
27	HBUF	
28	HREF	
29	HCAP	
30	HPLL2	

PIN	SYMBOL	INTERNAL CIRCUIT
31	HSMOD	
32	FOCUS	

Electrostatic discharge (ESD) protection

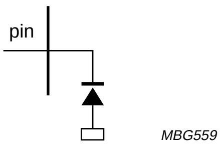


Fig.30 ESD protection for pins 4, 11 to 13, 16 and 17.

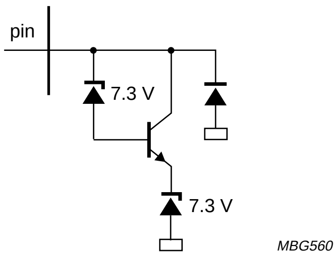
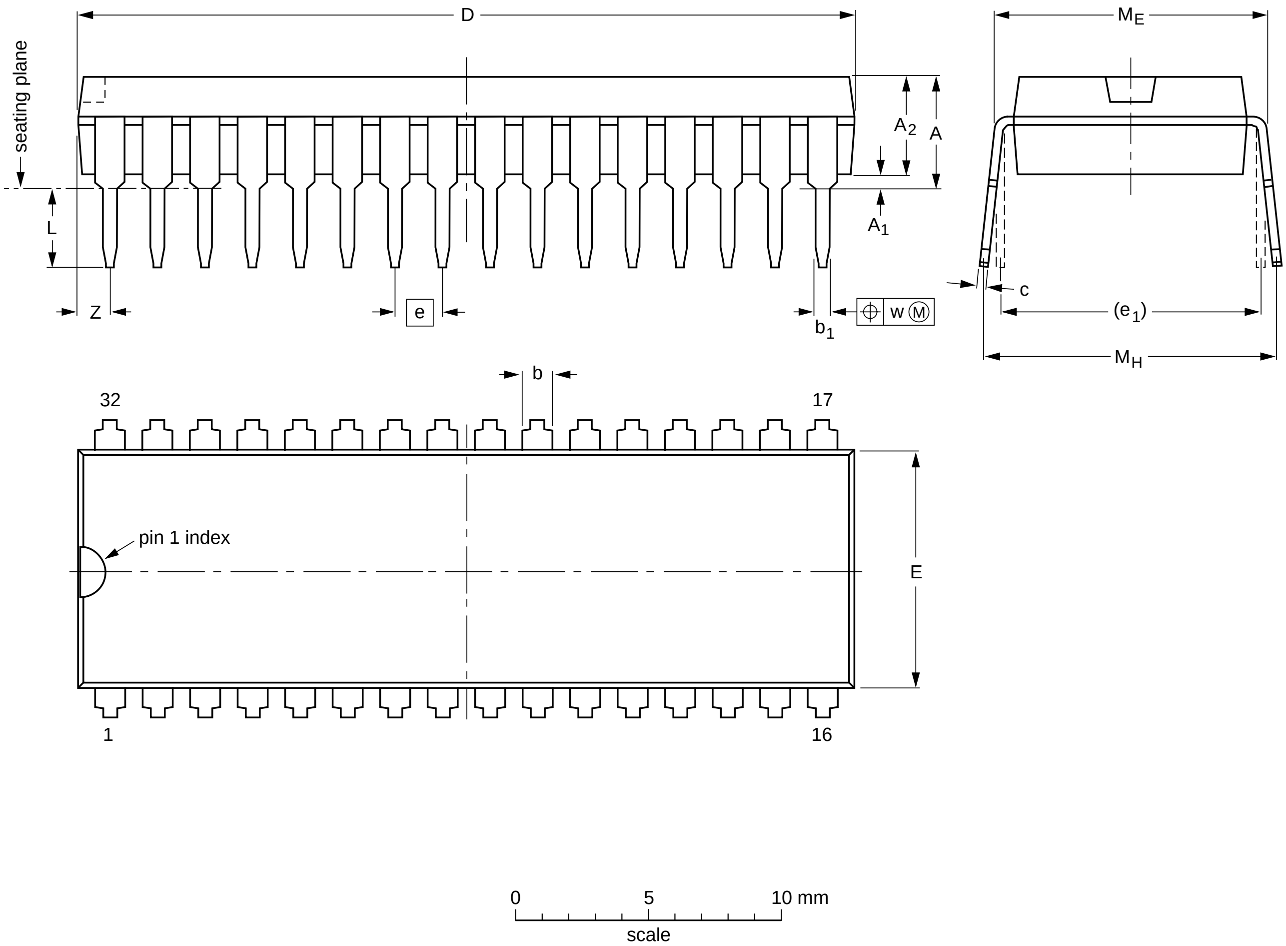


Fig.31 ESD protection for pins 2, 3, 5, 18 to 24 and 26 to 32.

PACKAGE OUTLINE

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil) **SOT232-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	29.4 28.5	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT232-1						~~92-11-17~~ 95-02-04

SOLDERING

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable(1)

Note

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I^{2}C COMPONENTS

Purchase of Philips I^{2}C components conveys a license under the Philips' I^{2}C patent to use the components in the I^{2}C system provided the system conforms to the I^{2}C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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