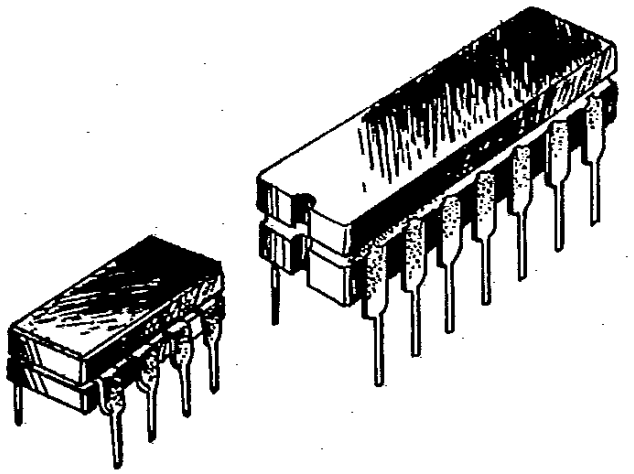
T-79-2

TELEDYNE
SEMICONDUCTOR

TSC76HV52*

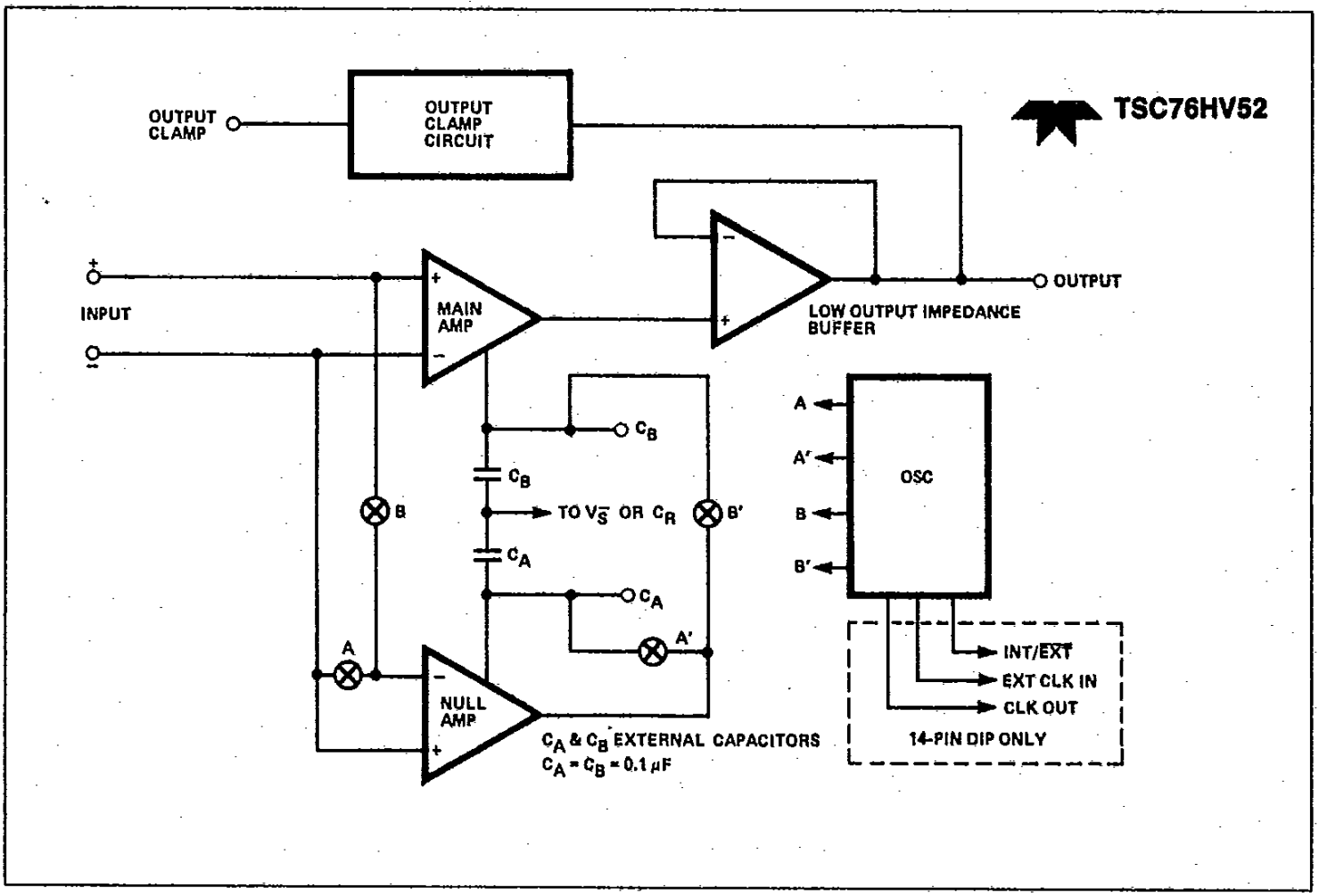
HIGH VOLTAGE, CHOPPER STABILIZED OPERATIONAL AMPLIFIER



FEATURES

- High voltage operation—± 15 V
- Low noise (0 to 1 Hz)—0.2 μV_{p-p}
- Wide common mode voltage—V_S^- to V_S^+ - 2V
- Low supply current—1 mA
- Low offset voltage—10 μV
- Pin compatible to low-voltage 7652
- Low impedance output

FUNCTIONAL DIAGRAM



* Patented—Patent No. 4605907

TSC76HV52

GENERAL DESCRIPTION

The TSC76HV52 brings the benefits of chopper stabilized operational amplifiers to the engineer needing high voltage power supply operation. As a substitute for the 7652, the TSC76HV52 offers reduced power dissipation, wider common mode voltage and greater output current drive capability. Pin compatible with the low voltage 7652, the TSC76HV52 extends power supply operation to ±15 V. Single or dual supply operation is possible.

Optimized for low noise and low power, the TSC76HV52 gives premium electrical performance. Noise (0 to 1 Hz) is a low 0.2 µV p-p. Operating from ±15 V, supply current is only 1.0 mA.

Application versatility is increased over the low-voltage 7652 by extending the input common mode voltage to V_S. Common mode rejection is 120 db. The TSC76HV52 output stage is designed to drive loads typical of bipolar operational amplifiers. Open loop gain is 120 db minimum with a 10KΩ load.

The TSC76HV52 maximum V_{OS} specification is only 10 µV. The maximum V_{OS} drift is only 0.3 µV/°C. Input bias currents of only 100 pA maximum are lower than those for the industry standard OP07E by a factor of 20.

In addition to low initial offset errors, the nulling circuitry ensures excellent performance over time and temperature. Long-term drift, which necessitates periodic system recalibration, is effectively eliminated. The nulling circuitry continues to operate over the full temperature range, whereas laser and zener zap trimming are only done at a single temperature. The result is a significant decrease in temperature-induced errors.

The TSC76HV52 uses two amplfiers to correct offset voltage errors. A main amplifier is always in the signal path, which prevents switching spikes at the output. A separate nulling amplifier alternately corrects its own V_{OS} error and then the main amplifier's V_{OS} errors. Only two external capacitors are required to store the nulling error voltages. All active nulling circuitry, including switches and oscillator, are included on the chip.

The TSC76HV52 is offered in an 8- or 14-pin standard, hermetic Cer DIP package for the same cost as standard ICL7652 plastic devices.

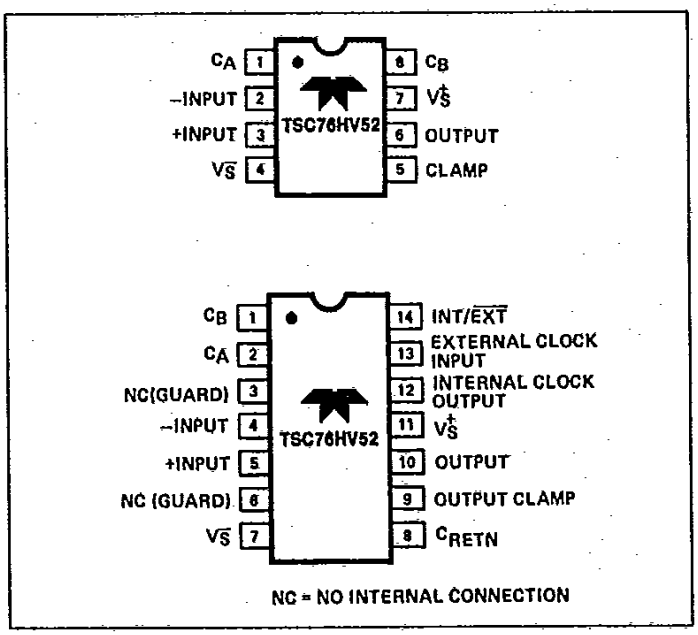
COMPARISON

Parameter	TSC76HV52	ICL7652CPD
Input noise	0.2 µV p-p	0.2 µV p-p
Operating voltage	7 to 32 V	5 to 16 V
Max supply current	1.5 mA	3.5 mA
Negative common mode voltage	V_S	V_S + 0.7 V
Single supp operation	Yes	No
Operating temperature	-25 to +85°C	0 to 70°C
Hermetic package	Yes	No

Ordering Information

Part No.	Package	Temp. Range
TSC76HV52CPA	8-pin Plastic DIP	0°C to 70°C
TSC76HV52IJA	8-pin CerDIP	-25°C to 85°C
TSC76HV52CPD	14-pin Plastic DIP	0°C to 70°C
TSC76HV52IJD	14-pin CerDIP	-25°C to 85°C

Pin Configurations



Absolute Maximum Ratings

Total supply voltage (V_S^- to V_S^+)—36 V
Input voltage—(V_S^- + 0.3) to (V_S^+ - 0.3) V
Storage temperature range— -55 to +150°C
Lead temperature (soldering 10 sec)—300°C
Current into any pin—10 mA
Operating temperature range— -25 to +85°C
Package power dissipation (T_A = 25°C)—500 mW

Electrical Characteristics V_S = ±15 V

T_A = 25°C unless otherwise indicated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	T_A=25°C			10	µV
V_{OS}/T	Average temperature coefficient of input offset voltage	-25°C ≤ T_A ≤ 85°C			0.3	µV/°C
I_B	Average input bias current	T_A = 25°C -25°C ≤ T_A ≤ 85°C		30	100 10	pA nA
I_{OS}	Average input offset current	T_A = 25°C		50	100	pA
en	Input voltage noise	0.1 to 1.0 Hz R_S ≤ 100 Ω		0.2		μV_{P-P}
en	Input voltage noise	0.1 to 10 Hz R_S ≤ 100 Ω		0.8		μV_{P-P}
CMRR	Common-mode rejection ratio	$V_S^- \le V_{CM} \le V_S^+ - 2$ V	120	140		dB
CMVR	Common-mode voltage range		V_S^-		V_S^+-2.0	V
A_{OL}	Open-loop voltage gain	R_L = 10 kΩ V_O = ±10 V	120	140		dB
V_{OUT}	Output voltage swing	R_L = 10 kΩ	V_S^- + 1V		V_S^+ - 1.2V	V
BW	Closed-loop bandwidth	Closed-loop gain = +1		0.5		MHz
SR	Slew rate	R_L = 10 kΩ C_L = 50 pf		0.5		V/µs
PSRR	Power supply rejection rate	V_S = ±5 V to ±15 V	120	140		dB
V_S	Operating supply voltage range	(See note)	±3.5 V		±16 V	V
I_S	Quiescent supply	V_S = ±15 V		1.0	1.5	mA

Note: Single supply operation: V_S = +7 to +32 V.

TSC76HV52

Theory of Operation

Figure 1 shows the major elements of the TSC76HV52. There are two amplifiers: the main (signal) amplifer and the nulling amplifier. Both have offset nulling capability. The main amplifier is always connected to the output. The nulling amplifier alternately samples and adjusts its own offset, and then the offset of the main amplifier.

A two-phase operation nulls the main amplifier. During the first phase the A pair of switches closes, while the B switches open. The nulling amp's inputs are shorted and its output is fed back to the nulling input. Capacitor C_A charges to a voltage which will maintain the nulling amp in its nulled state.

During the second phase the B switches close and the A switches open. The nulling amp's inputs now sample the offset voltage of the main amp. The nulling amp drives the main amp's nulling input to cancel the main amplifier's offset voltage. Capacitor C_B stores the nulling voltage of the main amplifier while the nulling amp is being nulled on the next cycle.

The TSC76HV52 design also incorporates an additional output buffer stage. The buffer provides a low impedance output traditionally associated with bipolar op amps. Some CMOS chopper-stabilized amplifiers such as the 7650 have a high output impedance which makes open-loop gain proportional to load resistance. The TSC76HV52 open-loop gain is not dependent on load resistance.

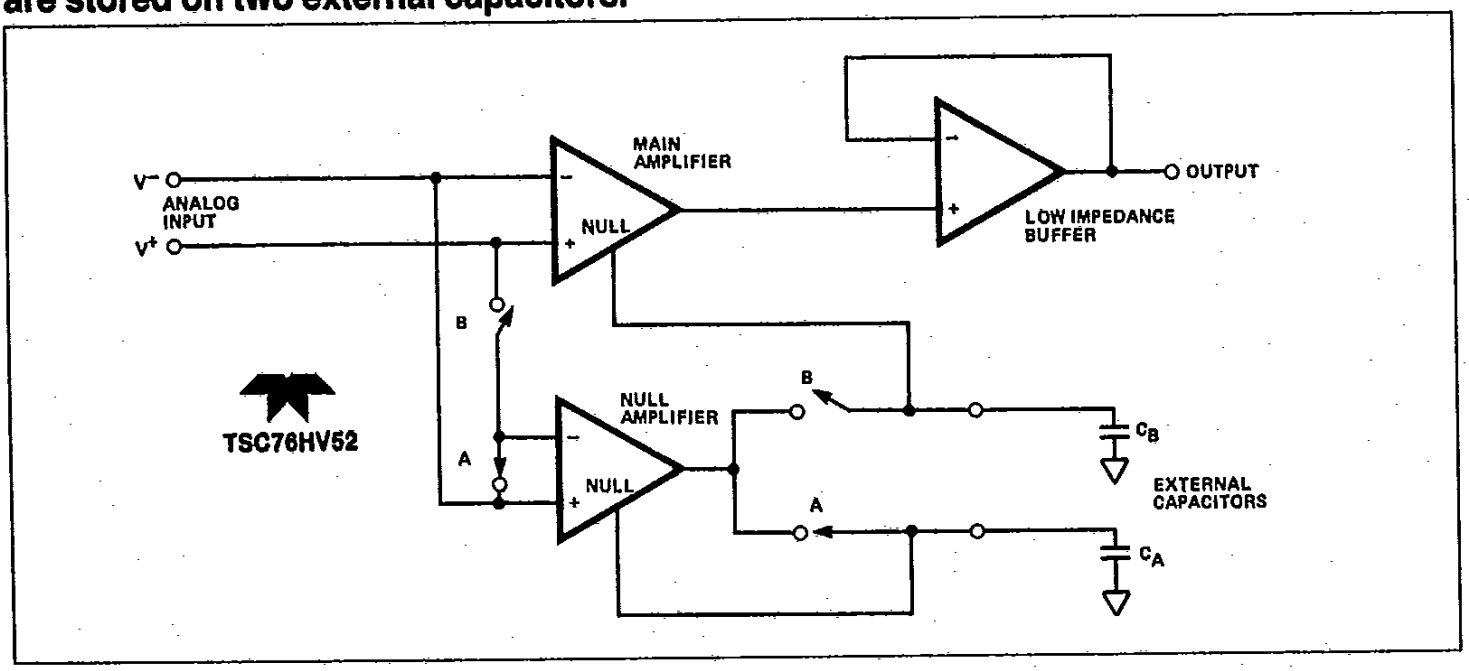
Pin Compatibility

Since the TSC76HV52 operates from the same ±15 V power supplies as bipolar op amps, upgrading existing circuits is simple. The bipolar op amp's nulling and compensation components are removed and the TSC76HV52 nulling capacitors are added.

On the 8-pin mini-DIP TSC76HV52 the external null storagae capacitors are connected to pins 1 and 8. On most other operational amplifiers these are either left open or used for offset potentiometer or compensation capacitor connections.

For OP05 and OP07 operational amplifiers, replacing the offset null pot between pins 1 and 8 with two capacitors from the pins to V_S will convert the OP05/07 pin configuration for TSC76HV52 operation. The 741 is easily upgraded by removing the nulling pot between pin 4 and pins 1 and 5, then conecting capacitors from pin 4 to pins 1 and 8. For LM108 devices the compensation capacitor is replaced by the external nulling capacitors. The LM101/748/749 pinouts are modified similarly by also removing any circuit conections to pin 5. On the TSC76HV52 pin 5 is the output clamp connection. Other operational amplifiers may use this pin as an offset or compenation point.

Figure 1: TSC76HV52 contains nulling and main amplifiers. Offset correction voltages are stored on two external capacitors.



The minor modifications needed to retrofit a TSC76HV52 into existing sockets make prototyping and circuit evaluation straightforward.

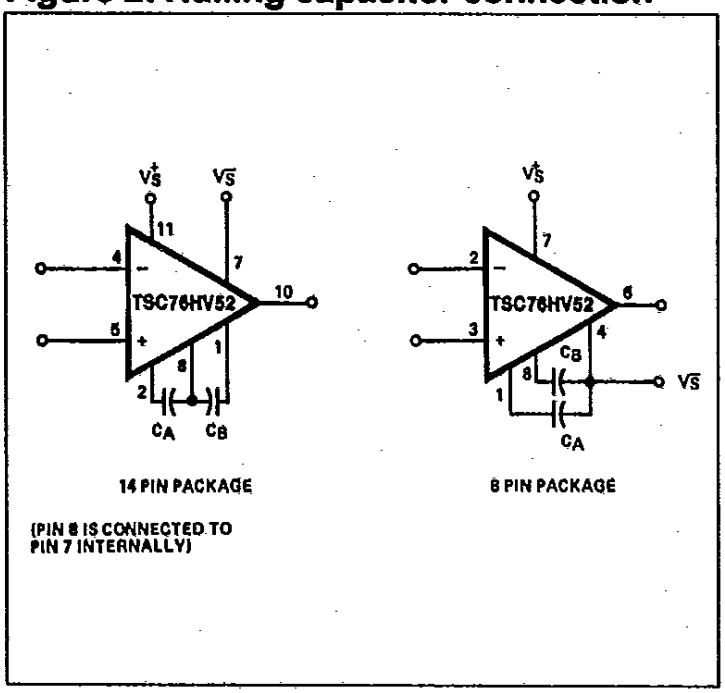
Nulling Capacitors

The offset voltage correction capacitors are conected to C_A and C_B. The common capacitor connection is made to V_S (pin 4) on the 8-pin packages and to capacitor return (C_R, pin 8) on the 14-pin packages. The common connection should be made through either a separate PC trace or wire to avoid voltage drops. Internally, V_S is connected to C_R.

Component Selection

The two required capacitors, C_A and C_B, have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1 µF. To maintain the same relationship between the chopping frequency and the nulling time constant, the capacitor values should be scaled in proportion to the external clock if used. High quality film-type capacitors such as mylar are preferred. Ceramic or other lower-grade capacitors may be suitable in some applications. For fast setting on initial turn-on, low dielectric absorprion capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1 µV. Not recommended are 25 V ceramics.

Figure 2: Nulling capacitor connection



Clock Operation

The internal oscillator is set for a 1,000 Hz nominal frequency on both the 8- and 14-pin dual-in-line packages. With the 14-pin DIP TSC76HV52, the 250 Hz internal chopping frequency is available at the internal clock output (pin 12). A 1,000 Hz nominal signal will be present at the external clock input pin (pin 13) with INT/$\overline{\text{EXT}}$ high or open. This is the internal clock signal before a divide by four operation.

The 14-pin DIP device can be driven by an external clock. The INT/$\overline{\text{EXT}}$ input (pin 14) has an internal pull-up and may be left open for internal clock operation. If an external clock is used, INT/$\overline{\text{EXT}}$ must be tied to V_S (pin 7) to disable the internal clock. The external clock signal is applied to the external clock input (pin 13).

The external clock amplitude should swing between V_S and ground for power supplies up to ±6 V and between V_S and V_S - 6 V for higher supply voltages. When the external clock is generated by + 5 V logic, capacitive coupling to pin 13 (through a 0.1 µF capacitor) provides adequate drive.

At low frequencies the external clock duty cycle is not critical since an internal divide by four gives the desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50 to 80% external clock positive duty cycle is desired for frequencies above 500 Hz to guarantee transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a strobe signal is connected at the external clock input so that it is low during the time an overload signal is applied, neither capacitor wil be charged. This function can be used to prevent input transients from overloading the nulling circuitry. The leakage currents at the capacitor pins are very low, so offset voltage dirft during strobe operation is minimized.

Output Clamp

Chopper-stabilized systems can exhibit long recovery times from overloads. If the output is driven to either supply, output saturation occurs. The inputs are no longer held at virtual ground. The V_{OS} null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, the repsonse time

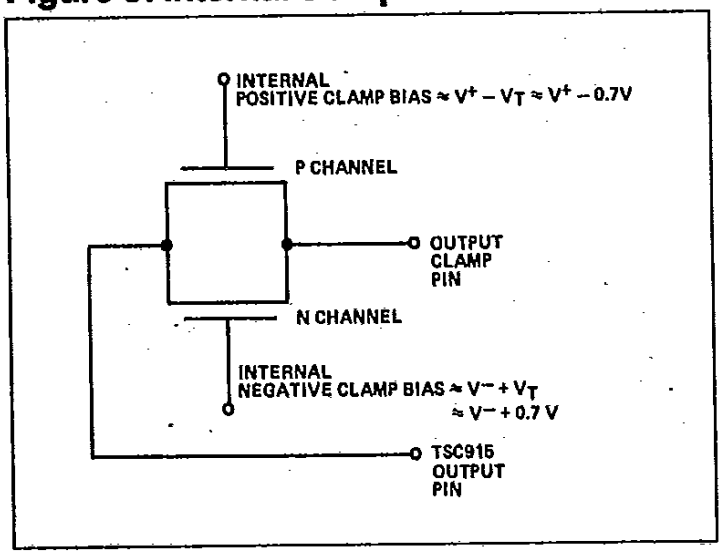
is lengthened by the long recovery time of the nulling amplifier and external capacitors.

Through an external clamp connection, the TSC76HV52 eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

The output clamp circuit is shown in Figure 3 withn typical inverting and non-invertig circuit conections shown in Figures 4 and 5. For the clamp to be fully effective, the impedance across the clamp output should be greater than 100 k Ω.

When the clamp is used, the clamp OFF leakage will add to input bias current. However, clamp leakage in the OFF state is typically only 1 pA.

Figure 3: Internal clamp circuit



Input Bias Current

The TSC76HV52 inputs are never disconnected from the main internal amplifier. The null amplifier samples the input offset voltage and corrects DC errors and drift by storing compensating voltages on external capacitors. The sampling causes, however, charge transfer at the inputs.

The impulse current is not usually a problem because the amount of charge transferred is very small. Care should be exercised, however, when replacing high input bias current bipolar op amps. Conventional design practice is to cancel bias current by matching the input impedances (Figure 6A). the TSC76HV52 has an input bias current of only 100 pA maximum so the additional resistor is not necessary. In fact, including the resistor will make the charge injection current, passing through the impedance balancing resistor, appear as a noise source. When replacing an existing op amp with the TSC76HV52, either omit the resistor or bypass it to ground with a capacitor (Figure 6B).

Figure 4: Non-inverting amplifier with optional clamp

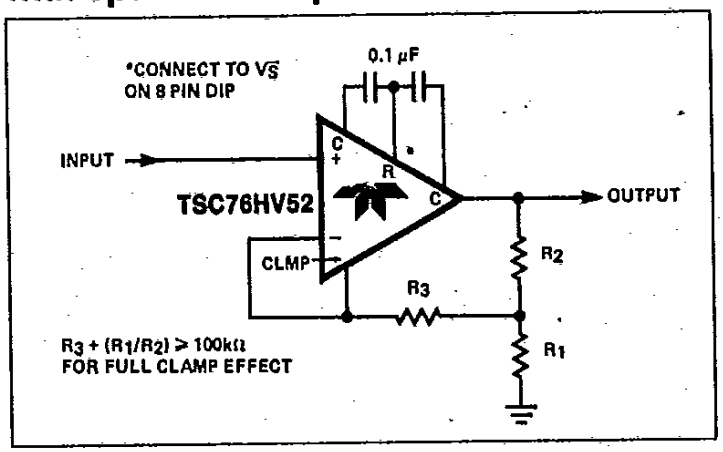


Figure 5: Inverting amplifier with optional clamp

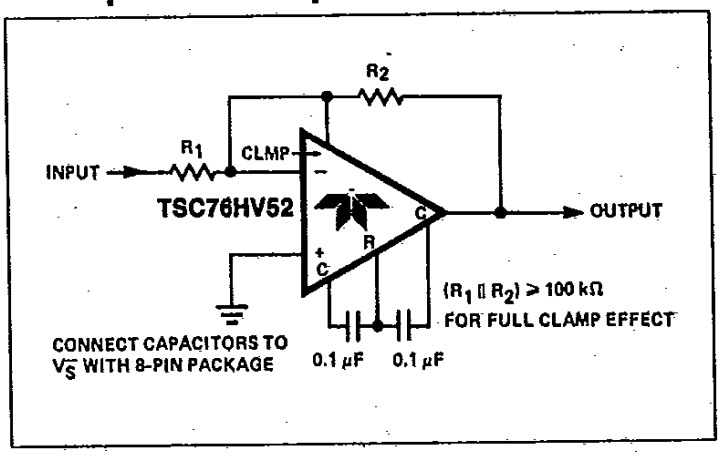
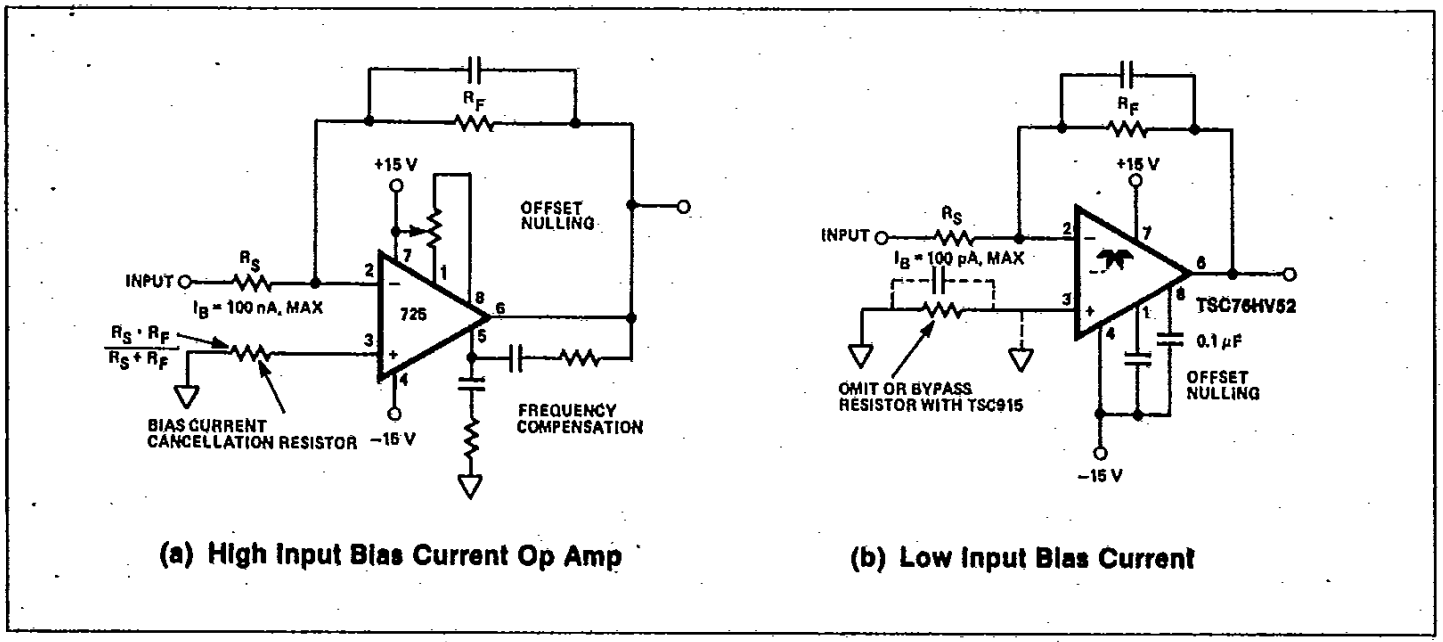
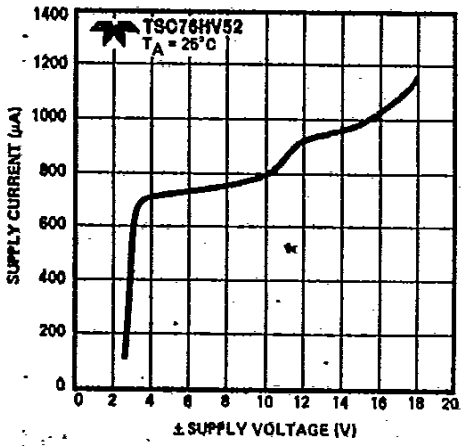


Figure 6: Input bias curve cancellation

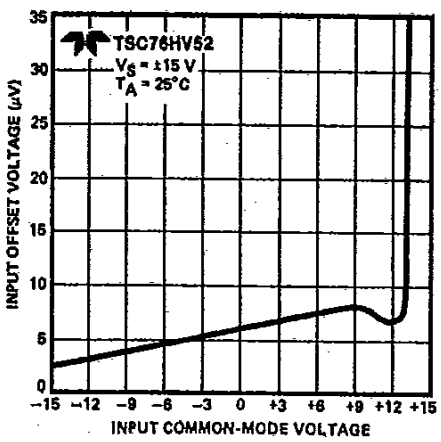


Typical Characteristic Curves

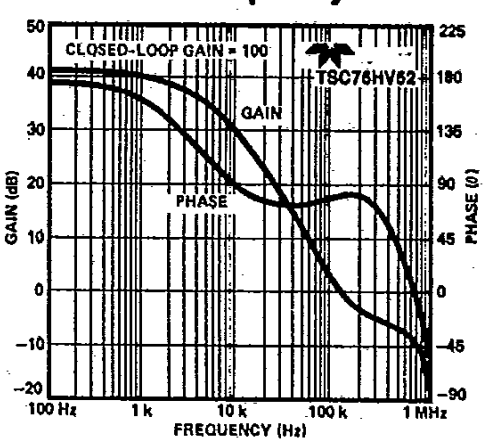
Supply Current vs ± Supply Voltage



Input Offset Voltage vs Common-Mode Voltage



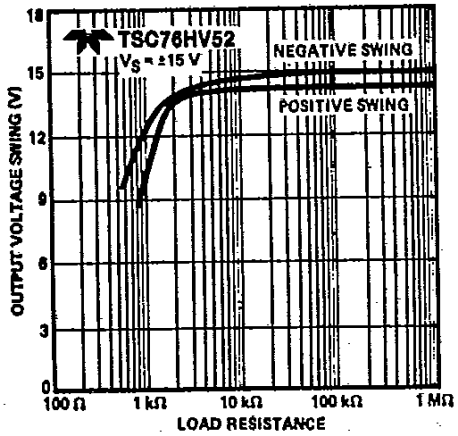
Gain and Phase vs Frequency



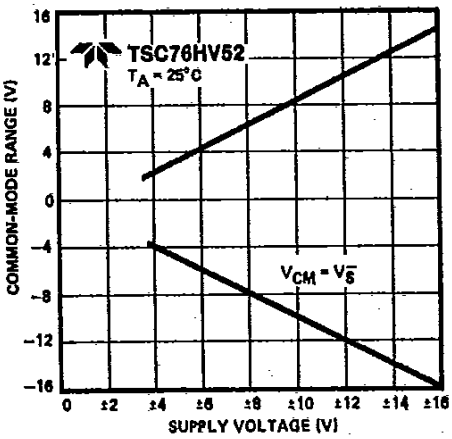
TSC76HV52

Typical Characteristic Curves (continued)

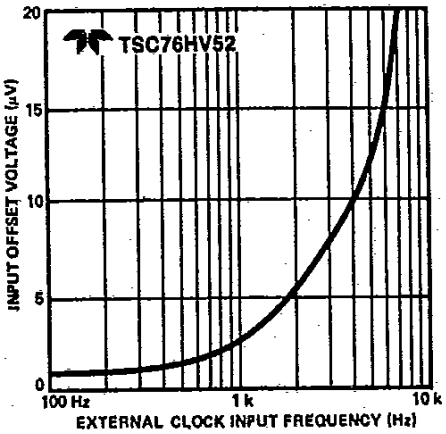
Output Voltage Swing vs Load Resistance



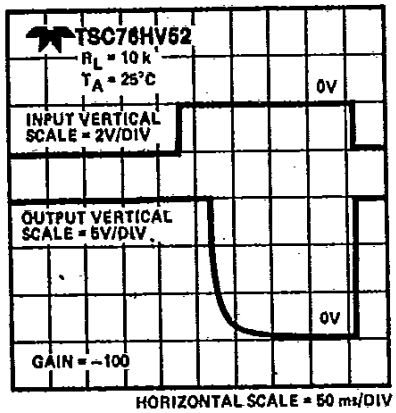
Input Common-Mode Voltage Range vs Supply Voltage



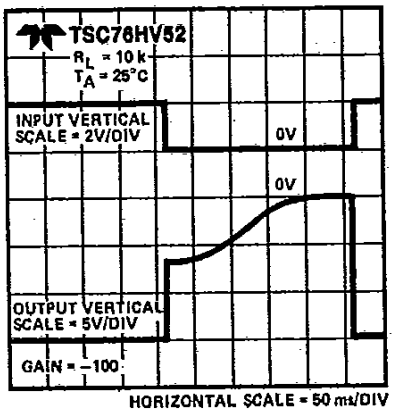
Input Offset Voltage vs Clock Frequency



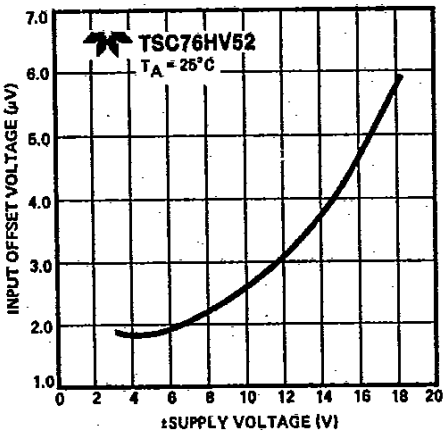
Positive Overload Recovery Time



Negative Overload Recovery Time



Input Offset Voltage vs Supply Voltage



Input Voltage Noise