a

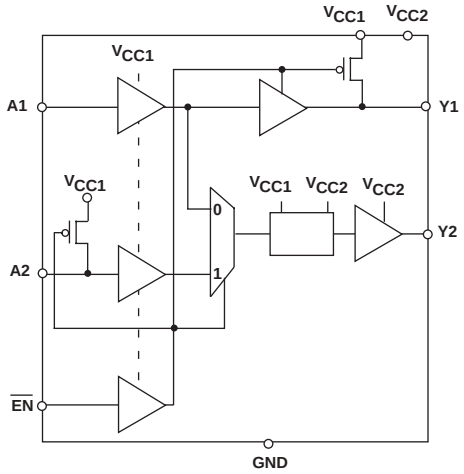
Low Voltage 1.65 V to 3.6 V, (Up/Down) Logic Level Translation, Bypass Switch

Preliminary Technical Data — ADG3233*

FEATURES
Operates from 1.65 V to 3.6 V Supply Rails
Bidirectional Level Translation, Unidirectional Signal Path
8 lead SOT23 and MicroSOIC Packages
Bypass or Normal Operation
Short Circuit Protection*
LVTTL/CMOS-Compatible Inputs

APPLICATIONS
JTAG Chain Bypassing
Daisychain Bypassing
Digital Switching

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG3233 is a bypass switch designed on a sub micron process which operates from supplies as low as 1.65 V. The device is guaranteed for operation over the supply range 1.65 V to 3.6 V. It operates from two supply voltages allowing bi-directional level translation, i.e. it translates low voltages to higher voltages and vice versa. The signal path is uni-directional, data may only flow from A to Y.

This type of device may be used in applications that require a bypassing function. It is ideally suited to bypassing devices in a JTAG chain or bypassing devices in a daisychain loop. One switch could be used for each device or a number of devices thus allowing easy bypassing of one or more devices in a chain. This may be particularly useful in reducing the time overhead in testing devices in the JTAG chain or in daisy chain applications where the user does not wish to change the settings of a particular device.

The Bypass Switch is packaged in two of the smallest footprints available for its required pin count. The 8 lead SOT23 package requires only 8.26mm^2 board space, while the MicroSOIC package occupies approximately 15mm^2 board area.

***Patent Pending**

PRODUCT HIGHLIGHTS

1. Level Translation.
2. The Bypass Switch offers high performance and is fully guaranteed from 1.65 V to 3.6 V supply range.
3. Short Circuit Protection
4. Tiny 8 lead SOT23 package, 8.26mm^2 board area, or 8 lead MicroSOIC.

Table I. Truth Table

E N	Function
L	A1 - Y2, Y1 = Hi-Z Enable Bypass Function
H	A1 - Y1, A2 - Y2 Disable Bypass Function

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ADG3233–SPECIFICATIONS[1]

(V_{CC1} = V_{CC2} = +1.65 to +3.6 V, GND = 0 V, All specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ[2]	Max	Units
LOGIC INPUTS/OUTPUTS[3]		**(V_{CC2} = +1.65 to +3.6 V, GND = 0 V)**				
Input High Voltage	V_{IH}	V_{CC1} = 3.0 V to 3.6 V	1.35			V
		V_{CC1} = 2.3 V to 2.7 V	1.35			V
		V_{CC1} = 1.65 V to 1.95 V	0.65V_{CC}			V
Input Low Voltage	V_{IL}	V_{CC1} = 3.0 V to 3.6 V	-0.5		0.8	V
		V_{CC1} = 2.3 V to 2.7 V	-0.5		0.7	V
		V_{CC1} = 1.65 V to 1.95 V	-0.5		0.35V_{CC}	V
Output High Voltage (Y1)	V_{OH}	I_{OH} = -100 µA, V_{CC1} = 3.0 V to 3.6 V	2.4			V
		V_{CC1} = 2.3 V to 2.7 V	2.0			V
		V_{CC1} = 1.65 V to 1.95 V	V_{CC} - 0.45			V
		I_{OH} = -4 mA, V_{CC1} = 2.3 V to 2.7 V	2.0			V
		V_{CC1} = 1.65 V to 1.95 V	V_{CC} - 0.45			V
		I_{OH} = -8 mA, V_{CC1} = 3.0 V to 3.6 V	2.4			V
Output Low Voltage (Y1)	V_{OL}	I_{OL} = 100 µA, V_{CC1} = 3.0 V to 3.6 V	-0.5		0.4	V
		V_{CC1} = 2.3 V to 2.7 V	-0.5		0.4	V
		V_{CC1} = 1.65 V to 1.95 V	-0.5		0.45	V
		I_{OL} = 4 mA, V_{CC1} = 2.3 V to 2.7 V	-0.5		0.4	V
		V_{CC1} = 1.65 V to 1.95 V	-0.5		0.45	V
		I_{OL} = 8 mA, V_{CC1} = 3.0 V to 3.6 V	-0.5		0.4	V
LOGIC OUTPUTS[3]		**(V_{CC1} = +1.65 to +3.6 V, GND = 0 V)**				
Output High Voltage (Y2)	V_{OH}	I_{OH} = -100 µA, V_{CC2} = 3.0 V to 3.6 V	2.4			V
		V_{CC2} = 2.3 V to 2.7 V	2.0			V
		V_{CC2} = 1.65 V to 1.95 V	V_{CC} - 0.45			V
		I_{OH} = -4 mA, V_{CC2} = 2.3 V to 2.7 V	2.0			V
		V_{CC2} = 1.65 V to 1.95 V	V_{CC} - 0.45			V
		I_{OH} = -8 mA, V_{CC2} = 3.0 V to 3.6 V	2.4			V
Output Low Voltage (Y2)	V_{OL}	I_{OL} = 100 µA, V_{CC2} = 3.0 V to 3.6 V	-0.5		0.4	V
		V_{CC2} = 2.3 V to 2.7 V	-0.5		0.4	V
		V_{CC2} = 1.65 V to 1.95 V	-0.5		0.45	V
		I_{OL} = 4 mA, V_{CC1} = 2.3 V to 2.7 V	-0.5		0.4	V
		V_{CC1} = 1.65 V to 1.95 V	-0.5		0.45	V
		I_{OL} = 8 mA, V_{CC1} = 3.0 V to 3.6 V	-0.5		0.4	V
SWITCHINGS CHARACTERISTICS[4,5]						
V_{CC} = V_{CC1} = V_{CC2} = 3.3V ±0.3 V						
Propagation Delay, t_{PD}						
A1 to Y1	t_{PHL}, t_{PLH}	C_L = 30 pF, V_T = V_{CC}/2			5	ns
A2 to Y2	t_{PHL}, t_{PLH}	C_L = 30 pF, V_T = V_{CC}/2			5	ns
A1 to Y2	t_{PHL}, t_{PLH}	C_L = 30 pF, V_T = V_{CC}/2			5	ns
ENABLE Time *EN* to Y1	t_{EN}	C_L = 30 pF, V_T = V_{CC}/2			5	ns
DISABLE Time *EN* to Y1	t_{DIS}	C_L = 30 pF, V_T = V_{CC}/2			4	ns
ENABLE Time *EN* to Y2	t_{EN}	C_L = 30 pF, V_T = V_{CC}/2			6	ns
DISABLE Time *EN* to Y2	t_{DIS}	C_L = 30 pF, V_T = V_{CC}/2			6	ns
V_{CC} = V_{CC1} = V_{CC2} = 2.5V ±0.2 V						
Propagation Delay, t_{PD}						
A1 to Y1	t_{PHL}, t_{PLH}	C_L = 30 pF, V_T = V_{CC}/2			6	ns
A2 to Y2	t_{PHL}, t_{PLH}	C_L = 30 pF, V_T = V_{CC}/2			6	ns
A1 to Y2	t_{PHL}, t_{PLH}	C_L = 30 pF, V_T = V_{CC}/2			6	ns
ENABLE Time *EN* to Y1	t_{EN}	C_L = 30 pF, V_T = V_{CC}/2			6	ns
DISABLE Time *EN* to Y1	t_{DIS}	C_L = 30 pF, V_T = V_{CC}/2			5	ns
ENABLE Time *EN* to Y2	t_{EN}	C_L = 30 pF, V_T = V_{CC}/2			8	ns
DISABLE Time *EN* to Y2	t_{DIS}	C_L = 30 pF, V_T = V_{CC}/2			7	ns
V_{CC} = V_{CC1} = V_{CC2} = 1.8V ±0.15 V						
Propagation Delay, t_{PD}						
A1 to Y1	t_{PHL}, t_{PLH}	C_L = 30 pF, V_T = V_{CC}/2			10	ns
A2 to Y2	t_{PHL}, t_{PLH}	C_L = 30 pF, V_T = V_{CC}/2			10	ns
A1 to Y2	t_{PHL}, t_{PLH}	C_L = 30 pF, V_T = V_{CC}/2			10	ns
ENABLE Time *EN* to Y1	t_{EN}	C_L = 30 pF, V_T = V_{CC}/2			9	ns
DISABLE Time *EN* to Y1	t_{DIS}	C_L = 30 pF, V_T = V_{CC}/2			7	ns
ENABLE Time *EN* to Y2	t_{EN}	C_L = 30 pF, V_T = V_{CC}/2			12	ns
DISABLE Time *EN* to Y2	t_{DIS}	C_L = 30 pF, V_T = V_{CC}/2			11	ns

SPECIFICATIONS[1]

(V_{CC1} = V_{CC2} = +1.65 V to +3.6 V, GND = 0 V, All specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ[2]	Max	Units
Input Leakage Current	I_I	$0 \le V_{IN} \le 3.6$ V			±1	µA
Output Leakage Current	I_O	$0 \le V_{IN} \le 3.6$ V			±1	µA
Input Capacitance[3]	C_{IN}	f = 1 MHz, V_{IN} = V_{CC} or GND		5		pF
Output Capacitance[3]	C_O	f = 1 MHz, V_{IN} = V_{CC} or GND		5		pF
Max Data Rate				TBD		Mbps
Jitter				TBD		ps
POWER REQUIREMENTS						
Power Supply Voltages	V_{CC1}		1.65		3.6	V
	V_{CC2}		1.65		3.6	V
Quiescent Power Supply Current	I_{CC1}	Digital Inputs = 0 V or V_{CC}			5	µA
	I_{CC2}	Digital Inputs = 0 V or V_{CC}			5	µA
Increase in I_{CC} per input	ΔI_{CC12}	V_{CC} = + 3.6 V, One input at 3.0 V; Others at V_{CC} or GND			100	µA

NOTES

[1]Temperature range is as follows: B Version: –40°C to +85°C.

[2] All typical vlaues are at V_{CC} = V_{CC1} = V_{CC2}, T_A = +25°C unless otherwise stated.

[3] V_{IL} and V_{IH} levels are specified with respect to V_{CC1}, while V_{OH} and V_{OL} levels for Y1 are specfied with respect to V_{CC1} and for Y2 with respect to V_{CC2}

[4] Guaranteed by design, not subject to production test.

[5] See Test Circuits and Waveforms.

Specifications subject to change without notice.

ADG3233

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C unless otherwise noted)

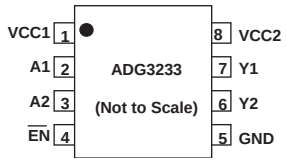
V_{CC} to GND ..... -0.5 V to +4.6 V
Digital Inputs to GND ..... -0.5 V to +4.6 V
DC Input Voltage ..... -0.5 V to +4.6 V
DC Output Current 50mA
Operating Temperature Range
Industrial (B Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... 150°C
8 Lead microSOIC,
θ_{JA} Thermal Impedance ..... 206°C/W
θ_{JC} Thermal Impedance ..... 43°C/W
8 Lead SOT23,
θ_{JA} Thermal Impedance ..... 211°C/W
Lead Temperature, Soldering (10seconds) ..... 300°C
IR Reflow, Peak Temperature (<20 seconds) ....+235°C

NOTES

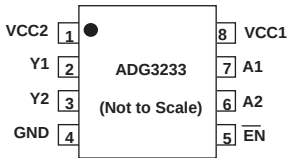
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this speci•cation is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

PIN CONFIGURATIONS

8 Lead SOT23 Package (RJ-8)



8 Lead MicroSOIC Package (RM-8)



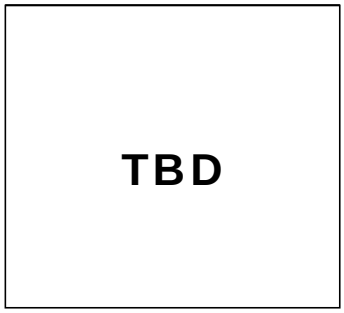
ORDERING GUIDE

Model Option	Temperature Range	Package Description	Branding	Package
ADG3233BRJ	–40°C to +85°C	SOT23	W1B	RJ-8
ADG3233BRM	–40°C to +85°C	MicroSOIC	W1B	RM-8

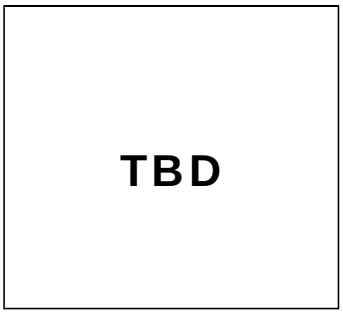
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG3233 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

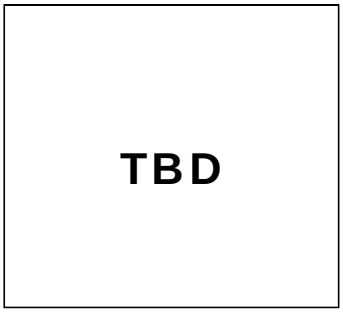
TYPICAL PERFORMANCE CHARACTERISTICS



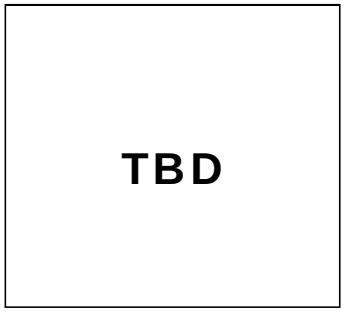
TPC 1. I_{CC} vs. Input Signal Frequency.



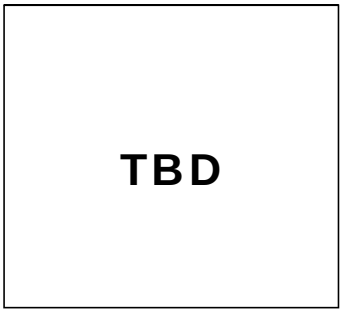
TPC 2. V_{CC} Supply vs temperature



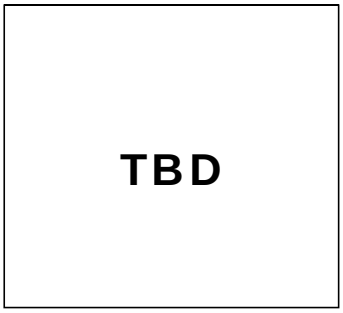
TPC 3. Rise/Fall time vs capacitive load



TPC 4. Propagation Delay vs Temperature



TPC 5. Propagation Delay vs Split Supply.



TPC 6. Propagation delay vs capacitive load

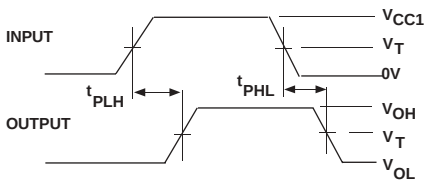


Figure 1. Propagation Delay

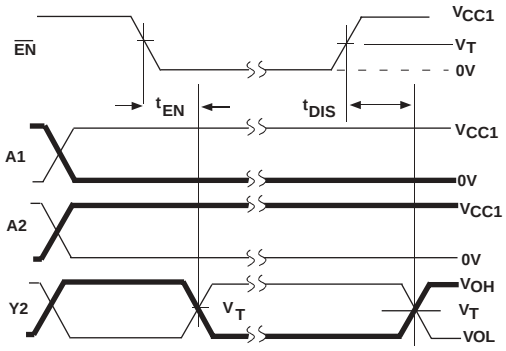


Figure 3. Y2 Enable and Disable Times

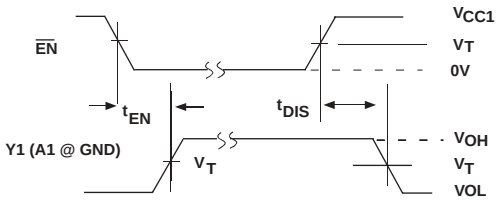


Figure 2. Y1 Enable and Disable Times

DESCRIPTION

The ADG3233 is a bypass switch designed on a sub micron process which operates from supplies as low as 1.65 V. The device is guaranteed for operation over the supply range 1.65 V to 3.6 V. It operates from two supply voltages allowing bi-directional level translation, i.e. it translates low voltages to higher voltages and vice versa. The signal path is uni-directional, data may only flow from A to Y.

A1 & *EN* Input

The A1 and enable (*EN*) inputs have V_{IL}/V_{IH} logic levels so that it can accept logic levels of V_{OL}/V_{OH} from Device 0 or the controlling device independent of the value of the supply being used by the controlling device. These inputs (A1, *EN*) are capable of accepting inputs outside the V_{CC1} supply range. For example, the V_{CC1} supply applied to the Bypass switch could be 1.8V while Device 0 could be operating from a 2.5V or 3.3V supply rail, there are no internal diodes to the supply rails, so the device can handle inputs above the supply, but inside the absolute maximum ratings.

Normal Operation

Figure 4 shows the Bypass switch being used in Normal Mode. In this mode, the signal paths are from A1 to Y1 and A2 to Y2. The device will level translate the signal applied to A1 to a V_{CC1} logic level (this level translation can be either to a higher or lower supply) and route the signal to the Y1 output, which will have standard V_{OL}/V_{OH} levels for V_{CC1} supplies. The signal is then passed through Device 1 and back to the A2 input pin of the bypass switch.

The logic level inputs of A2 are with respect to the V_{CC1} supply. The signal will be level translated from V_{CC1} to V_{CC2} and routed to the Y2 output pin of the bypass switch. Y2 output logic levels are with respect to the V_{CC2} supply.

Bypass Operation

Figure 5 illustrates the device as used in Bypass operation. The signal path is now from A1 directly to Y2, thus bypassing Device 1 completely. The signal will be level translated to a V_{CC2} logic level and available on Y2 where it may be applied directly to the input of Device2. In Bypass mode, Y1 is pulled up to V_{CC1}.

The three supplies in Figures 4 & 5 may be any combination of supplies, i.e. V_{CC0}, V_{CC1} and V_{CC2} may be any combination of supplies, for example: 1.8, 2.5, 3.3V.

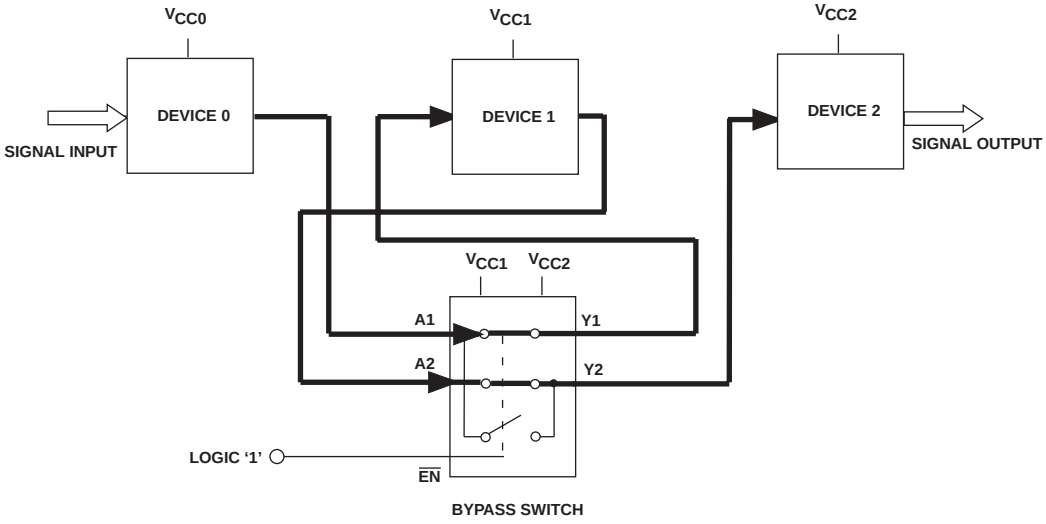


Figure 4. Bypass Switch in Normal Mode

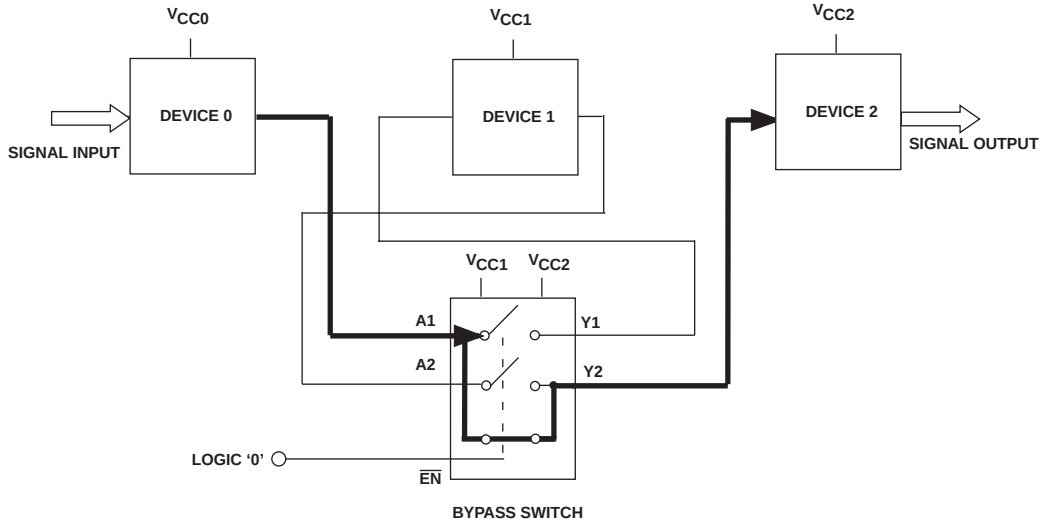
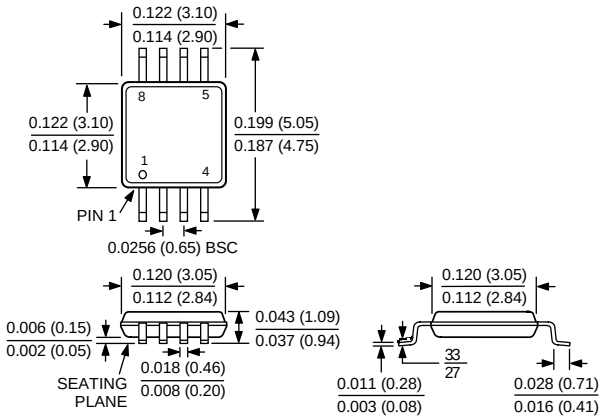


Figure 5. Bypass Switch in Bypass Mode

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead µSOIC
(RM-8)



8-Lead SOT23
(RJ-8)