TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

JBT6K48-AS

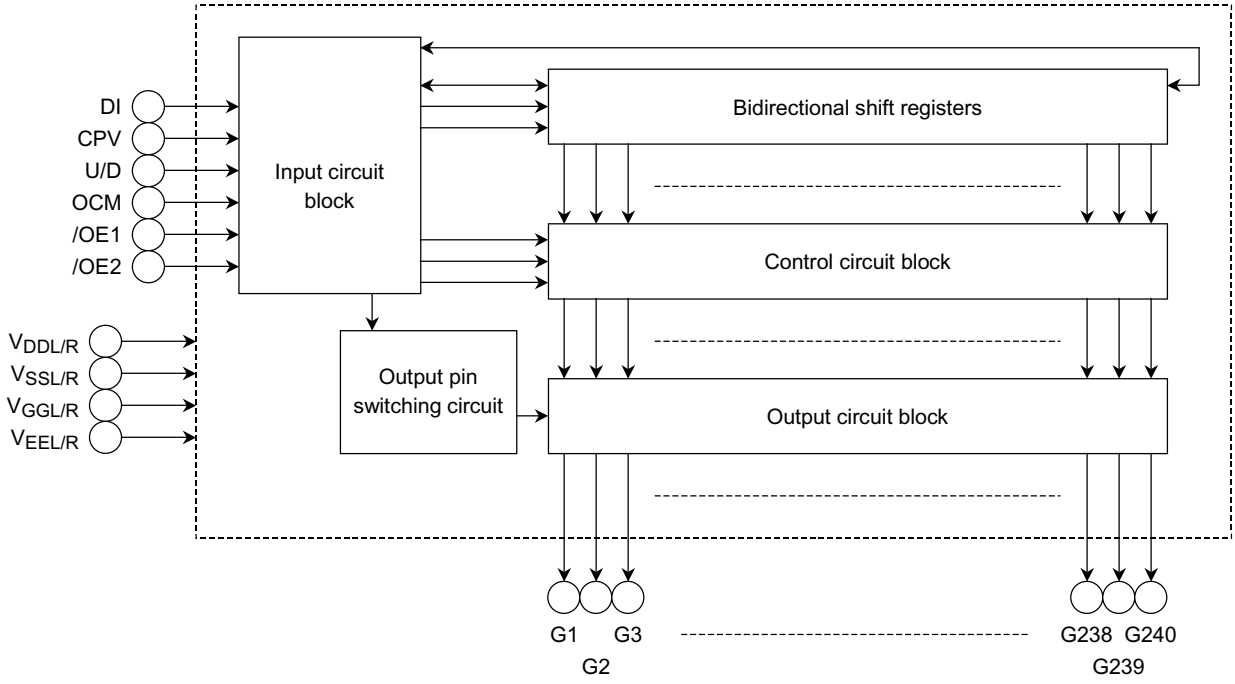
Gate Driver for TFT LCD Panel

The JBT6K48-AS is a 240-channel output gate driver for TFT-LCD. Combining the source driver JBT6K47-AS for TFT-LCD panel and the power supply IC JBT6K49-AS enables low power consumption operation.
Based on high-speed CMOS, the JBT6K48-AS offers both low power consumption and high-speed operation.

Features

- LCD panel drive output pins: Switching 220 pins /240 pins output
- LCD panel drive output voltage: 13.0 to 33.0 V
- Power supply voltage (V_{DD}): 2.5 to 3.6 V
- Data transfer method: Bidirectional shift registers
- Operating temperature: −20 to 75°C
- Package: Gold bump chip
- CMOS process
- Recommended driver: Source driver JBT6K47-AS for TFT-LCD panel
  Power supply IC JBT6K49-AS

Block Diagram



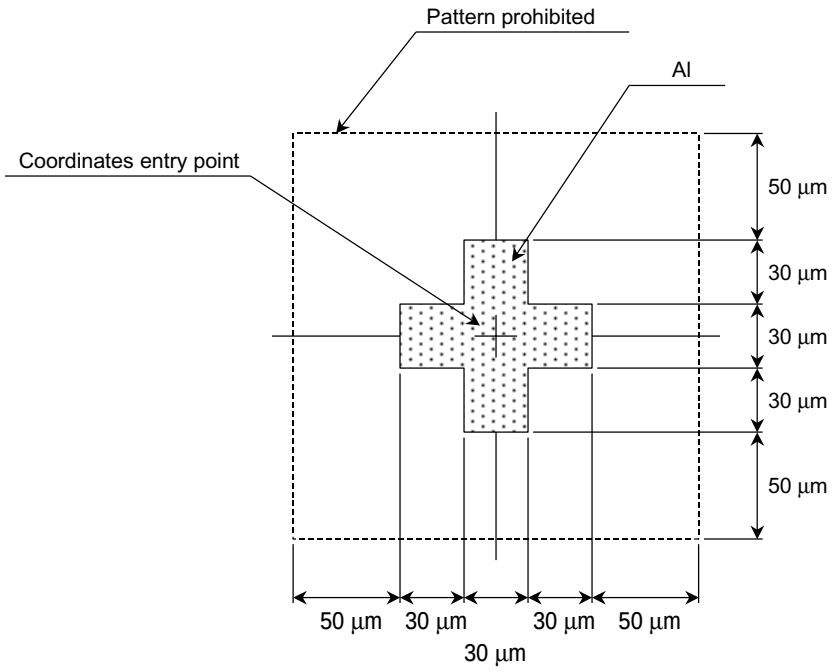
PAD Specification

Item		Size	Unit
Chip size		15470 × 1240	μm
Chip end coordinates	(1)	−7735, 620	μm
	(2)	7735, −620	
	(3)	−7735, −620	
	(4)	7735, 620	
Bump pitch		60	μm
Bump height		15	μm

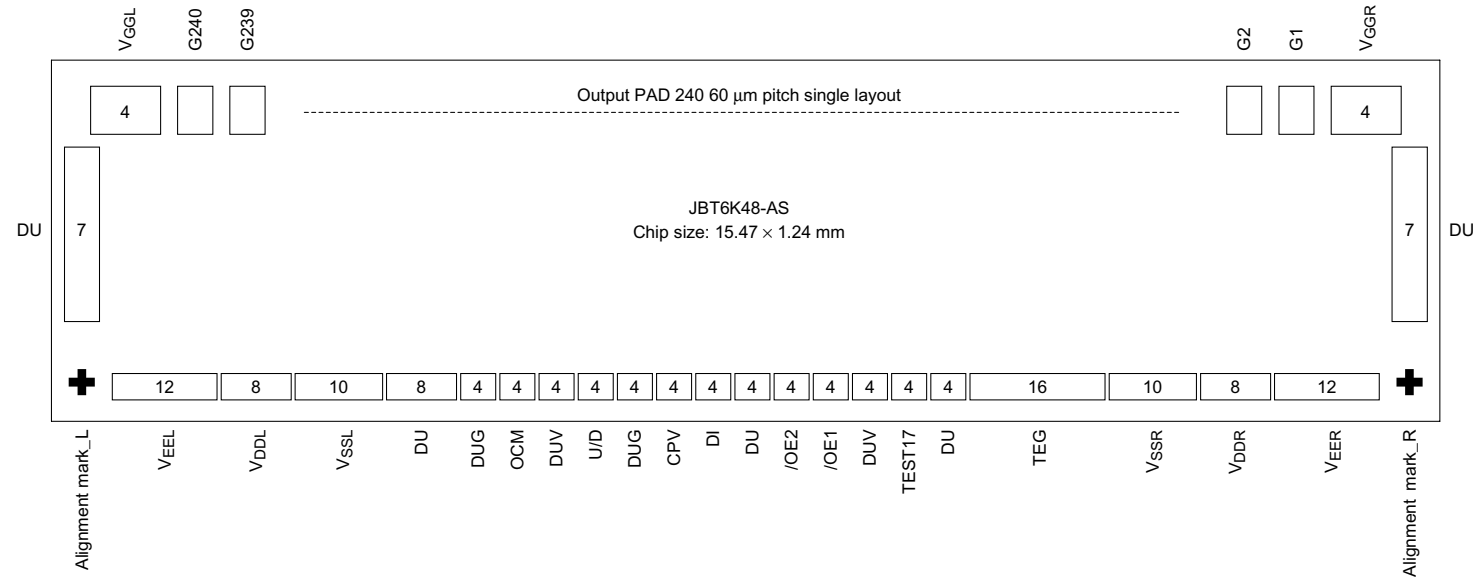
Pin Name	Numbers of Pin
Input pin	96
Output pin	240
TEG pin	16
DUMMY pin	46 (Include DUV, DUG, DU)
Alignment mark	2

Note 1: The TEG pin is a test pin reserved for electrical characteristics measurements, and must be left open.

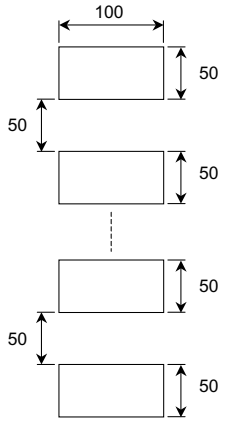
Alignment mark specification



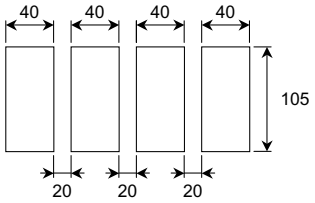
PAD Layout



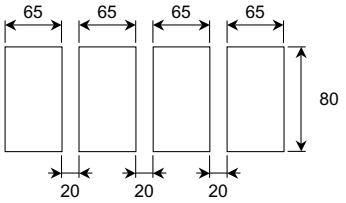
- Short-side dummy PAD (DU)



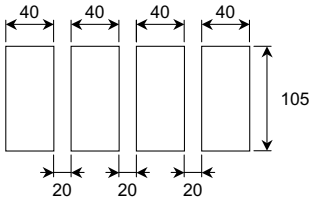
- Long-side power supply PAD ($V_{GGL/R}$)



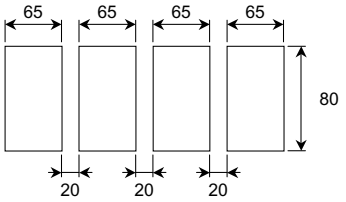
- Long-side input PAD



- Long-side output PAD (G1 to G240)



- Long-side power supply PAD ($V_{EEL/R}$, $V_{DDL/R}$, $V_{SSL/R}$)



[Unit: μm]

PAD Coordinates (1)

[Unit: μm]

No.	Name	X POINT	Y POINT
1	V_{EEL}	−7258	−482
2	V_{EEL}	−7173	−482
3	V_{EEL}	−7088	−482
4	V_{EEL}	−7003	−482
5	V_{EEL}	−6918	−482
6	V_{EEL}	−6833	−482
7	V_{EEL}	−6748	−482
8	V_{EEL}	−6663	−482
9	V_{EEL}	−6578	−482
10	V_{EEL}	−6493	−482
11	V_{EEL}	−6408	−482
12	V_{EEL}	−6323	−482
13	V_{DDL}	−5948	−482
14	V_{DDL}	−5863	−482
15	V_{DDL}	−5778	−482
16	V_{DDL}	−5693	−482
17	V_{DDL}	−5608	−482
18	V_{DDL}	−5523	−482
19	V_{DDL}	−5438	−482
20	V_{DDL}	−5353	−482
21	V_{SSL}	−5108	−482
22	V_{SSL}	−5023	−482
23	V_{SSL}	−4938	−482
24	V_{SSL}	−4853	−482
25	V_{SSL}	−4768	−482
26	V_{SSL}	−4683	−482
27	V_{SSL}	−4598	−482
28	V_{SSL}	−4513	−482
29	V_{SSL}	−4428	−482
30	V_{SSL}	−4343	−482
31	DU	−4098	−482
32	DU	−4013	−482
33	DU	−3928	−482
34	DU	−3843	−482
35	DU	−3758	−482
36	DU	−3673	−482
37	DU	−3588	−482
38	DU	−3503	−482
39	DUG	−3261	−482
40	DUG	−3176	−482
41	DUG	−3091	−482
42	DUG	−3006	−482
43	OCM	−2786	−482
44	OCM	−2701	−482
45	OCM	−2616	−482
46	OCM	−2531	−482
47	DUV	−2311	−482
48	DUV	−2226	−482
49	DUV	−2141	−482
50	DUV	−2056	−482
51	U/D	−1836	−482
52	U/D	−1751	−482
53	U/D	−1666	−482
54	U/D	−1581	−482
55	DUG	−1361	−482
56	DUG	−1276	−482
57	DUG	−1191	−482
58	DUG	−1106	−482
59	CPV	−886	−482
60	CPV	−801	−482
61	CPV	−716	−482
62	CPV	−631	−482
63	DI	−436	−482
64	DI	−351	−482
65	DI	−266	−482
66	DI	−181	−482
67	DU	39	−482
68	DU	124	−482
69	DU	209	−482
70	DU	294	−482
71	/OE2	514	−482
72	/OE2	599	−482
73	/OE2	684	−482
74	/OE2	769	−482
75	/OE1	964	−482
76	/OE1	1049	−482
77	/OE1	1134	−482
78	/OE1	1219	−482
79	DUV	1439	−482
80	DUV	1524	−482
81	DUV	1609	−482
82	DUV	1694	−482
83	TEST17	1914	−482
84	TEST17	1999	−482
85	TEST17	2084	−482
86	TEST17	2169	−482
87	DU	2364	−482
88	DU	2449	−482
89	DU	2534	−482
90	DU	2619	−482
91	TEG1	2848	−482
92	TEG2	2933	−482
93	TEG3	3018	−482
94	TEG4	3103	−482
95	TEG5	3188	−482
96	TEG6	3273	−482
97	TEG7	3358	−482
98	TEG8	3443	−482
99	TEG9	3528	−482
100	TEG10	3613	−482
101	TEG11	3698	−482
102	TEG12	3783	−482
103	TEG13	3868	−482
104	TEG14	3953	−482
105	TEG15	4038	−482
106	TEG16	4123	−482
107	V_{SSR}	4343	−482
108	V_{SSR}	4428	−482
109	V_{SSR}	4513	−482
110	V_{SSR}	4598	−482
111	V_{SSR}	4683	−482
112	V_{SSR}	4768	−482
113	V_{SSR}	4853	−482
114	V_{SSR}	4938	−482
115	V_{SSR}	5023	−482
116	V_{SSR}	5108	−482
117	V_{DDR}	5353	−482
118	V_{DDR}	5438	−482
119	V_{DDR}	5523	−482
120	V_{DDR}	5608	−482
121	V_{DDR}	5693	−482
122	V_{DDR}	5778	−482
123	V_{DDR}	5863	−482
124	V_{DDR}	5948	−482
125	V_{EER}	6323	−482
126	V_{EER}	6408	−482
127	V_{EER}	6493	−482
128	V_{EER}	6578	−482
129	V_{EER}	6663	−482

PAD Coordinates (2)

[Unit: μm]

No.	Name	X POINT	Y POINT
130	V_{EER}	6748	–482
131	V_{EER}	6833	–482
132	V_{EER}	6918	–482
133	V_{EER}	7003	–482
134	V_{EER}	7088	–482
135	V_{EER}	7173	–482
136	V_{EER}	7258	–482
137	DU	7587	–305
138	DU	7587	–205
139	DU	7587	–105
140	DU	7587	–5
141	DU	7587	95
142	DU	7587	195
143	DU	7587	295
144	V_{GGR}	7463	411
145	V_{GGR}	7403	411
146	V_{GGR}	7343	411
147	V_{GGR}	7283	411
148	G1	7170	411
149	G2	7110	411
150	G3	7050	411
151	G4	6990	411
152	G5	6930	411
153	G6	6870	411
154	G7	6810	411
155	G8	6750	411
156	G9	6690	411
157	G10	6630	411
158	G11	6570	411
159	G12	6510	411
160	G13	6450	411
161	G14	6390	411
162	G15	6330	411
163	G16	6270	411
164	G17	6210	411
165	G18	6150	411
166	G19	6090	411
167	G20	6030	411
168	G21	5970	411
169	G22	5910	411
170	G23	5850	411
171	G24	5790	411
172	G25	5730	411

No.	Name	X POINT	Y POINT
173	G26	5670	411
174	G27	5610	411
175	G28	5550	411
176	G29	5490	411
177	G30	5430	411
178	G31	5370	411
179	G32	5310	411
180	G33	5250	411
181	G34	5190	411
182	G35	5130	411
183	G36	5070	411
184	G37	5010	411
185	G38	4950	411
186	G39	4890	411
187	G40	4830	411
188	G41	4770	411
189	G42	4710	411
190	G43	4650	411
191	G44	4590	411
192	G45	4530	411
193	G46	4470	411
194	G47	4410	411
195	G48	4350	411
196	G49	4290	411
197	G50	4230	411
198	G51	4170	411
199	G52	4110	411
200	G53	4050	411
201	G54	3990	411
202	G55	3930	411
203	G56	3870	411
204	G57	3810	411
205	G58	3750	411
206	G59	3690	411
207	G60	3630	411
208	G61	3570	411
209	G62	3510	411
210	G63	3450	411
211	G64	3390	411
212	G65	3330	411
213	G66	3270	411
214	G67	3210	411
215	G68	3150	411

No.	Name	X POINT	Y POINT
216	G69	3090	411
217	G70	3030	411
218	G71	2970	411
219	G72	2910	411
220	G73	2850	411
221	G74	2790	411
222	G75	2730	411
223	G76	2670	411
224	G77	2610	411
225	G78	2550	411
226	G79	2490	411
227	G80	2430	411
228	G81	2370	411
229	G82	2310	411
230	G83	2250	411
231	G84	2190	411
232	G85	2130	411
233	G86	2070	411
234	G87	2010	411
235	G88	1950	411
236	G89	1890	411
237	G90	1830	411
238	G91	1770	411
239	G92	1710	411
240	G93	1650	411
241	G94	1590	411
242	G95	1530	411
243	G96	1470	411
244	G97	1410	411
245	G98	1350	411
246	G99	1290	411
247	G100	1230	411
248	G101	1170	411
249	G102	1110	411
250	G103	1050	411
251	G104	990	411
252	G105	930	411
253	G106	870	411
254	G107	810	411
255	G108	750	411
256	G109	690	411
257	G110	630	411
258	G111	570	411

PAD Coordinates (3)

[Unit: μm]

No.	Name	X POINT	Y POINT
259	G112	510	411
260	G113	450	411
261	G114	390	411
262	G115	330	411
263	G116	270	411
264	G117	210	411
265	G118	150	411
266	G119	90	411
267	G120	30	411
268	G121	−30	411
269	G122	−90	411
270	G123	−150	411
271	G124	−210	411
272	G125	−270	411
273	G126	−330	411
274	G127	−390	411
275	G128	−450	411
276	G129	−510	411
277	G130	−570	411
278	G131	−630	411
279	G132	−690	411
280	G133	−750	411
281	G134	−810	411
282	G135	−870	411
283	G136	−930	411
284	G137	−990	411
285	G138	−1050	411
286	G139	−1110	411
287	G140	−1170	411
288	G141	−1230	411
289	G142	−1290	411
290	G143	−1350	411
291	G144	−1410	411
292	G145	−1470	411
293	G146	−1530	411
294	G147	−1590	411
295	G148	−1650	411
296	G149	−1710	411
297	G150	−1770	411
298	G151	−1830	411
299	G152	−1890	411
300	G153	−1950	411
301	G154	−2010	411
302	G155	−2070	411
303	G156	−2130	411
304	G157	−2190	411
305	G158	−2250	411
306	G159	−2310	411
307	G160	−2370	411
308	G161	−2430	411
309	G162	−2490	411
310	G163	−2550	411
311	G164	−2610	411
312	G165	−2670	411
313	G166	−2730	411
314	G167	−2790	411
315	G168	−2850	411
316	G169	−2910	411
317	G170	−2970	411
318	G171	−3030	411
319	G172	−3090	411
320	G173	−3150	411
321	G174	−3210	411
322	G175	−3270	411
323	G176	−3330	411
324	G177	−3390	411
325	G178	−3450	411
326	G179	−3510	411
327	G180	−3570	411
328	G181	−3630	411
329	G182	−3690	411
330	G183	−3750	411
331	G184	−3810	411
332	G185	−3870	411
333	G186	−3930	411
334	G187	−3990	411
335	G188	−4050	411
336	G189	−4110	411
337	G190	−4170	411
338	G191	−4230	411
339	G192	−4290	411
340	G193	−4350	411
341	G194	−4410	411
342	G195	−4470	411
343	G196	−4530	411
344	G197	−4590	411
345	G198	−4650	411
346	G199	−4710	411
347	G200	−4770	411
348	G201	−4830	411
349	G202	−4890	411
350	G203	−4950	411
351	G204	−5010	411
352	G205	−5070	411
353	G206	−5130	411
354	G207	−5190	411
355	G208	−5250	411
356	G209	−5310	411
357	G210	−5370	411
358	G211	−5430	411
359	G212	−5490	411
360	G213	−5550	411
361	G214	−5610	411
362	G215	−5670	411
363	G216	−5730	411
364	G217	−5790	411
365	G218	−5850	411
366	G219	−5910	411
367	G220	−5970	411
368	G221	−6030	411
369	G222	−6090	411
370	G223	−6150	411
371	G224	−6210	411
372	G225	−6270	411
373	G226	−6330	411
374	G227	−6390	411
375	G228	−6450	411
376	G229	−6510	411
377	G230	−6570	411
378	G231	−6630	411
379	G232	−6690	411
380	G233	−6750	411
381	G234	−6810	411
382	G235	−6870	411
383	G236	−6930	411
384	G237	−6990	411
385	G238	−7050	411
386	G239	−7110	411
387	G240	−7170	411

PAD Coordinates (4) [Unit: μm]

No.	Name	X POINT	Y POINT
388	V_{GGL}	−7283	411
389	V_{GGL}	−7343	411
390	V_{GGL}	−7403	411
391	V_{GGL}	−7463	411
392	DU	−7587	295
393	DU	−7587	195
394	DU	−7587	95
395	DU	−7587	−5
396	DU	−7587	−105
397	DU	−7587	−205
398	DU	−7587	−305
—	Alignment mark_L	−7548	−433
—	Alignment mark_R	7548	−433

Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>U/D</td><td>I</td><td>Data transfer direction switching pin
Specifies the shift direction of the shift registers.
• U/D = H: G1 → G2 → G3 → G4 → G5 → ⋯ → G240
• U/D = L: G240 → G239 → G238 → G237 → ⋯ → G1
Use the pin at DC level. For High, V_{DD}; for Low, V_{SS}.</td></tr>
<tr><td>CPV</td><td>I</td><td>Vertical shift clock
Shift clock for the shift registers. Data are shifted in sync with the rising edge of CPV.</td></tr>
<tr><td>DI</td><td>I</td><td>Vertical shift data input pin
The data is input in the first stage of the shift register and latched in the shift register at the first rising edge of the CPV.</td></tr>
<tr><td>OCM</td><td>I</td><td>Output switching
This pin switches numbers of LCD panel drive pins.
OCM = H: 220 Output mode (G221 to G240 pin output indefinite voltage.)
OCM = L: 240 Output mode</td></tr>
<tr><td>/OE1</td><td>I</td><td>Output mode switching pin (1)
<table><tr><th>Mode</th><th>Output Mode</th></tr><tr><td>H</td><td>Normal mode</td></tr><tr><td>L</td><td>All output off mode (ASYNC)</td></tr></table></td></tr>
<tr><td>/OE2</td><td>I</td><td>Output mode switching pin (2)
<table><tr><th>Mode</th><th>Output Mode</th></tr><tr><td>H</td><td>Normal mode</td></tr><tr><td>L</td><td>All output off mode (sync with CPV)</td></tr></table></td></tr>
<tr><td>G1 to G240</td><td>O</td><td>LCD panel drive pins.</td></tr>
<tr><td>V_{DDL}/V_{DDR}</td><td>—</td><td>Power supply pin for internal logic</td></tr>
<tr><td>V_{SSL}/V_{SSR}</td><td>—</td><td>Power supply pin for internal logic</td></tr>
<tr><td>V_{GGL}/V_{GGR}</td><td>—</td><td>LCD panel drive pins</td></tr>
<tr><td>V_{EEL}/V_{EER}</td><td>—</td><td>LCD panel drive pins</td></tr>
<tr><td>TEST17</td><td>I</td><td>Test pin (1)
The pull down resistor is connected to this pin, and must be left open.</td></tr>
<tr><td>TEG1 to 16</td><td>I</td><td>Test pin (2)
This is a test pin, and must be left open.</td></tr>
<tr><td>DUG
DUV
DU</td><td>—</td><td>Dummy pin
These pins are dummies, and each pin has an electric function such as, V_{DD}, V_{SS} or floating. The details are listed below.
<table><tr><th>Pin Name</th><th>Remarks</th></tr><tr><td>DUG</td><td>DUG … A dummy pin for V_{SS}.</td></tr><tr><td>DUV</td><td>DUV … A dummy pin for V_{DD}.</td></tr><tr><td>DU</td><td>DU … A dummy pin for floating.</td></tr></table>Note 2: The DUG pin and the DUV pin are used to fix the level by the adjacent input pin. Do not use them as the reference power supply.</td></tr>
</table>

Device Function and Operation

- Setting the Data Transferring Direction

  Setting U/D pin enables JBT6K48-AS shift the shift register in sync with the falling edge of the vertical shift clock input from the CPV pin. When the U/D pin data is fixed before the DI data is input, the function becomes valid.

- Inputting Data

  The data is latched at the first falling edge of the CPV. The signal is output from the first falling edge of the CPV recognized the data.

- Switching Numbers of the Output Pin

  The valid output pin can be switched either 220 pins or 240 pins using the COM pin. The details about the valid output pins are listed below.

OCM	Valid output pin	Remarks
0	G1 to G240	
1	G1 to G220	G221 to G240 output indefinite voltage level

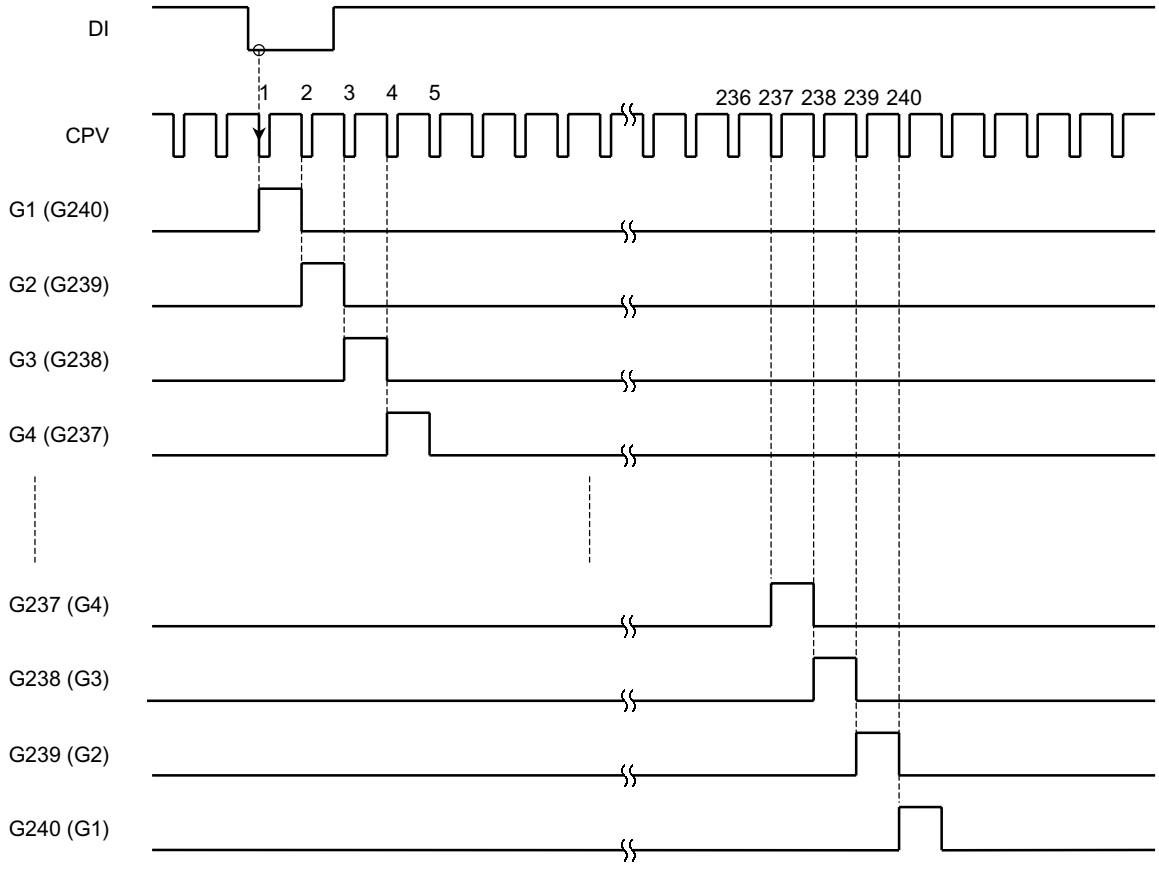
OCM	U/D	Shifting Direction
0	0	G240 → G239 → G238 → ····· → G3 → G2 → G1
0	1	G1 → G2 → G3 → ····· → G238 → G239 → G240
1	0	G220 → G219 → G218 → ····· → G3 → G2 → G1
1	1	G1 → G2 → G3 → ····· → G218 → G219 → G220

- Output mode switching function

  JBT6K48-AS is capable to control the output signal using /OE1 and /OE2 pins. The /OE2 signal proceeds the /OE1 signal at output-off mode.

/OE2	/OE1	Functions
1	1	Normal mode (Fig. 1)
	0	Output signals turn off unsynchronizing with CPV (Fig. 3)
0	1	Output signals turn off synchronizing with CPV (Fig. 2)
	0	/OE2 has priority no relation to /OE1 and output signals turn off

a) Normal operation mode



( ) indicates when U/D is Low.

Figure 1

b) Normal mode + Sync off mode (/OE2)

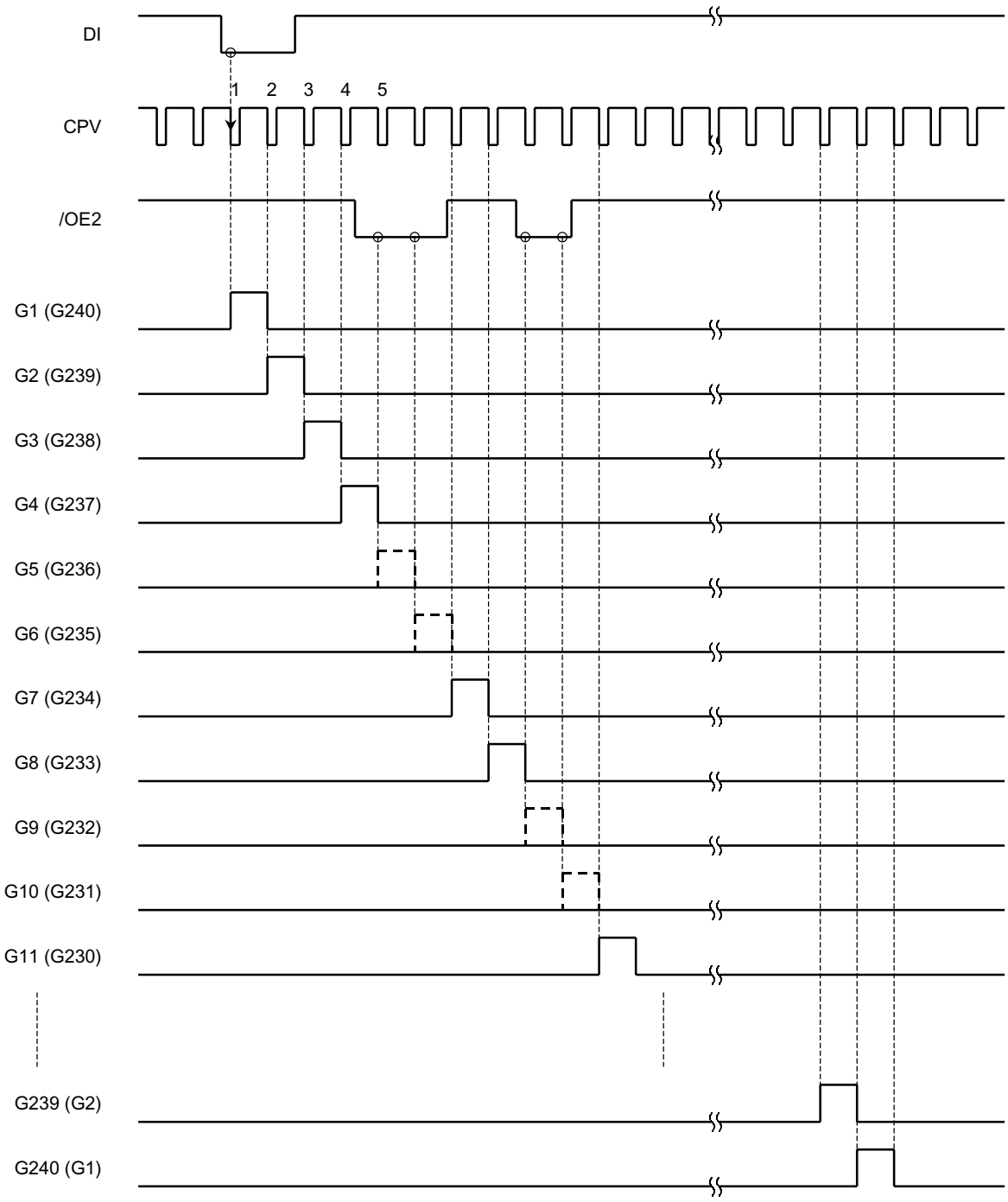


Figure 2

c) Normal mode+ ASYNC off mode (/OE1)

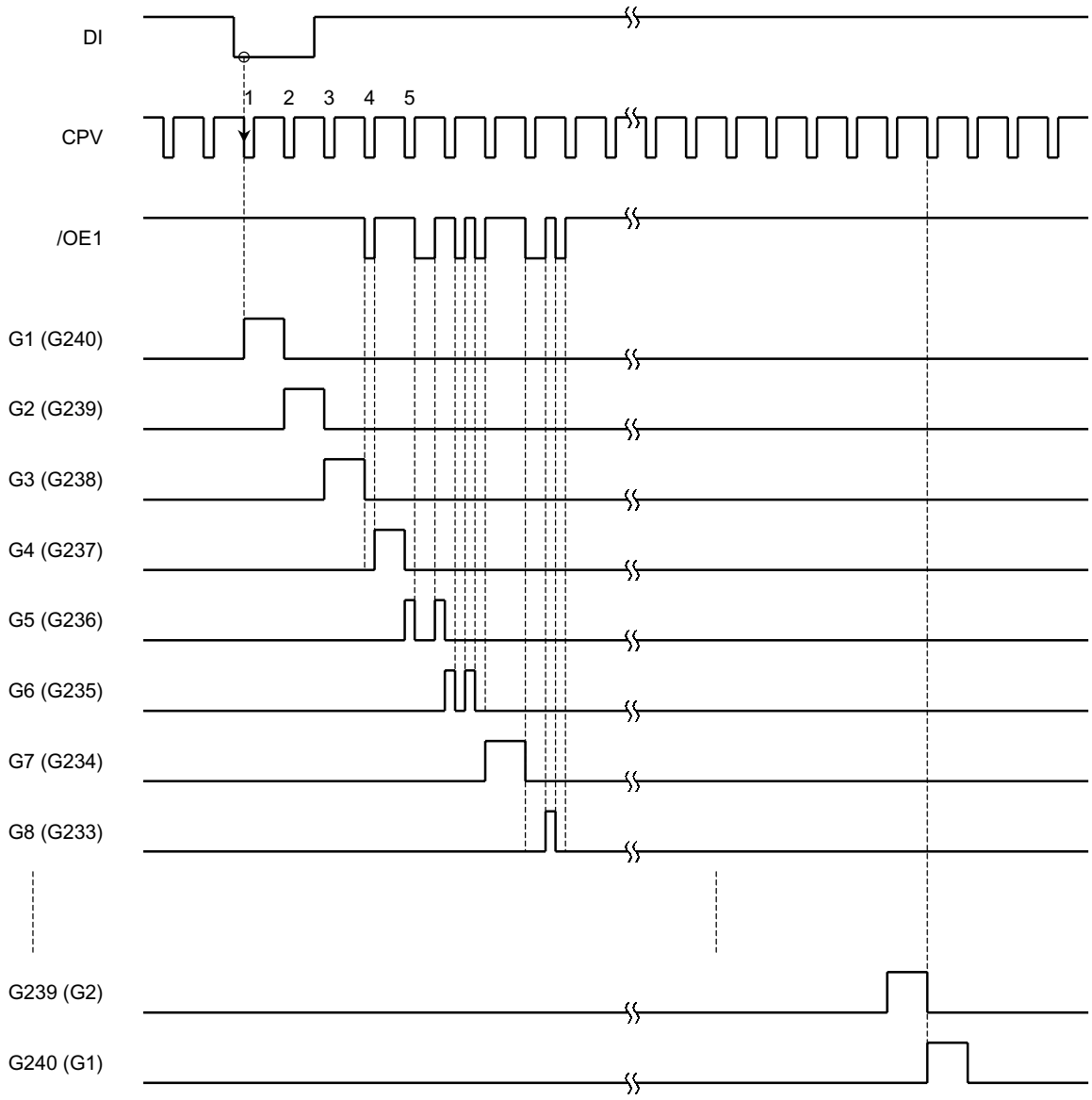


Figure 3

d) Synchronizing off mode + un-synchronizing off mode

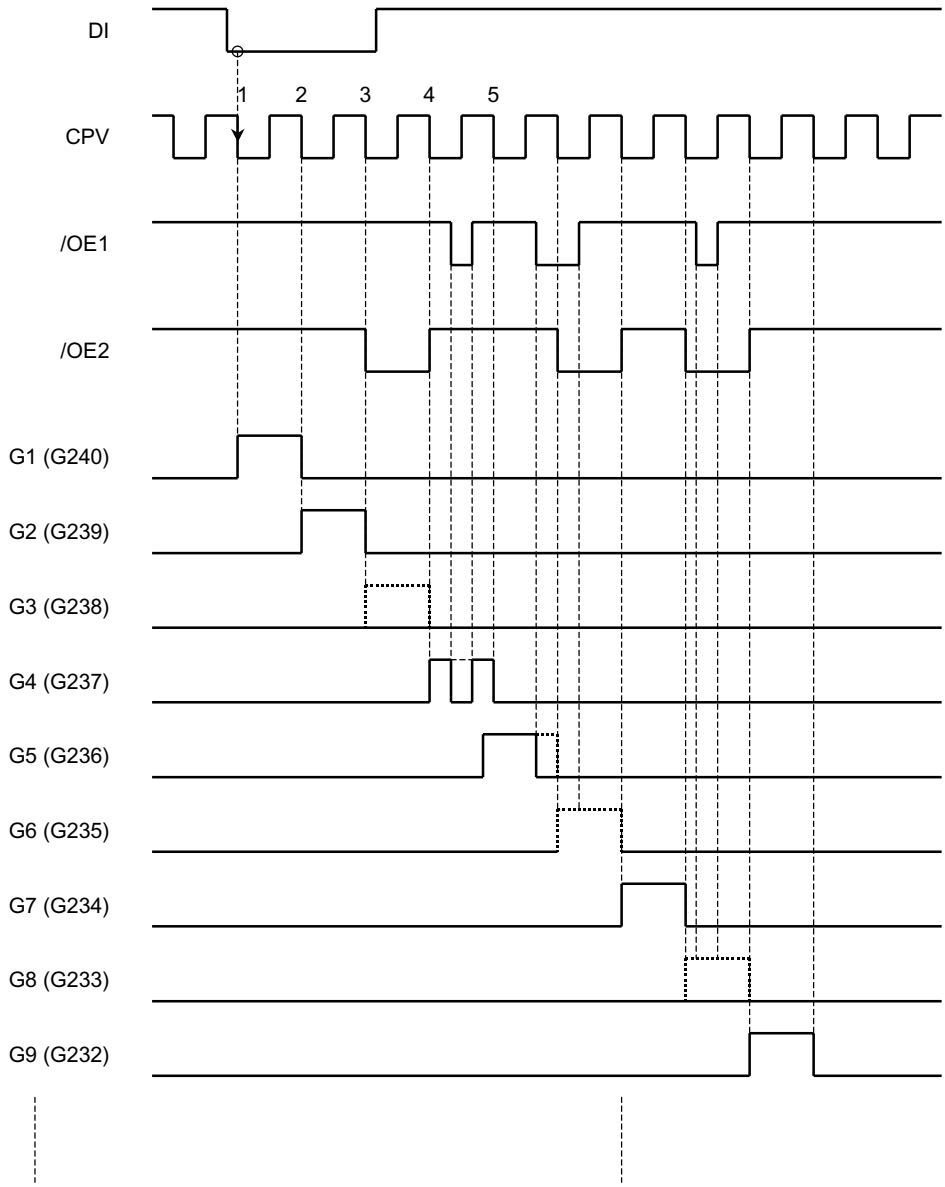


Figure 4

- Recommended Power-on and Power-off Sequence

  If the logic power supply is applied under the floating condition, the device might be destructed by the large amounts of current because the LCD panel drive voltage is high. For this reason, apply the logic power supply first, then turn the LCD panel drive power supply on, or turn the both power supply on at the same timing. The internal logic condition is instable immediately after the logic power-on. Therefore, initialize the internal logic by transferring the clock for the continuous connecting and setting period using the CPV and DI input.

  Turn the LCD panel drive power off first, then turn the logic power off, or turn the both power off at the same timing.

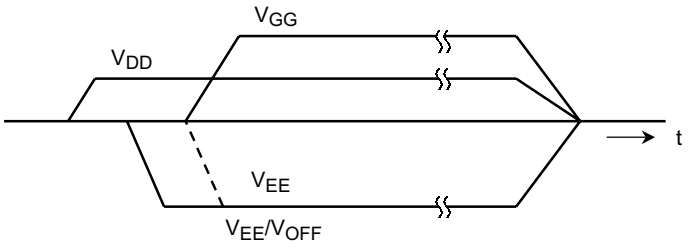
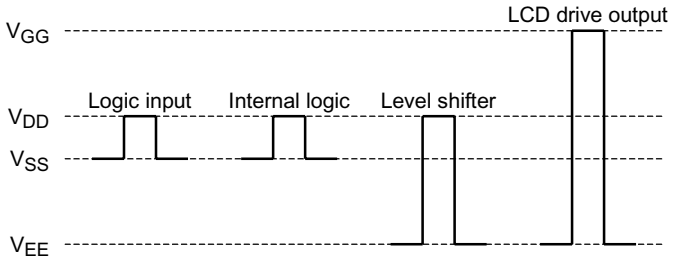


Figure 1

- Relations between power supplies



Maximum Ratings (Unless Otherwise Noted, V_{SS} = 0 V, Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage (1)	V_{DD}	−0.3 to 6.5	V
Supply voltage (2)	V_{EE}	−20.0 to 0.3	V
Supply voltage (3)	$V_{GG} - V_{EE}$	−0.3 to 45.0	V
Input voltage	V_{IN}	−0.3 to V_{DD} + 0.3	V
Operating temperature	T_{opr}	−20 to 75	°C
Storage temperature	T_{stg}	−55 to 125	°C

Electrical Characteristics

DC Characteristics (1) (Unless Otherwise Noted, $V_{GG} - V_{EE}$ = 16.0 to 33.0 V, V_{DD} = 2.5 to 3.6 V, Ta = –20 to 75°C)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Relevant Pin
Supply voltage 1)		V_{DD}	—	—	2.5	—	3.6	V	$V_{DDL/R}$
Supply voltage (2)		V_{EE}	—	—	–16.5	–11.0	–5	V	$V_{EEL/R}$
Supply voltage (3)		V_{GG}	—	—	8	12.5	16.5	V	$V_{GGL/R}$
Supply voltage (4)		$\lvert V_{GG} - V_{EE} \rvert$	—	—	16.0	—	33.0	V	$V_{GGL/R}$, $V_{EEL/R}$
Input voltage	Low level	V_{IL}	—	—	V_{SS}	—	0.2 V_{DD}	V	DI, CPV, U/D, /OE1, /OE2, OCM
	High level	V_{IH}			0.8 V_{DD}	—	V_{DD}		
Output resistance	Low level	R_{OL}	—	$V_{OUT} = V_{OFF} + 0.5$ V	—	—	7.5	kΩ	G1 to G240
	High level	R_{OH}		$V_{OUT} = V_{GG} - 0.5$ V	—	—	7.5		
Input leakage current		I_{IN}	—	—	–1	—	1	μA	DI, CPV, U/D, /OE1, /OE2, OCM
Operating frequency		f_{CPV1}	—	—	—	20	50	kHz	CPV
Output load capacitance		C_{L1}	—	(Note 3)	—	36	100	pF	G1~G240

Note 3: Load capacitance per an output pin.

DC Characteristics (2) (Unless Otherwise Noted, $V_{GG} - V_{EE}$ = 16.0 to 33.0 V, V_{DD} = 2.5 to 3.6 V, Ta = –20 to 75°C; Typical value is V_{DD} = 3.0 V, $V_{GG} - V_{EE}$ = 30.0 V, CPV = 20 kHz, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Relevant Pin
Current dissipation (1)	I_{GG}	—	(Note 4, 5)	—	3.2	30.0	μA	$V_{GGL/R}$
Current dissipation (2)	I_{EE}	—	(Note 4, 5)	—	3.3	–30.0		$V_{EEL/R}$
Current dissipation (3)	I_{DD}	—	(Note 4)	—	1.8	12.5		$V_{DDL/R}$
Current dissipation (4)	I_{SS}	—	(Note 4)	—	1.7	–13.0		$V_{SSL/R}$
Current dissipation (5)	STB	—	(Note 6)	–1	—	1		$V_{GGL/R}$, $V_{EEL/R}$, $V_{DDL/R}$, $V_{SSL/R}$

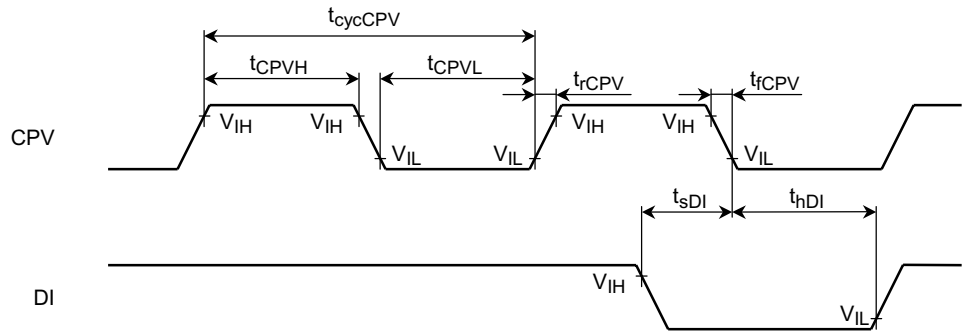
Note 4: CPV = 50 kHz

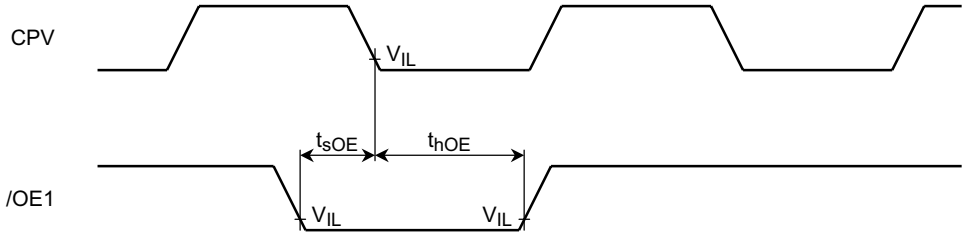
Note 5: f_{Fram} = 70 Hz

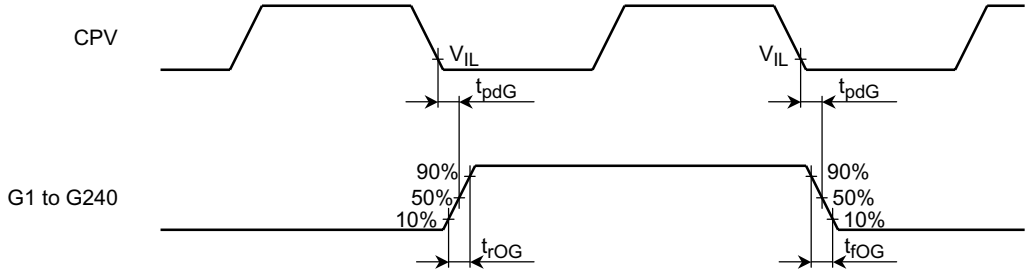
Note 6: CPV = "L"

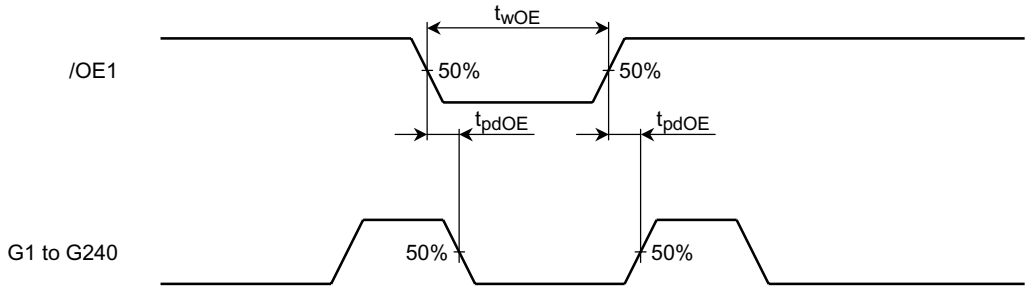
AC Characteristics (Unless Otherwise Noted, $V_{GG} - V_{EE}$ = 30.0 V, V_{DD} = 2.5 to 3.6 V, Ta = –20 to 75°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
CPV cycle time	t_{cycCPV}	—	—			10	μs
CPV pulse width Low level	t_{CPVL}	—	—	500			ns
CPV pulse width High level	t_{CPVH}	—	—	5			μs
CPV rising/falling time	t_{rCPV} /t_{fCPV}	—	—			100	ns
/OE enable time	t_{wOE}	—	—	1			μs
Data setup time	t_{sDI}	—	—	100			ns
	t_{sOE}	—	—	100			
Data hold time	t_{hDI}	—	—	300			ns
	t_{hOE}	—	—	300			
Output delay time (1)	t_{pdG}	—	C_L = 100 pF			2	μs
Output delay time (2)	t_{pdOE}	—	C_L = 100 pF			2	μs
Output rising/falling time	t_{rOG} /t_{fOG}	—	C_L = 100 pF			1.5	μs


tcycCPV
tCPVH
tCPVL
trCPV
tfCPV
CPV
VIH
VIL
tsDI
thDI
DI


CPV
VIL
tsOE
thOE
/OE1


CPV
VIL
tpdG
G1 to G240
90%
50%
10%
trOG
tfOG


twOE
/OE1
50%
tpdOE
G1 to G240

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000707EBM

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