Data Sheet October 26, 2004 FN2925.9

Dual and Quad, 8MHz, Low Noise Operational Amplifiers

Low noise and high performance are key words describing HA-5102 and HA-5104. These general purpose amplifiers offer an array of dynamic specifications including a 3V/µs slew rate and 8MHz bandwidth. Complementing these outstanding parameters is a very low noise specification of 4.3nV/$\sqrt{Hz}$ at 1kHz.

Fabricated using the Intersil high frequency DI process, these operational amplifiers also offer excellent input specifications such as a 0.5mV offset voltage and 30nA offset current. Complementing these specifications are 108dB open loop gain and 60dB channel separation. Consuming a very modest amount of power (90mW/ package for duals and 150mW/package for quads), HA-5102/04 also provide 15mA of output current.

This impressive combination of features make this series of amplifiers ideally suited for designs ranging from audio amplifiers and active filters to the most demanding signal conditioning and instrumentation circuits.

These operational amplifiers are available in dual or quad form with industry standard pinouts allowing for immediate interchangeability with most other dual and quad operational amplifiers.

HA-5102 Dual, Comp. HA-5104 Quad, Comp.

Refer to the /883 data sheet for military product.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. DWG. #
HA7-5102-2	-55 to 125	8 Ld CERDIP	F8.3A
HA1-5104-2	-55 to 125	14 Ld CERDIP	F14.3
HA9P5104-9	-40 to 85	16 Ld SOIC	M16.3

Features

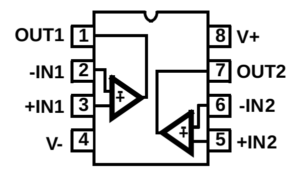
- Low Noise . . . . 4.3nV/$\sqrt{Hz}$
- Bandwidth . . . . 8MHz (Compensated)
- Slew Rate. 3V/µs (Compensated)
- Low Offset Voltage. 0.5mV
- Available in Duals or Quads

Applications

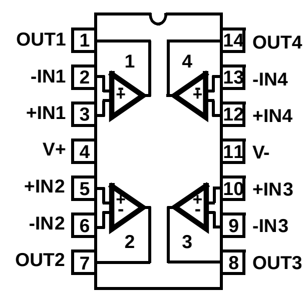
- High Q, Active Filters
- Audio Amplifiers
- Instrumentation Amplifiers
- Integrators
- Signal Generators
- For Further Design Ideas, See Application Note AN554

Pinouts

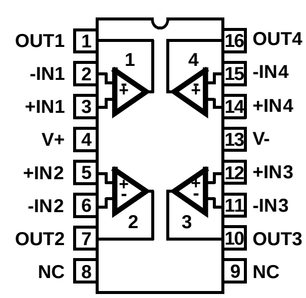
HA-5102 (CERDIP)
TOP VIEW



HA-5104 (CERDIP)
TOP VIEW



HA5104 (SOIC)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 7V
Input Voltage . . . . $\pm V_{SUPPLY}$
Output Short Circuit Duration (Note 3). . . . . Indefinite

Operating Conditions

Temperature Range
HA-510X-2 . . . . -55°C to 125°C
HA-5104-9 . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Lead CERDIP Package	115	28
14 Lead CERDIP Package	75	20
SOIC Package	100	N/A

Maximum Junction Temperature (Note 1, Hermetic Package) . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . 150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load, must be designed to maintain the maximum junction temperature below 175°C for hermetic packages, and below 150°C for plastic packages.
2. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
3. Any one amplifier may be shorted to ground indefinitely.

Electrical Specifications $V_{SUPPLY} = \pm 15V$, Unless Otherwise Specified

PARAMETER		TEMP. (°C)	HA-5102-2			HA-5104-2			HA-5104-9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS												
Offset Voltage		25	-	0.5	2.0	-	0.5	2.5	-	0.5	2.5	mV
		Full	-	-	2.5	-	-	3.0	-	-	3.0	mV
Offset Voltage Average Drift		Full	-	3	-	-	3	-	-	3	-	μV/°C
Bias Current		25	-	130	200	-	130	200	-	130	200	nA
		Full	-	-	325	-	-	325	-	-	500	nA
Offset Current		25	-	30	75	-	30	75	-	30	75	nA
		Full	-	-	125	-	-	125	-	-	125	nA
Input Resistance		25	-	500	-	-	500	-	-	500	-	kΩ
Common Mode Range		Full	±12	-	-	±12	-	-	±12	-	-	V
TRANSFER CHARACTERISTICS												
Large Signal Voltage Gain, ($V_{OUT} = \pm 5V$, $R_L = 2k\Omega$)		25	100	250	-	100	250	-	80	250	-	kV/V
		Full	100	-	-	100	-	-	80	-	-	kV/V
Common Mode Rejection Ratio ($V_{CM} = \pm 5.0V$)		Full	86	95	-	86	95	-	80	95	-	dB
Small Signal Bandwidth, ($A_V = 1$)		25	-	8	-	-	8	-	-	8	-	MHz
Channel Separation (Note 4)		25	-	60	-	-	60	-	-	60	-	dB
OUTPUT CHARACTERISTICS												
Output Voltage Swing	($R_L = 10k\Omega$)	Full	±12	±13	-	±12	±13	-	±12	±13	-	V
	($R_L = 2k\Omega$)	Full	±10	±12	-	±10	±12	-	±10	±12	-	V
Output Current, ($V_{OUT} = \pm 5V$)		Full	±10	±15	-	±10	±15	-	±7	±15	-	mA
Full Power Bandwidth (Note 5)		25	16	47	-	16	47	-	16	47	-	kHz
Output Resistance		25	-	110	-	-	110	-	-	110	-	Ω
STABILITY												
Minimum Stable Closed Loop Gain		Full	1	-	-	1	-	-	1	-	-	V/V
TRANSIENT RESPONSE (Note 6)												

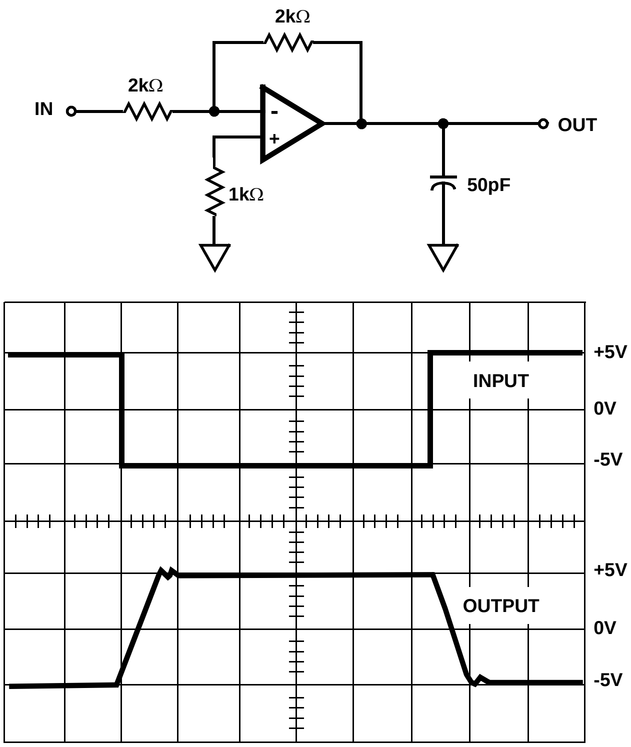
Electrical Specifications V_{SUPPLY} = ±15V, Unless Otherwise Specified **(Continued)**

PARAMETER		TEMP. (°C)	HA-5102-2			HA-5104-2			HA-5104-9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Rise Time		25	-	108	200	-	108	200	-	108	200	ns
Overshoot		25	-	20	35	-	20	35	-	20	35	%
Slew Rate		25	1	3	-	1	3	-	1	3	-	V/μs
Settling Time (Note 7)		25	-	4.5	-	-	4.5	-	-	4.5	-	μs
NOISE CHARACTERISTICS (Note 8)												
Input Noise Voltage	f = 10Hz	25	-	9	25	-	9	25	-	9	25	$nV/\sqrt{Hz}$
	f = 1kHz	25	-	4.3	6.0	-	4.3	6.0	-	4.3	6.0	$nV/\sqrt{Hz}$
Input Noise Current	f = 10Hz	25	-	5.1	15	-	5.1	15	-	5.1	15	$pA/\sqrt{Hz}$
	f = 1kHz	25	-	0.57	3	-	0.57	3	-	0.57	3	$pA/\sqrt{Hz}$
Broadband Noise Voltage	f = DC to 30kHz	25	-	870	-	-	870	-	-	870	-	nV_{RMS}
POWER SUPPLY CHARACTERISTICS												
Supply Current (All Amps)		25	-	3.0	5.0	-	5.0	6.5	-	5.0	6.5	mA
Power Supply Rejection Ratio, (ΔV_S = ±5V)		Full	86	100	-	86	100	-	80	100	-	dB

NOTES:

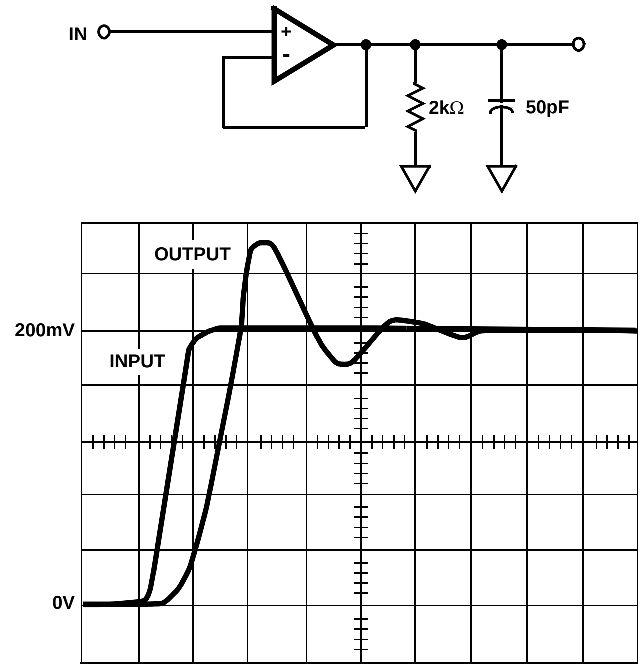
4. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 100mV_{PEAK}; R_S = 1kΩ.
5. Full power bandwidth is guaranteed by equation: Full power bandwidth $= \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
6. Refer to Test Circuits section of the data sheet.
7. Settling time is measured to 0.1% of final value for a 10V input step, A_V = -1.
8. The limits for these parameters are guaranteed based on lab characterization, and reflect lot-to-lot variation.

Test Circuits and Waveforms



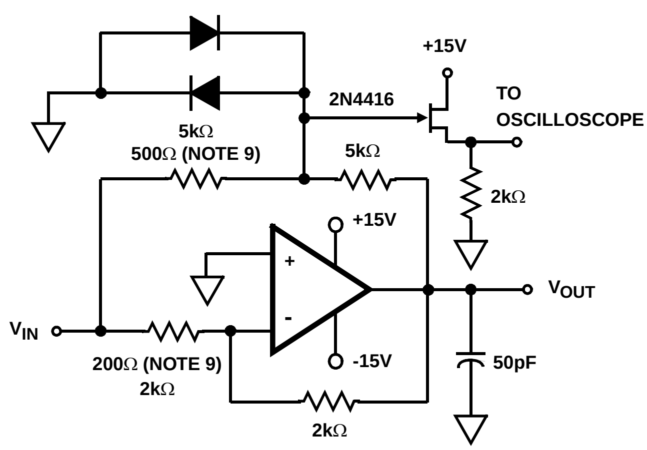
Vertical = 5V/Div., Horizontal = 5µs/Div. (A_V = -1)

FIGURE 1. LARGE SIGNAL RESPONSE CIRCUIT



Vertical = 40mV/Div., Horizontal = 50ns/Div. (A_V = +1)

FIGURE 2. SMALL SIGNAL RESPONSE CIRCUIT

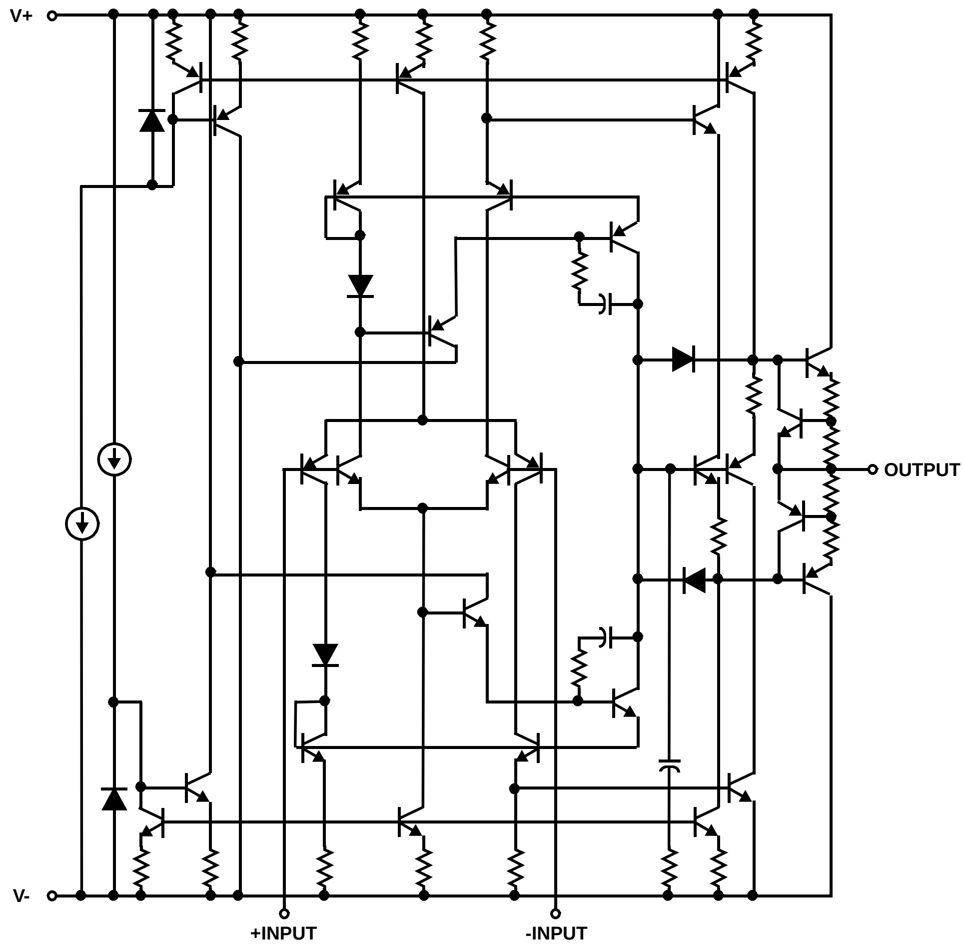


NOTES:

9. A_V = -1.
10. Feedback and summing resistors should be 0.1% matched.
11. Clipping diodes are optional, HP5082-2810 recommended.

FIGURE 3. SETTLING TIME CIRCUIT

Simplified Schematic



Typical Performance Curves

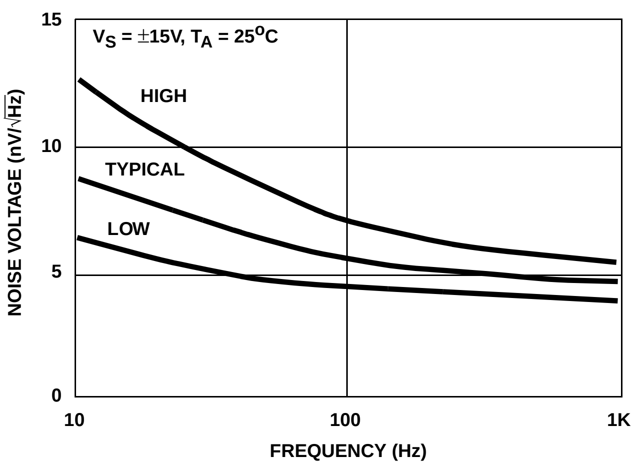


FIGURE 4. INPUT NOISE VOLTAGE DENSITY

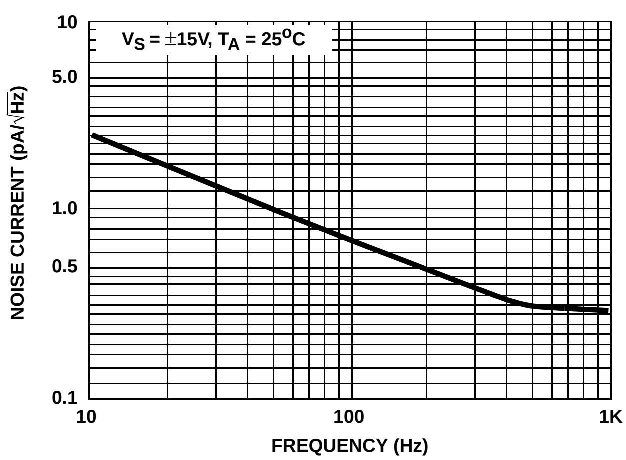
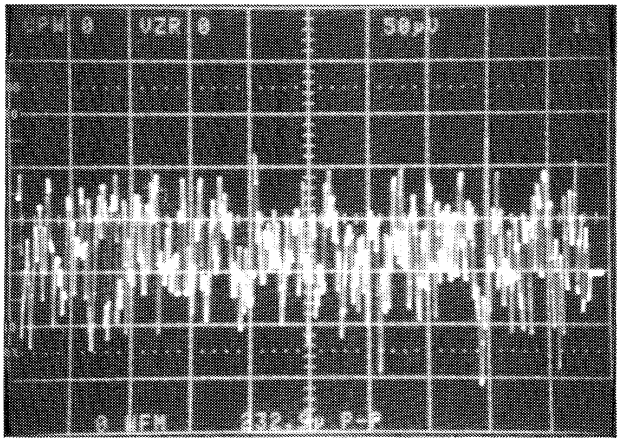
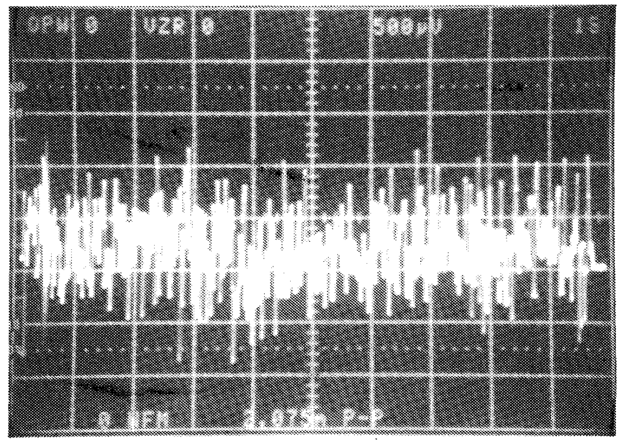


FIGURE 5. INPUT NOISE CURRENT DENSITY

Typical Performance Curves (Continued)



$V_S = \pm15V$, $T_A = 25^oC$, 50μV/Div., 1s/Div., $A_V = 1000V/V$
Input Noise = 0.232μV_{P-P}
FIGURE 6. 0.1Hz TO 10Hz NOISE



$V_S = \pm15V$, $T_A = 25^oC$, 500μV/Div., 1s/Div., $A_V = 1000V/V$
Total Output Noise = 2.075μV_{P-P}
FIGURE 7. 0.1Hz TO 1MHz NOISE

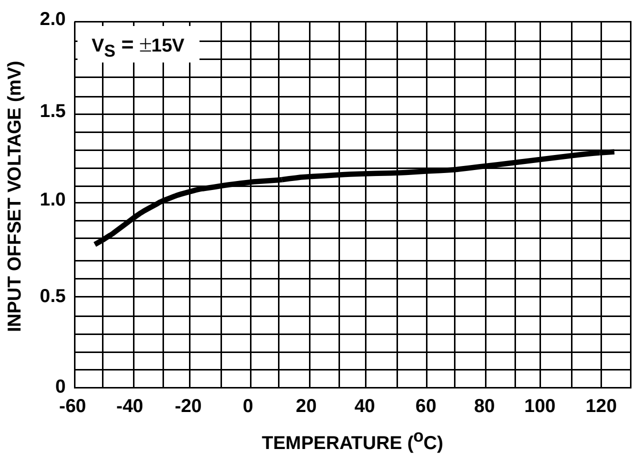


FIGURE 8. V_{IO} vs TEMPERATURE

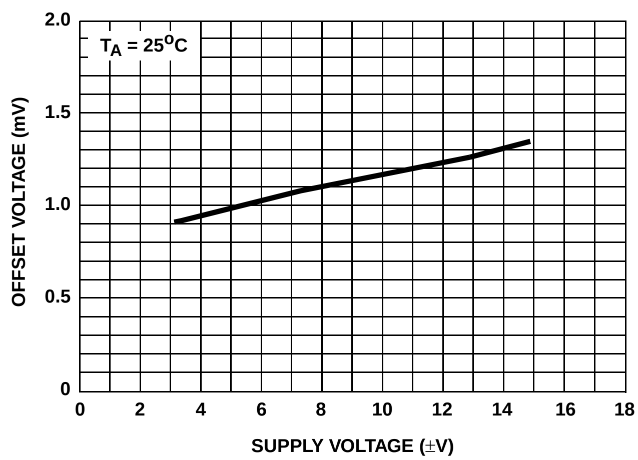


FIGURE 9. V_{IO} vs V_S

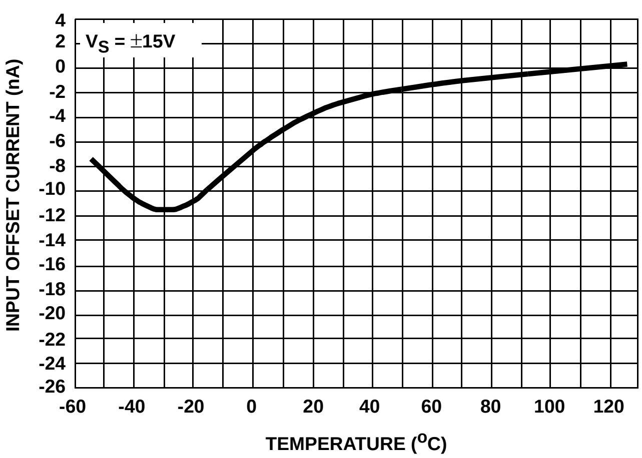


FIGURE 10. I_{IO} vs TEMPERATURE

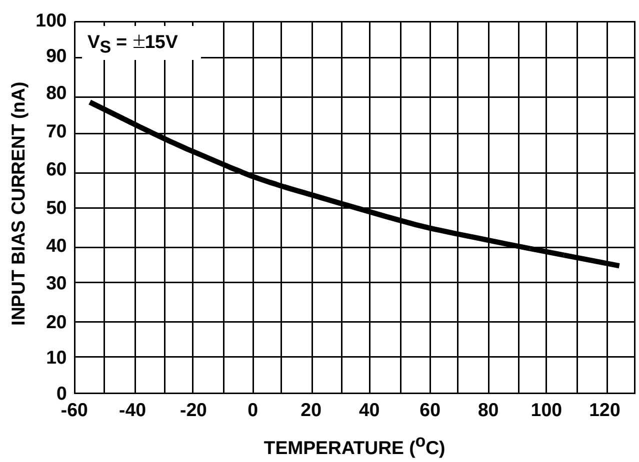


FIGURE 11. I_{BIAS} vs TEMPERATURE

Typical Performance Curves (Continued)

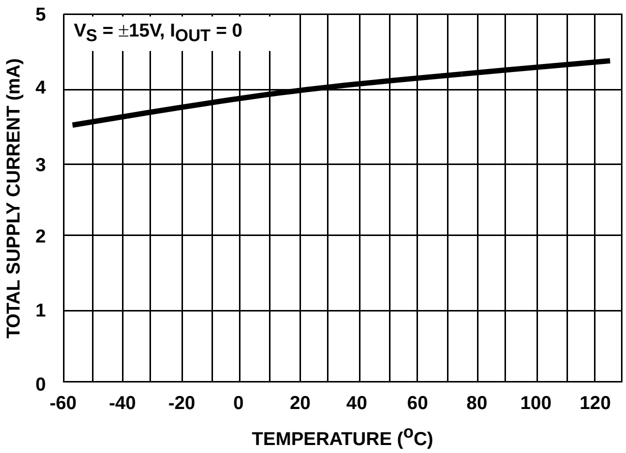


FIGURE 12. I_{CC} vs TEMPERATURE (HA-5104)

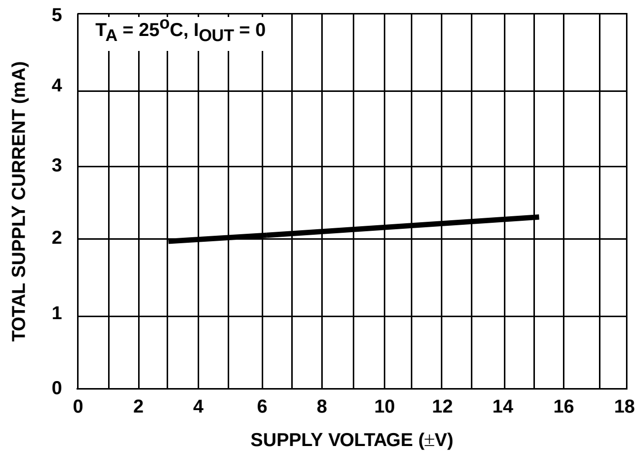


FIGURE 13. I_{CC} vs V_S (HA-5102)

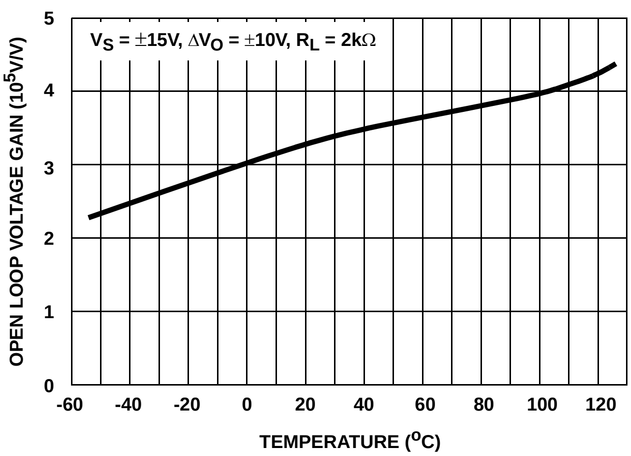


FIGURE 14. A_{VOL} vs TEMPERATURE

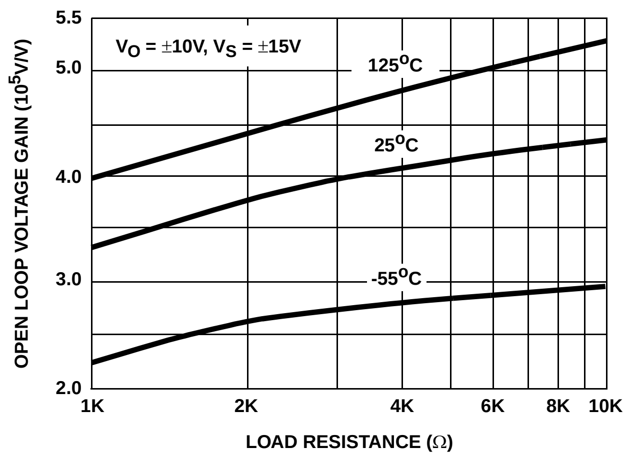


FIGURE 15. A_{VOL} vs LOAD RESISTANCE

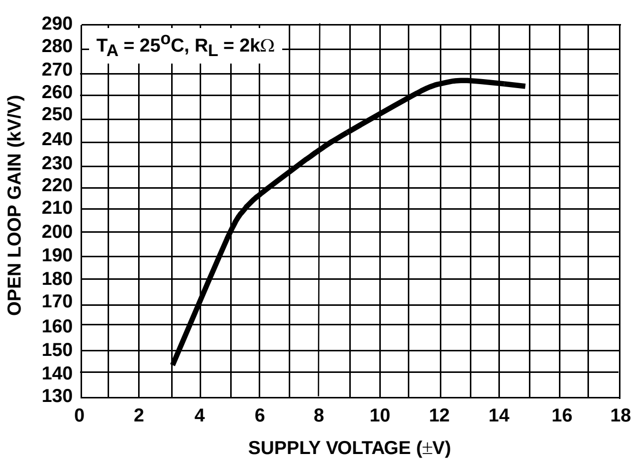


FIGURE 16. A_{VOL} vs V_S

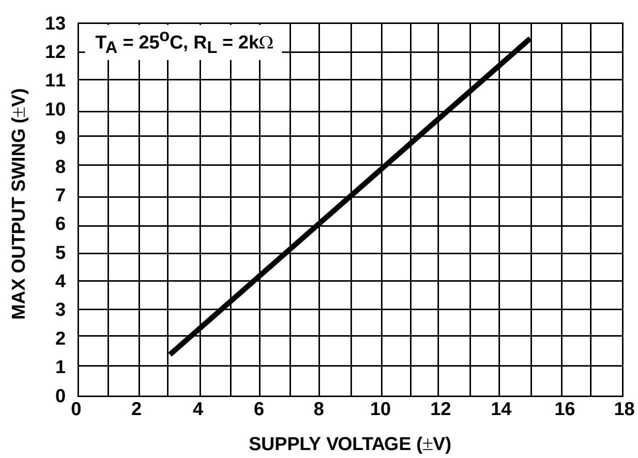


FIGURE 17. V_{OUT} vs V_S

Typical Performance Curves (Continued)

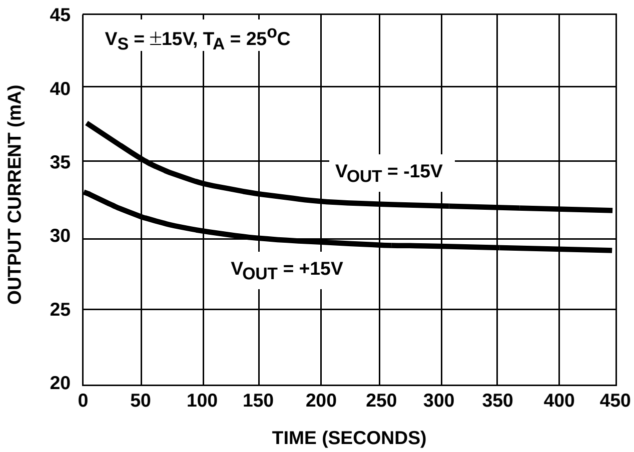


FIGURE 18. OUTPUT SHORT CIRCUIT CURRENT vs TIME

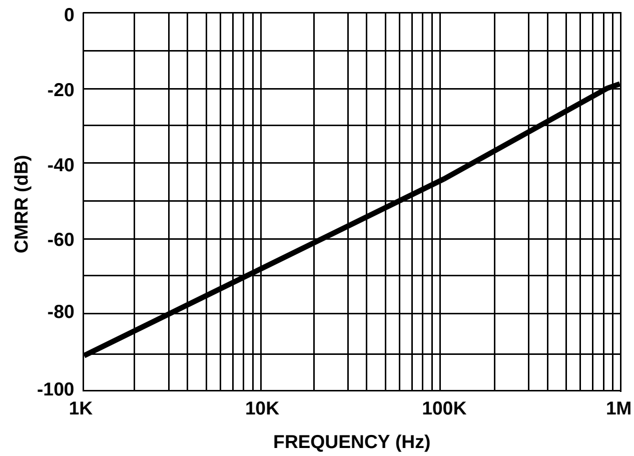


FIGURE 19. CMRR vs FREQUENCY

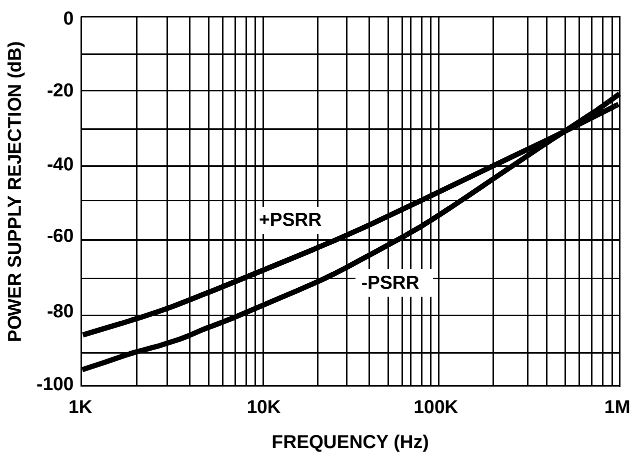


FIGURE 20. PSRR vs FREQUENCY

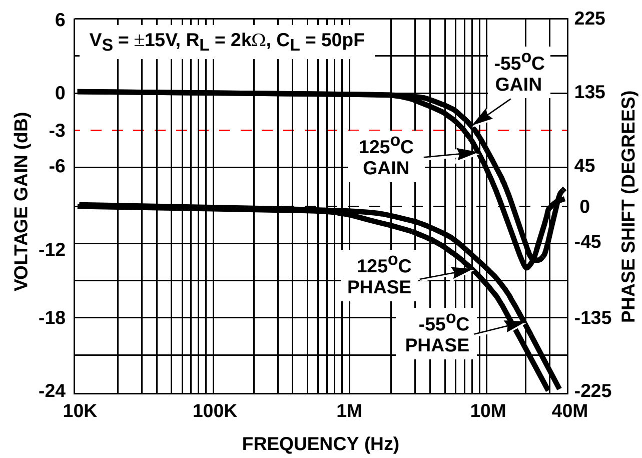


FIGURE 21. UNITY GAIN FREQUENCY RESPONSE

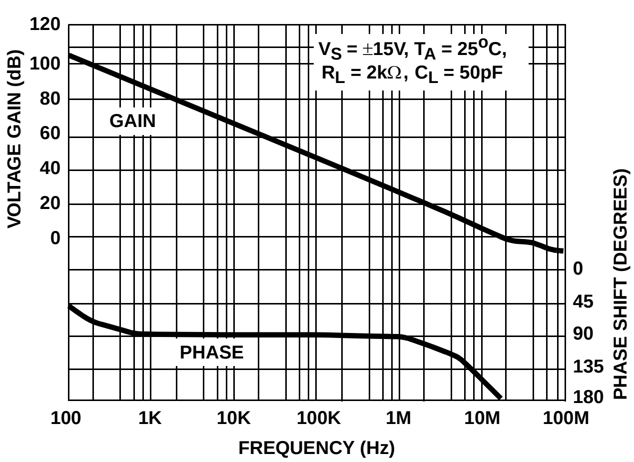


FIGURE 22. OPEN LOOP GAIN vs FREQUENCY

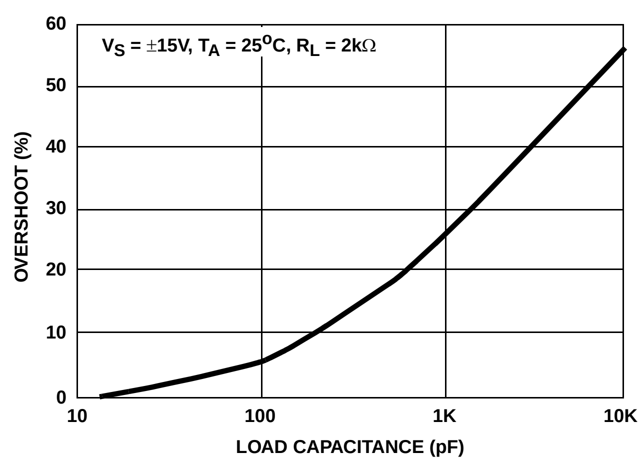


FIGURE 23. SMALL SIGNAL OVERSHOOT vs C_{LOAD}

Typical Performance Curves (Continued)

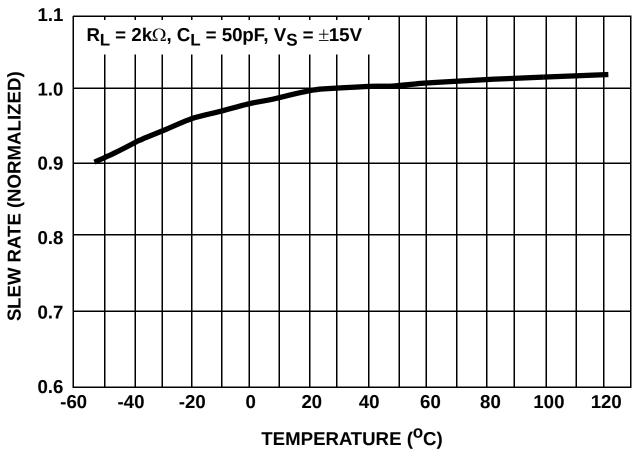


FIGURE 24. SLEW RATE vs TEMPERATURE

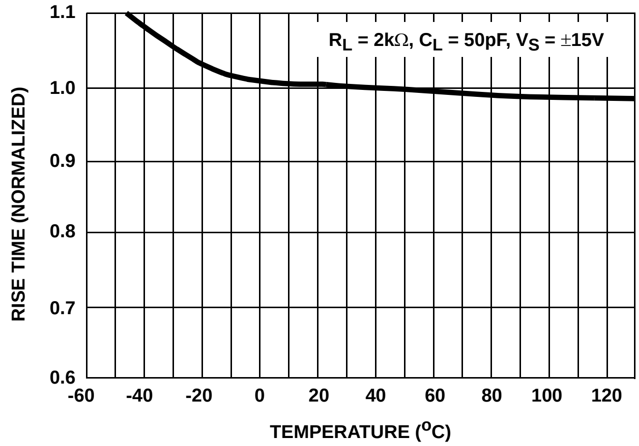


FIGURE 25. RISE TIME vs TEMPERATURE

Die Characteristics

DIE DIMENSIONS:

98.4 mils x 67.3 mils x 19 mils
2500μm x 1710μm x 483μm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (POWERED UP):

Unbiased

TRANSISTOR COUNT:

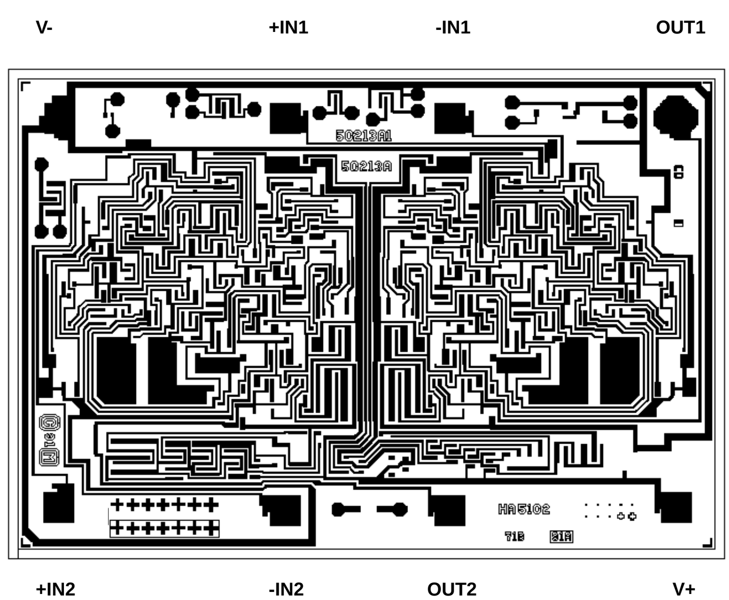
93

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5102



Die Characteristics

DIE DIMENSIONS:

95 mils x 99 mils x 19 mils
2420μm x 2530μm x 483μm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (POWERED UP):

Unbiased

TRANSISTOR COUNT:

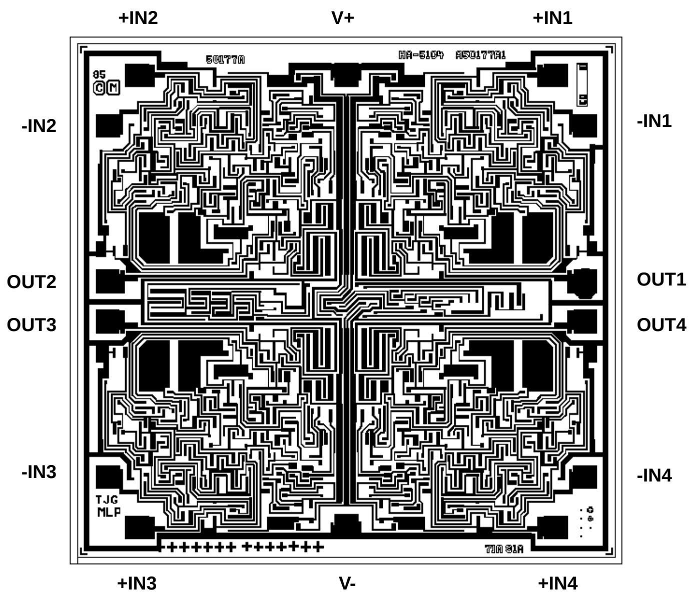
175

PROCESS:

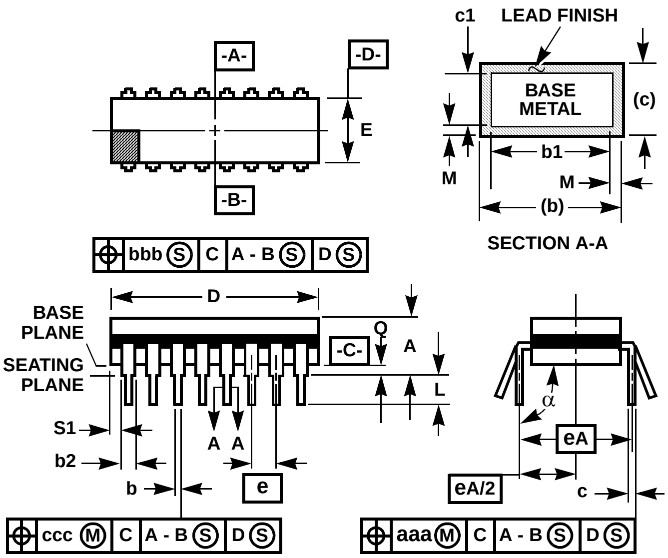
Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5104



Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH

F8.3A **MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)**
8 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	8		8		8

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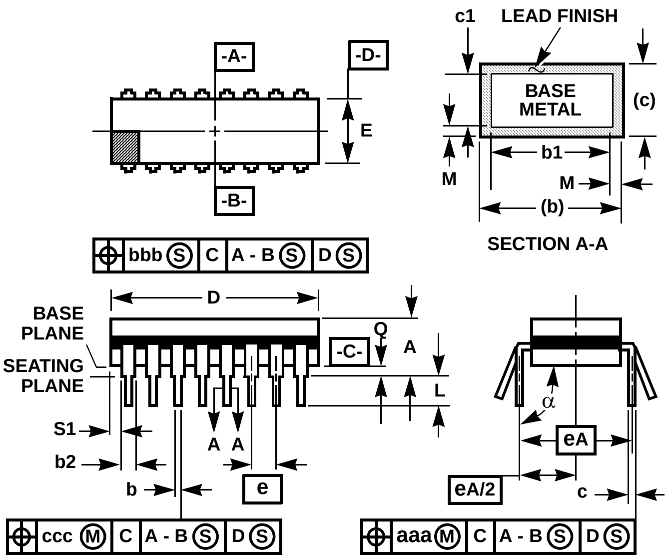
Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F14.3 MIL-STD-1835 GDIP1-T14 (D-1, CONFIGURATION A)
14 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	14		14		8

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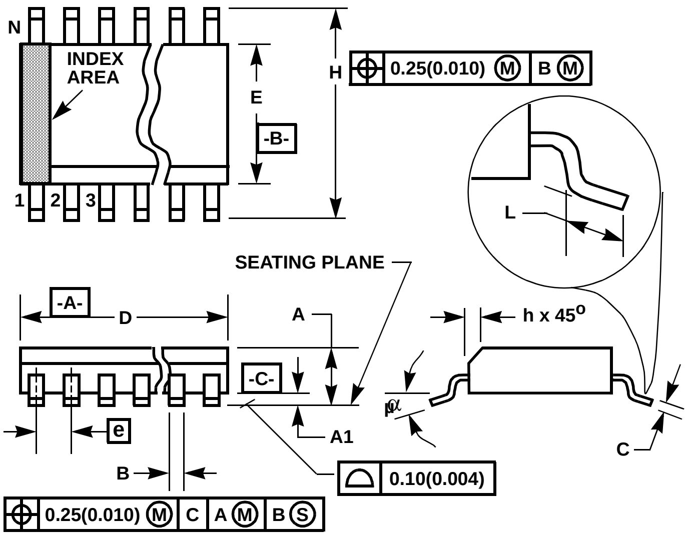
Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.3 **(JEDEC MS-013-AA ISSUE C)**
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

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