

Features

- High Performance, Low Power AVR[®] 8-Bit Microcontroller
- Advanced RISC Architecture
 - 120 Powerful Instructions – Most Single Clock Cycle Execution
 - 32 x 8 General Purpose Working Registers
 - Fully Static Operation
- High Endurance, Non-Volatile Memory Segments
 - 2K/4K Bytes of In-System, Self-Programmable Flash Program Memory
 - Endurance: 10,000 Write/Erase Cycles
 - 128/256 Bytes of In-System Programmable EEPROM
 - Endurance: 100,000 Write/Erase Cycles
 - 128/256 Bytes of Internal SRAM
 - Data retention: 20 years at 85°C / 100 years at 25°C
 - Programming Lock for Self-Programming Flash & EEPROM Data Security
- Peripheral Features
 - One 8-Bit and One 16-Bit Timer/Counter with Two PWM Channels, Each
 - 10-bit ADC
 - 8 Single-Ended Channels
 - 12 Differential ADC Channel Pairs with Programmable Gain (1x / 20x)
 - Programmable Watchdog Timer with Separate On-chip Oscillator
 - On-Chip Analog Comparator
 - Universal Serial Interface
- Special Microcontroller Features
 - debugWIRE On-chip Debug System
 - In-System Programmable via SPI Port
 - Internal and External Interrupt Sources
 - Pin Change Interrupt on 12 Pins
 - Low Power Idle, ADC Noise Reduction, Standby and Power-Down Modes
 - Enhanced Power-on Reset Circuit
 - Programmable Brown-Out Detection Circuit with Software Disable Function
 - Internal Calibrated Oscillator
 - On-Chip Temperature Sensor
- I/O and Packages
 - Available in 20-Pin QFN/MLF & 14-Pin SOIC and PDIP
 - Twelve Programmable I/O Lines
- Operating Voltage:
 - 1.8 – 5.5V
- Speed Grade:
 - 0 – 4 MHz @ 1.8 – 5.5V
 - 0 – 10 MHz @ 2.7 – 5.5V
 - 0 – 20 MHz @ 4.5 – 5.5V
- Industrial Temperature Range: -40°C to +85°C
- Low Power Consumption
 - Active Mode:
 - 210 µA at 1.8V and 1MHz
 - Idle Mode:
 - 33 µA at 1.8V and 1MHz
 - Power-Down Mode:
 - 0.1 µA at 1.8V and 25°C



8-bit AVR[®] Microcontroller with 2K/4K Bytes In-System Programmable Flash

ATtiny24A
(Preliminary)

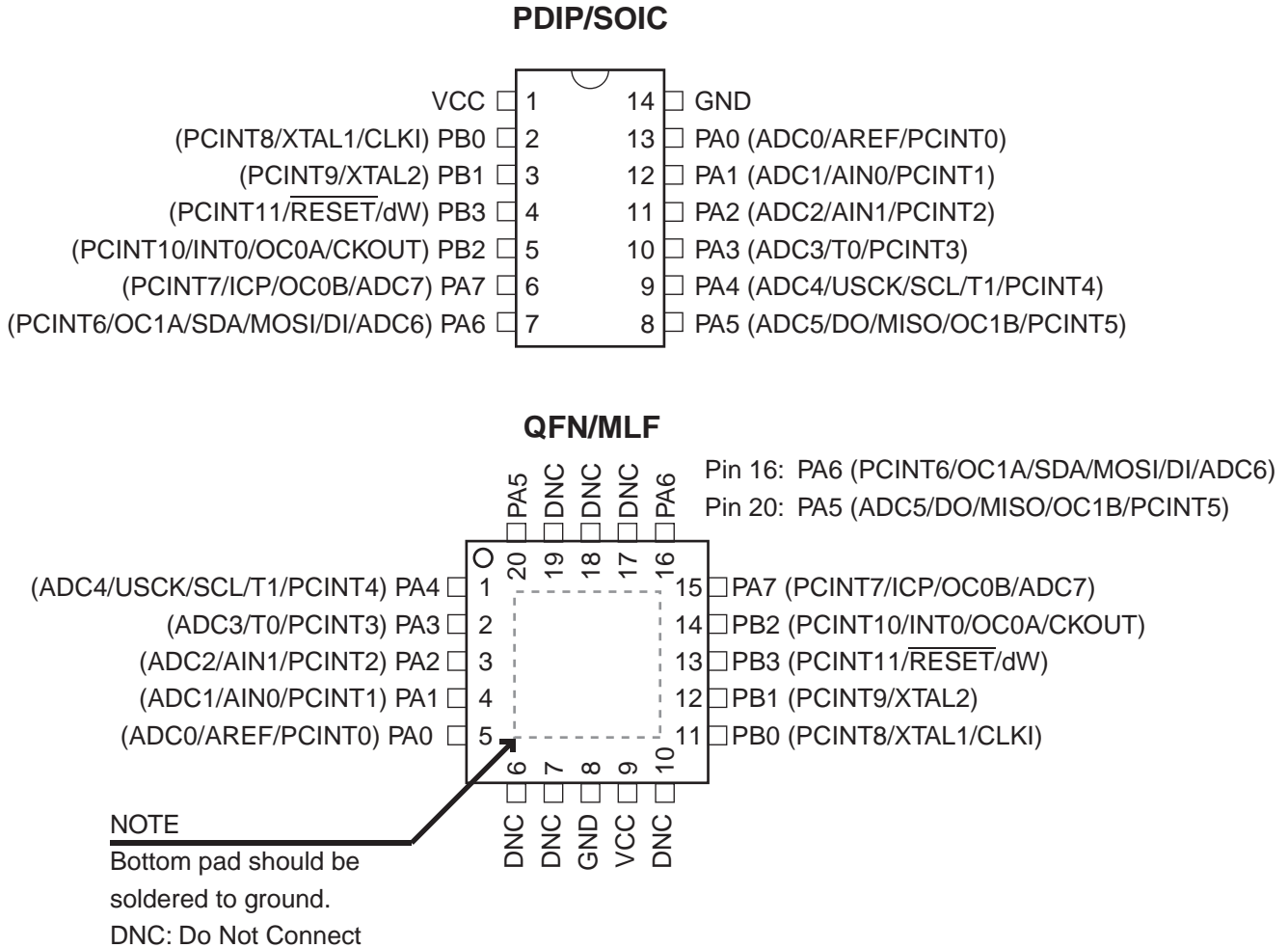
ATtiny44A

Summary



1. Pin Configurations

Figure 1-1. Pinout of ATtiny24A/44A



1.1 Pin Descriptions

1.1.1 VCC

Supply voltage.

1.1.2 GND

Ground.

1.1.3 Port B (PB3...PB0)

Port B is a 4-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability except PB3 which has the RESET capability. To use pin PB3 as an I/O pin, instead of RESET pin, program ('0') RSTDISBL fuse. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATtiny24A/44A as listed in [Section 10.2 “Alternate Port Functions” on page 57](#).

1.1.4 **RESET**

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running and provided the reset pin has not been disabled. The minimum pulse length is given in [Table 20-4 on page 176](#). Shorter pulses are not guaranteed to generate a reset.

The reset pin can also be used as a (weak) I/O pin.

1.1.5 **Port A (PA7...PA0)**

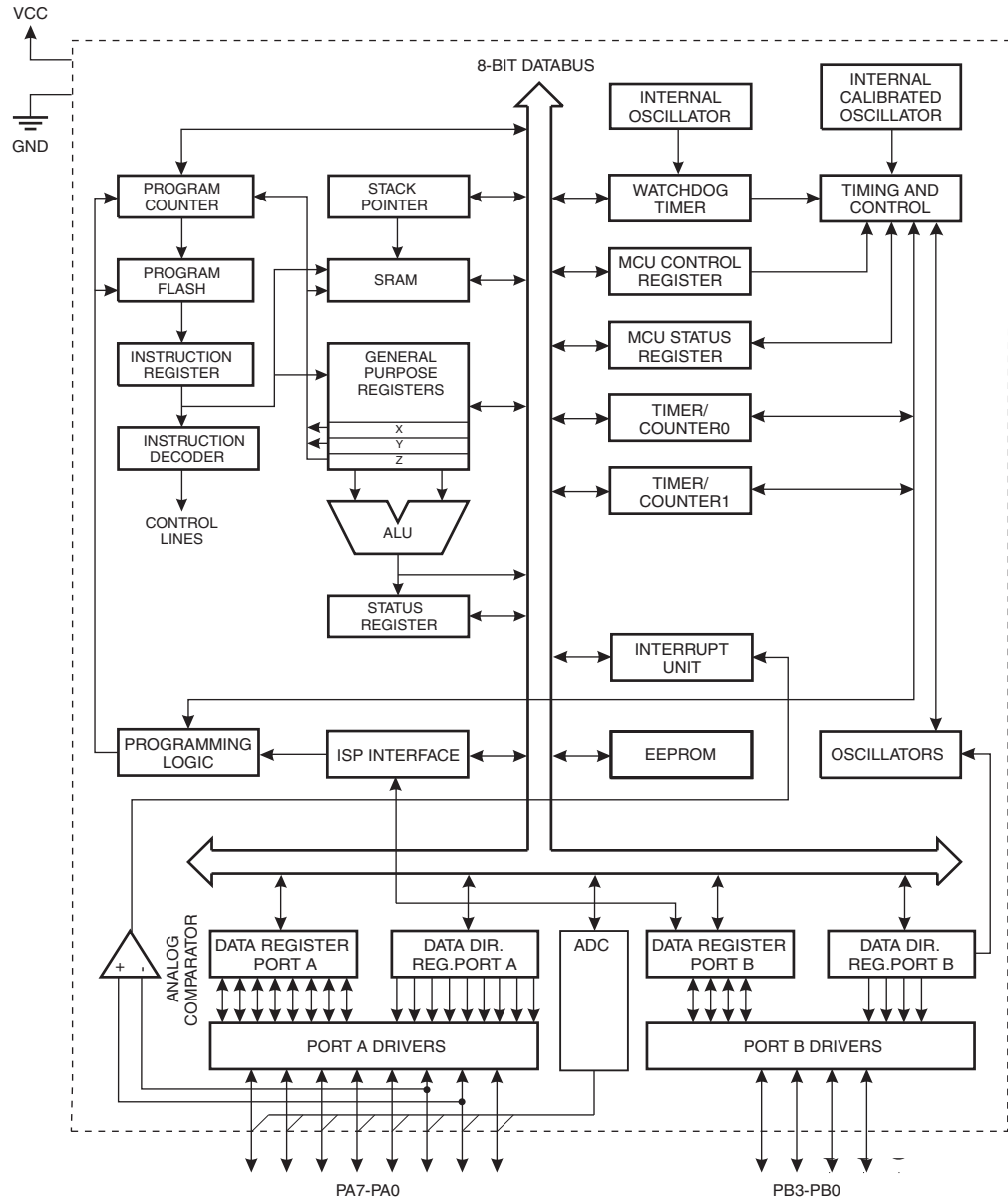
Port A is a 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A has alternate functions as analog inputs for the ADC, analog comparator, timer/counter, SPI and pin change interrupt as described in [“Alternate Port Functions” on page 57](#).

2. Overview

ATtiny24A/44A are low-power CMOS 8-bit microcontrollers based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny24A/44A achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

Figure 2-1. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATtiny24A/44A provides the following features: 2K/4K byte of In-System Programmable Flash, 128/256 bytes EEPROM, 128/256 bytes SRAM, 12 general purpose I/O lines, 32 general purpose working registers, an 8-bit Timer/Counter with two PWM channels, a 16-bit timer/counter with two PWM channels, Internal and External Interrupts, a 8-channel 10-bit ADC, programmable gain stage (1x, 20x) for 12 differential ADC channel pairs, a programmable Watchdog Timer with internal oscillator, internal calibrated oscillator, and four software selectable power saving modes. Idle mode stops the CPU while allowing the SRAM, Timer/Counter, ADC, Analog Comparator, and Interrupt system to continue functioning. ADC Noise Reduction mode minimizes switching noise during ADC conversions by stopping the CPU and all I/O modules except the ADC. In Power-down mode registers keep their contents and all chip functions are disabled until the next interrupt or hardware reset. In Standby mode, the crystal/resonator oscillator is running while the rest of the device is sleeping, allowing very fast start-up combined with low power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The on-chip ISP Flash allows the Program memory to be re-programmed in-system through an SPI serial interface, by a conventional non-volatile memory programmer or by an on-chip boot code running on the AVR core.

The ATtiny24A/44A AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators and Evaluation kits.

3. About

3.1 Resources

A comprehensive set of drivers, application notes, data sheets and descriptions on development tools are available for download at <http://www.atmel.com/avr>.

3.2 Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

For I/O Registers located in the extended I/O map, “IN”, “OUT”, “SBIS”, “SBIC”, “CBI”, and “SBI” instructions must be replaced with instructions that allow access to extended I/O. Typically, this means “LDS” and “STS” combined with “SBRS”, “SBRC”, “SBR”, and “CBR”. Note that not all AVR devices include an extended I/O map.

3.3 Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

3.4 Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device has been characterized.

4. Register Summary

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|-------------|----------|---|--------|--------|--------|---------|---------|---------|---------|----------------------|
| 0x3F (0x5F) | SREG | I | T | H | S | V | N | Z | C | Page 8 |
| 0x3E (0x5E) | SPH | – | – | – | – | – | – | SP9 | SP8 | Page 10 |
| 0x3D (0x5D) | SPL | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 | Page 10 |
| 0x3C (0x5C) | OCR0B | Timer/Counter0 – Output Compare Register B | | | | | | | | Page 83 |
| 0x3B (0x5B) | GIMSK | – | INT0 | PCIE1 | PCIE0 | – | – | – | – | Page 49 |
| 0x3A (0x5A) | GIFR | – | INTF0 | PCIF1 | PCIF0 | – | – | – | – | Page 50 |
| 0x39 (0x59) | TIMSK0 | – | – | – | – | – | OCIE0B | OCIE0A | TOIE0 | Page 83 |
| 0x38 (0x58) | TIFR0 | – | – | – | – | – | OCF0B | OCF0A | TOV0 | Page 83 |
| 0x37 (0x57) | SPMCSR | – | – | RSIG | CTPB | RFLB | PGWRT | PGERS | SPMEN | Page 156 |
| 0x36 (0x56) | OCR0A | Timer/Counter0 – Output Compare Register A | | | | | | | | Page 82 |
| 0x35 (0x55) | MCUCR | BODS | PUD | SE | SM1 | SM0 | BODSE | ISC01 | ISC00 | Pages 35, 49, and 65 |
| 0x34 (0x54) | MCUSR | – | – | – | – | WDRF | BORF | EXTRF | PORF | Page 43 |
| 0x33 (0x53) | TCCR0B | FOC0A | FOC0B | – | – | WGM02 | CS02 | CS01 | CS00 | Page 81 |
| 0x32 (0x52) | TCNT0 | Timer/Counter0 | | | | | | | | Page 82 |
| 0x31 (0x51) | OSCCAL | CAL7 | CAL6 | CAL5 | CAL4 | CAL3 | CAL2 | CAL1 | CAL0 | Page 29 |
| 0x30 (0x50) | TCCR0A | COM0A1 | COM0A0 | COM0B1 | COM0B0 | – | – | WGM01 | WGM00 | Page 78 |
| 0x2F (0x4F) | TCCR1A | COM1A1 | COM1A0 | COM1B1 | COM1B0 | – | – | WGM11 | WGM10 | Page 106 |
| 0x2E (0x4E) | TCCR1B | ICNC1 | ICES1 | – | WGM13 | WGM12 | CS12 | CS11 | CS10 | Page 108 |
| 0x2D (0x4D) | TCNT1H | Timer/Counter1 – Counter Register High Byte | | | | | | | | Page 110 |
| 0x2C (0x4C) | TCNT1L | Timer/Counter1 – Counter Register Low Byte | | | | | | | | Page 110 |
| 0x2B (0x4B) | OCR1AH | Timer/Counter1 – Compare Register A High Byte | | | | | | | | Page 110 |
| 0x2A (0x4A) | OCR1AL | Timer/Counter1 – Compare Register A Low Byte | | | | | | | | Page 110 |
| 0x29 (0x49) | OCR1BH | Timer/Counter1 – Compare Register B High Byte | | | | | | | | Page 110 |
| 0x28 (0x48) | OCR1BL | Timer/Counter1 – Compare Register B Low Byte | | | | | | | | Page 110 |
| 0x27 (0x47) | DWDR | DWDR[7:0] | | | | | | | | Page 151 |
| 0x26 (0x46) | CLKPR | CLKPCE | – | – | – | CLKPS3 | CLKPS2 | CLKPS1 | CLKPS0 | Page 30 |
| 0x25 (0x45) | ICR1H | Timer/Counter1 - Input Capture Register High Byte | | | | | | | | Page 111 |
| 0x24 (0x44) | ICR1L | Timer/Counter1 - Input Capture Register Low Byte | | | | | | | | Page 111 |
| 0x23 (0x43) | GTCCR | TSM | – | – | – | – | – | – | PSR10 | Page 114 |
| 0x22 (0x42) | TCCR1C | FOC1A | FOC1B | – | – | – | – | – | – | Page 109 |
| 0x21 (0x41) | WDTCR | WDIF | WDIE | WDP3 | WDCE | WDE | WDP2 | WDP1 | WDP0 | Page 43 |
| 0x20 (0x40) | PCMSK1 | – | – | – | – | PCINT11 | PCINT10 | PCINT9 | PCINT8 | Page 50 |
| 0x1F (0x3F) | Reserved | – | – | – | – | – | – | – | – | |
| 0x1E (0x3E) | EEARL | EEAR7 | EEAR6 | EEAR5 | EEAR4 | EEAR3 | EEAR2 | EEAR1 | EEAR0 | Page 20 |
| 0x1D (0x3D) | EEDR | EEPROM Data Register | | | | | | | | Page 21 |
| 0x1C (0x3C) | EEDR | – | – | EEDM1 | EEDM0 | EERIE | EEMPE | EEPE | EERE | Page 21 |
| 0x1B (0x3B) | PORTA | PORTA7 | PORTA6 | PORTA5 | PORTA4 | PORTA3 | PORTA2 | PORTA1 | PORTA0 | Page 65 |
| 0x1A (0x3A) | DDRA | DDA7 | DDA6 | DDA5 | DDA4 | DDA3 | DDA2 | DDA1 | DDA0 | Page 65 |
| 0x19 (0x39) | PINA | PINA7 | PINA6 | PINA5 | PINA4 | PINA3 | PINA2 | PINA1 | PINA0 | Page 66 |
| 0x18 (0x38) | PORTB | – | – | – | – | PORTB3 | PORTB2 | PORTB1 | PORTB0 | Page 66 |
| 0x17 (0x37) | DDRB | – | – | – | – | DDB3 | DDB2 | DDB1 | DDB0 | Page 66 |
| 0x16 (0x36) | PINB | – | – | – | – | PINB3 | PINB2 | PINB1 | PINB0 | Page 66 |
| 0x15 (0x35) | GPOR2 | General Purpose I/O Register 2 | | | | | | | | Page 22 |
| 0x14 (0x34) | GPOR1 | General Purpose I/O Register 1 | | | | | | | | Page 22 |
| 0x13 (0x33) | GPOR0 | General Purpose I/O Register 0 | | | | | | | | Page 22 |
| 0x12 (0x32) | PCMSK0 | PCINT7 | PCINT6 | PCINT5 | PCINT4 | PCINT3 | PCINT2 | PCINT1 | PCINT0 | Page 51 |
| 0x11 (0x31) | Reserved | – | | | | | | | | |
| 0x10 (0x30) | USIBR | USI Buffer Register | | | | | | | | Page 127 |
| 0x0F (0x2F) | USIDR | USI Data Register | | | | | | | | Page 123 |
| 0x0E (0x2E) | USISR | USISIF | USIOIF | USIPF | USIDC | USICNT3 | USICNT2 | USICNT1 | USICNT0 | Page 128 |
| 0x0D (0x2D) | USICR | USISIE | USIOIE | USIWM1 | USIWM0 | USICS1 | USICS0 | USICLK | USITC | Page 128 |
| 0x0C (0x2C) | TIMSK1 | – | – | ICIE1 | – | – | OCIE1B | OCIE1A | TOIE1 | Page 111 |
| 0x0B (0x2B) | TIFR1 | – | – | ICF1 | – | – | OCF1B | OCF1A | TOV1 | Page 112 |
| 0x0A (0x2A) | Reserved | – | | | | | | | | |
| 0x09 (0x29) | Reserved | – | | | | | | | | |
| 0x08 (0x28) | ACSR | ACD | ACBG | ACO | ACI | ACIE | ACIC | ACIS1 | ACIS0 | Page 129 |
| 0x07 (0x27) | ADMUX | REFS1 | REFS0 | MUX5 | MUX4 | MUX3 | MUX2 | MUX1 | MUX0 | Page 144 |
| 0x06 (0x26) | ADCSRA | ADEN | ADSC | ADATE | ADIF | ADIE | ADPS2 | ADPS1 | ADPS0 | Page 146 |
| 0x05 (0x25) | ADCH | ADC Data Register High Byte | | | | | | | | Page 148 |
| 0x04 (0x24) | ADCL | ADC Data Register Low Byte | | | | | | | | Page 148 |
| 0x03 (0x23) | ADCSRB | BIN | ACME | – | ADLAR | – | ADTS2 | ADTS1 | ADTS0 | Page 130, Page 148 |
| 0x02 (0x22) | Reserved | – | | | | | | | | |
| 0x01 (0x21) | DIDR0 | ADC7D | ADC6D | ADC5D | ADC4D | ADC3D | ADC2D | ADC1D | ADC0D | Page 131, Page 149 |
| 0x00 (0x20) | PRR | – | – | – | – | PRTIM1 | PRTIM0 | PRUSI | PRADC | Page 36 |





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- Note:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
 2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
 3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVR's, the CBI and SBI instructions will only operation the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.

5. Instruction Set Summary

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|--|----------|--|--|---------------|---------|
| ARITHMETIC AND LOGIC INSTRUCTIONS | | | | | |
| ADD | Rd, Rr | Add two Registers | $Rd \leftarrow Rd + Rr$ | Z,C,N,V,H | 1 |
| ADC | Rd, Rr | Add with Carry two Registers | $Rd \leftarrow Rd + Rr + C$ | Z,C,N,V,H | 1 |
| ADIW | Rd,K | Add Immediate to Word | $Rdh:Rdl \leftarrow Rdh:Rdl + K$ | Z,C,N,V,S | 2 |
| SUB | Rd, Rr | Subtract two Registers | $Rd \leftarrow Rd - Rr$ | Z,C,N,V,H | 1 |
| SUBI | Rd, K | Subtract Constant from Register | $Rd \leftarrow Rd - K$ | Z,C,N,V,H | 1 |
| SBC | Rd, Rr | Subtract with Carry two Registers | $Rd \leftarrow Rd - Rr - C$ | Z,C,N,V,H | 1 |
| SBCI | Rd, K | Subtract with Carry Constant from Reg. | $Rd \leftarrow Rd - K - C$ | Z,C,N,V,H | 1 |
| SBIW | Rd,K | Subtract Immediate from Word | $Rdh:Rdl \leftarrow Rdh:Rdl - K$ | Z,C,N,V,S | 2 |
| AND | Rd, Rr | Logical AND Registers | $Rd \leftarrow Rd \bullet Rr$ | Z,N,V | 1 |
| ANDI | Rd, K | Logical AND Register and Constant | $Rd \leftarrow Rd \bullet K$ | Z,N,V | 1 |
| OR | Rd, Rr | Logical OR Registers | $Rd \leftarrow Rd \vee Rr$ | Z,N,V | 1 |
| ORI | Rd, K | Logical OR Register and Constant | $Rd \leftarrow Rd \vee K$ | Z,N,V | 1 |
| EOR | Rd, Rr | Exclusive OR Registers | $Rd \leftarrow Rd \oplus Rr$ | Z,N,V | 1 |
| COM | Rd | One's Complement | $Rd \leftarrow 0xFF - Rd$ | Z,C,N,V | 1 |
| NEG | Rd | Two's Complement | $Rd \leftarrow 0x00 - Rd$ | Z,C,N,V,H | 1 |
| SBR | Rd,K | Set Bit(s) in Register | $Rd \leftarrow Rd \vee K$ | Z,N,V | 1 |
| CBR | Rd,K | Clear Bit(s) in Register | $Rd \leftarrow Rd \bullet (0xFF - K)$ | Z,N,V | 1 |
| INC | Rd | Increment | $Rd \leftarrow Rd + 1$ | Z,N,V | 1 |
| DEC | Rd | Decrement | $Rd \leftarrow Rd - 1$ | Z,N,V | 1 |
| TST | Rd | Test for Zero or Minus | $Rd \leftarrow Rd \bullet Rd$ | Z,N,V | 1 |
| CLR | Rd | Clear Register | $Rd \leftarrow Rd \oplus Rd$ | Z,N,V | 1 |
| SER | Rd | Set Register | $Rd \leftarrow 0xFF$ | None | 1 |
| BRANCH INSTRUCTIONS | | | | | |
| RJMP | k | Relative Jump | $PC \leftarrow PC + k + 1$ | None | 2 |
| IJMP | | Indirect Jump to (Z) | $PC \leftarrow Z$ | None | 2 |
| RCALL | k | Relative Subroutine Call | $PC \leftarrow PC + k + 1$ | None | 3 |
| ICALL | | Indirect Call to (Z) | $PC \leftarrow Z$ | None | 3 |
| RET | | Subroutine Return | $PC \leftarrow STACK$ | None | 4 |
| RETI | | Interrupt Return | $PC \leftarrow STACK$ | I | 4 |
| CPSE | Rd,Rr | Compare, Skip if Equal | if (Rd = Rr) $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| CP | Rd,Rr | Compare | $Rd - Rr$ | Z, N, V, C, H | 1 |
| CPC | Rd,Rr | Compare with Carry | $Rd - Rr - C$ | Z, N, V, C, H | 1 |
| CPI | Rd,K | Compare Register with Immediate | $Rd - K$ | Z, N, V, C, H | 1 |
| SBRC | Rr, b | Skip if Bit in Register Cleared | if (Rr(b)=0) $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBRS | Rr, b | Skip if Bit in Register is Set | if (Rr(b)=1) $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBIC | P, b | Skip if Bit in I/O Register Cleared | if (P(b)=0) $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBIS | P, b | Skip if Bit in I/O Register is Set | if (P(b)=1) $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| BRBS | s, k | Branch if Status Flag Set | if (SREG(s) = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRBC | s, k | Branch if Status Flag Cleared | if (SREG(s) = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BREQ | k | Branch if Equal | if (Z = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRNE | k | Branch if Not Equal | if (Z = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRCS | k | Branch if Carry Set | if (C = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRCC | k | Branch if Carry Cleared | if (C = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRSH | k | Branch if Same or Higher | if (C = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRLO | k | Branch if Lower | if (C = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRMI | k | Branch if Minus | if (N = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRPL | k | Branch if Plus | if (N = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRGE | k | Branch if Greater or Equal, Signed | if (N \oplus V = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRLT | k | Branch if Less Than Zero, Signed | if (N \oplus V = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRHS | k | Branch if Half Carry Flag Set | if (H = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRHC | k | Branch if Half Carry Flag Cleared | if (H = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRTS | k | Branch if T Flag Set | if (T = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRTC | k | Branch if T Flag Cleared | if (T = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRVS | k | Branch if Overflow Flag is Set | if (V = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRVC | k | Branch if Overflow Flag is Cleared | if (V = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRIE | k | Branch if Interrupt Enabled | if (I = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRID | k | Branch if Interrupt Disabled | if (I = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BIT AND BIT-TEST INSTRUCTIONS | | | | | |
| SBI | P,b | Set Bit in I/O Register | $I/O(P,b) \leftarrow 1$ | None | 2 |
| CBI | P,b | Clear Bit in I/O Register | $I/O(P,b) \leftarrow 0$ | None | 2 |
| LSL | Rd | Logical Shift Left | $Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$ | Z,C,N,V | 1 |
| LSR | Rd | Logical Shift Right | $Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$ | Z,C,N,V | 1 |
| ROL | Rd | Rotate Left Through Carry | $Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$ | Z,C,N,V | 1 |

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|-----------------------------------|----------|----------------------------------|--|---------|---------|
| ROR | Rd | Rotate Right Through Carry | $Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$ | Z,C,N,V | 1 |
| ASR | Rd | Arithmetic Shift Right | $Rd(n) \leftarrow Rd(n+1), n=0..6$ | Z,C,N,V | 1 |
| SWAP | Rd | Swap Nibbles | $Rd(3..0) \leftarrow Rd(7..4), Rd(7..4) \leftarrow Rd(3..0)$ | None | 1 |
| BSET | s | Flag Set | $SREG(s) \leftarrow 1$ | SREG(s) | 1 |
| BCLR | s | Flag Clear | $SREG(s) \leftarrow 0$ | SREG(s) | 1 |
| BST | Rr, b | Bit Store from Register to T | $T \leftarrow Rr(b)$ | T | 1 |
| BLD | Rd, b | Bit load from T to Register | $Rd(b) \leftarrow T$ | None | 1 |
| SEC | | Set Carry | $C \leftarrow 1$ | C | 1 |
| CLC | | Clear Carry | $C \leftarrow 0$ | C | 1 |
| SEN | | Set Negative Flag | $N \leftarrow 1$ | N | 1 |
| CLN | | Clear Negative Flag | $N \leftarrow 0$ | N | 1 |
| SEZ | | Set Zero Flag | $Z \leftarrow 1$ | Z | 1 |
| CLZ | | Clear Zero Flag | $Z \leftarrow 0$ | Z | 1 |
| SEI | | Global Interrupt Enable | $I \leftarrow 1$ | I | 1 |
| CLI | | Global Interrupt Disable | $I \leftarrow 0$ | I | 1 |
| SES | | Set Signed Test Flag | $S \leftarrow 1$ | S | 1 |
| CLS | | Clear Signed Test Flag | $S \leftarrow 0$ | S | 1 |
| SEV | | Set Twos Complement Overflow | $V \leftarrow 1$ | V | 1 |
| CLV | | Clear Twos Complement Overflow | $V \leftarrow 0$ | V | 1 |
| SET | | Set T in SREG | $T \leftarrow 1$ | T | 1 |
| CLT | | Clear T in SREG | $T \leftarrow 0$ | T | 1 |
| SEH | | Set Half Carry Flag in SREG | $H \leftarrow 1$ | H | 1 |
| CLH | | Clear Half Carry Flag in SREG | $H \leftarrow 0$ | H | 1 |
| DATA TRANSFER INSTRUCTIONS | | | | | |
| MOV | Rd, Rr | Move Between Registers | $Rd \leftarrow Rr$ | None | 1 |
| MOVW | Rd, Rr | Copy Register Word | $Rd+1:Rd \leftarrow Rr+1:Rr$ | None | 1 |
| LDI | Rd, K | Load Immediate | $Rd \leftarrow K$ | None | 1 |
| LD | Rd, X | Load Indirect | $Rd \leftarrow (X)$ | None | 2 |
| LD | Rd, X+ | Load Indirect and Post-Inc. | $Rd \leftarrow (X), X \leftarrow X + 1$ | None | 2 |
| LD | Rd, -X | Load Indirect and Pre-Dec. | $X \leftarrow X - 1, Rd \leftarrow (X)$ | None | 2 |
| LD | Rd, Y | Load Indirect | $Rd \leftarrow (Y)$ | None | 2 |
| LD | Rd, Y+ | Load Indirect and Post-Inc. | $Rd \leftarrow (Y), Y \leftarrow Y + 1$ | None | 2 |
| LD | Rd, -Y | Load Indirect and Pre-Dec. | $Y \leftarrow Y - 1, Rd \leftarrow (Y)$ | None | 2 |
| LDD | Rd, Y+q | Load Indirect with Displacement | $Rd \leftarrow (Y + q)$ | None | 2 |
| LD | Rd, Z | Load Indirect | $Rd \leftarrow (Z)$ | None | 2 |
| LD | Rd, Z+ | Load Indirect and Post-Inc. | $Rd \leftarrow (Z), Z \leftarrow Z + 1$ | None | 2 |
| LD | Rd, -Z | Load Indirect and Pre-Dec. | $Z \leftarrow Z - 1, Rd \leftarrow (Z)$ | None | 2 |
| LDD | Rd, Z+q | Load Indirect with Displacement | $Rd \leftarrow (Z + q)$ | None | 2 |
| LDS | Rd, k | Load Direct from SRAM | $Rd \leftarrow (k)$ | None | 2 |
| ST | X, Rr | Store Indirect | $(X) \leftarrow Rr$ | None | 2 |
| ST | X+, Rr | Store Indirect and Post-Inc. | $(X) \leftarrow Rr, X \leftarrow X + 1$ | None | 2 |
| ST | -X, Rr | Store Indirect and Pre-Dec. | $X \leftarrow X - 1, (X) \leftarrow Rr$ | None | 2 |
| ST | Y, Rr | Store Indirect | $(Y) \leftarrow Rr$ | None | 2 |
| ST | Y+, Rr | Store Indirect and Post-Inc. | $(Y) \leftarrow Rr, Y \leftarrow Y + 1$ | None | 2 |
| ST | -Y, Rr | Store Indirect and Pre-Dec. | $Y \leftarrow Y - 1, (Y) \leftarrow Rr$ | None | 2 |
| STD | Y+q, Rr | Store Indirect with Displacement | $(Y + q) \leftarrow Rr$ | None | 2 |
| ST | Z, Rr | Store Indirect | $(Z) \leftarrow Rr$ | None | 2 |
| ST | Z+, Rr | Store Indirect and Post-Inc. | $(Z) \leftarrow Rr, Z \leftarrow Z + 1$ | None | 2 |
| ST | -Z, Rr | Store Indirect and Pre-Dec. | $Z \leftarrow Z - 1, (Z) \leftarrow Rr$ | None | 2 |
| STD | Z+q, Rr | Store Indirect with Displacement | $(Z + q) \leftarrow Rr$ | None | 2 |
| STS | k, Rr | Store Direct to SRAM | $(k) \leftarrow Rr$ | None | 2 |
| LPM | | Load Program Memory | $R0 \leftarrow (Z)$ | None | 3 |
| LPM | Rd, Z | Load Program Memory | $Rd \leftarrow (Z)$ | None | 3 |
| LPM | Rd, Z+ | Load Program Memory and Post-Inc | $Rd \leftarrow (Z), Z \leftarrow Z + 1$ | None | 3 |
| SPM | | Store Program Memory | $(z) \leftarrow R1:R0$ | None | |
| IN | Rd, P | In Port | $Rd \leftarrow P$ | None | 1 |
| OUT | P, Rr | Out Port | $P \leftarrow Rr$ | None | 1 |
| PUSH | Rr | Push Register on Stack | $STACK \leftarrow Rr$ | None | 2 |
| POP | Rd | Pop Register from Stack | $Rd \leftarrow STACK$ | None | 2 |
| MCU CONTROL INSTRUCTIONS | | | | | |
| NOP | | No Operation | | None | 1 |
| SLEEP | | Sleep | (see specific descr. for Sleep function) | None | 1 |
| WDR | | Watchdog Reset | (see specific descr. for WDR/Timer) | None | 1 |
| BREAK | | Break | For On-chip Debug Only | None | N/A |

6. Ordering Information

6.1 ATtiny24A

| Speed (MHz) | Power Supply | Ordering Code ⁽¹⁾ | Package ⁽²⁾ | Operational Range |
|-------------|--------------|--|------------------------------|-------------------------------|
| 20 | 1.8 - 5.5V | ATtiny24A-SSU ATtiny24A-PU ATtiny24A-MU ATtiny24A-MMH | 14S1 14P3 20M1 20M2 | Industrial (-40°C to 85°C) |

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

| Package Type | |
|--------------|---|
| 14S1 | 14-lead, 0.150" Wide Body, Plastic Gull Wing Small Outline Package (SOIC) |
| 14P3 | 14-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| 20M1 | 20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No Lead / Micro Lead Frame Package (QFN/MLF) |
| 20M2 | 20-pad, 3 x 3 x 0.85 mm Body, Very Thin Quad Flat No Lead Package (VQFN) |



6.2 ATtiny44A

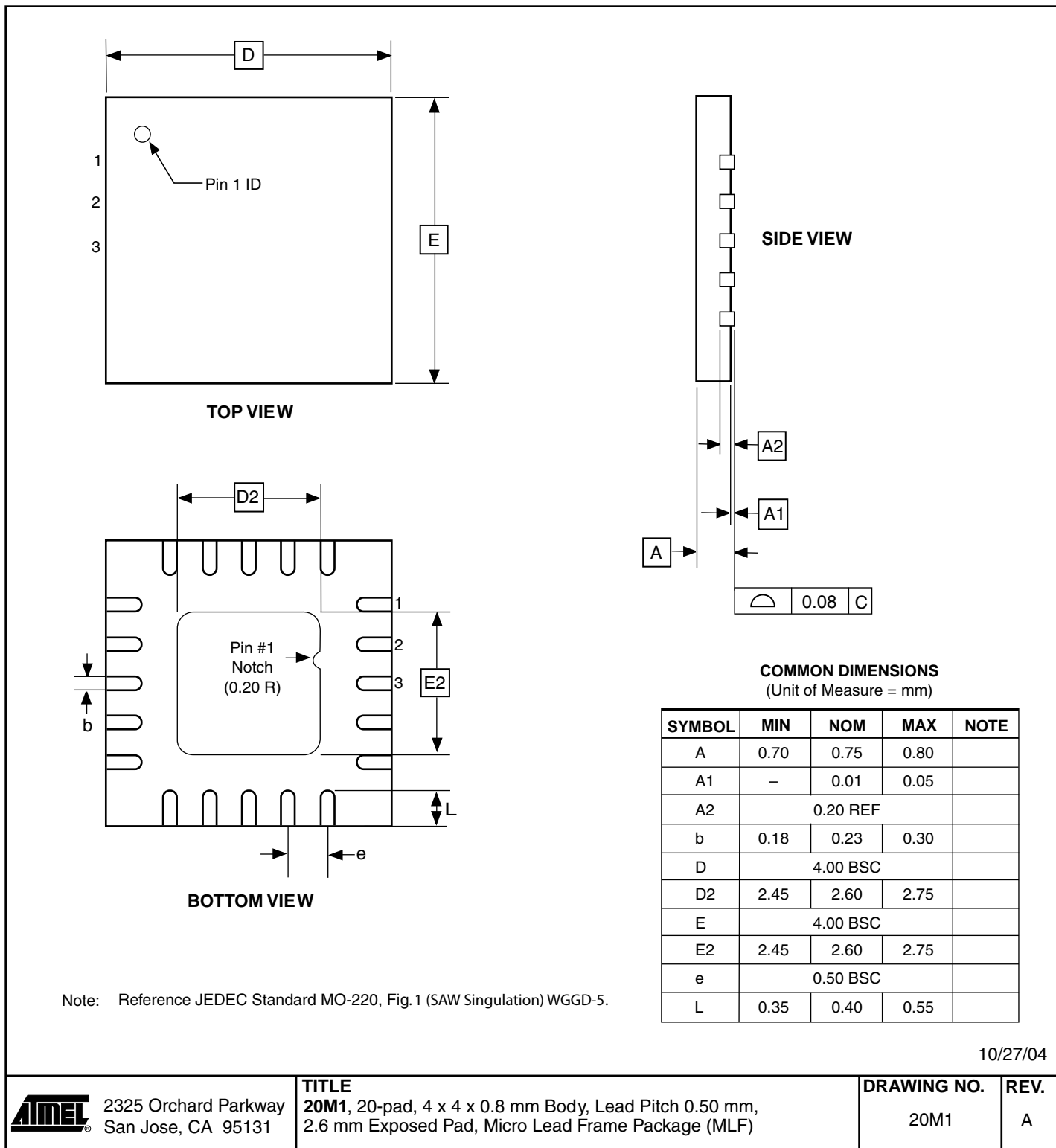
| Speed (MHz) | Power Supply | Ordering Code ⁽¹⁾ | Package ⁽²⁾ | Operational Range |
|-------------|--------------|--|------------------------------|-------------------------------|
| 20 | 1.8 - 5.5V | ATtiny44A-SSU ATtiny44A-PU ATtiny44A-MU ATtiny44A-MMH | 14S1 14P3 20M1 20M2 | Industrial (-40°C to 85°C) |

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

| Package Type | |
|--------------|---|
| 14S1 | 14-lead, 0.150" Wide Body, Plastic Gull Wing Small Outline Package (SOIC) |
| 14P3 | 14-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| 20M1 | 20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF) |
| 20M2 | 20-pad, 3 x 3 x 0.85 mm Body, Very Thin Quad Flat No Lead Package (VQFN) |

7. Packaging Information

7.1 20M1



10/27/04



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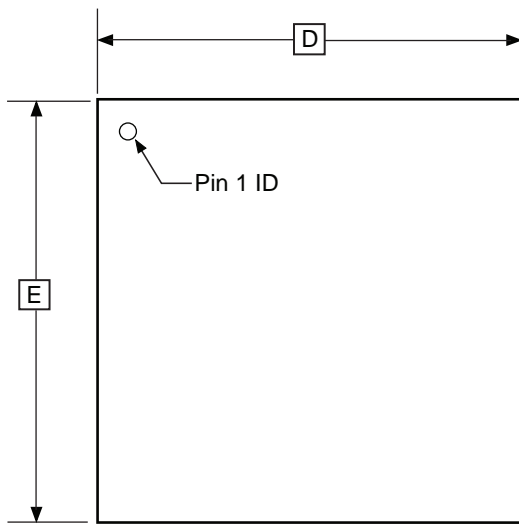
TITLE
20M1, 20-pad, 4 x 4 x 0.8 mm Body, Lead Pitch 0.50 mm,
2.6 mm Exposed Pad, Micro Lead Frame Package (MLF)

DRAWING NO.
20M1

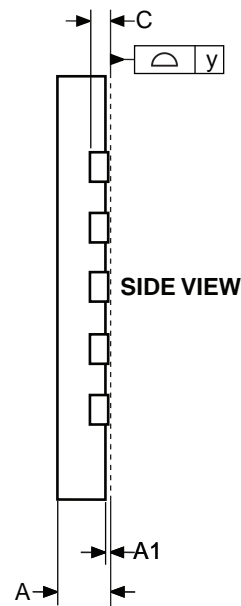
REV.
A



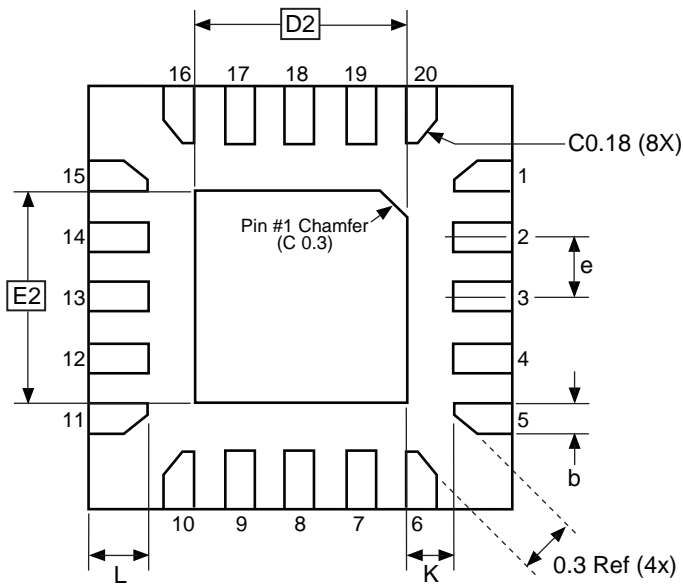
7.2 20M2



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-------|------|------|------|
| A | 0.75 | 0.80 | 0.85 | |
| A1 | 0.00 | 0.02 | 0.05 | |
| b | 0.17 | 0.22 | 0.27 | |
| C | 0.152 | | | |
| D | 2.90 | 3.00 | 3.10 | |
| D2 | 1.40 | 1.55 | 1.70 | |
| E | 2.90 | 3.00 | 3.10 | |
| E2 | 1.40 | 1.55 | 1.70 | |
| e | - | 0.45 | - | |
| L | 0.35 | 0.40 | 0.45 | |
| K | 0.20 | - | - | |
| y | 0.00 | - | 0.08 | |

10/24/08



Package Drawing Contact:
packagedrawings@atmel.com

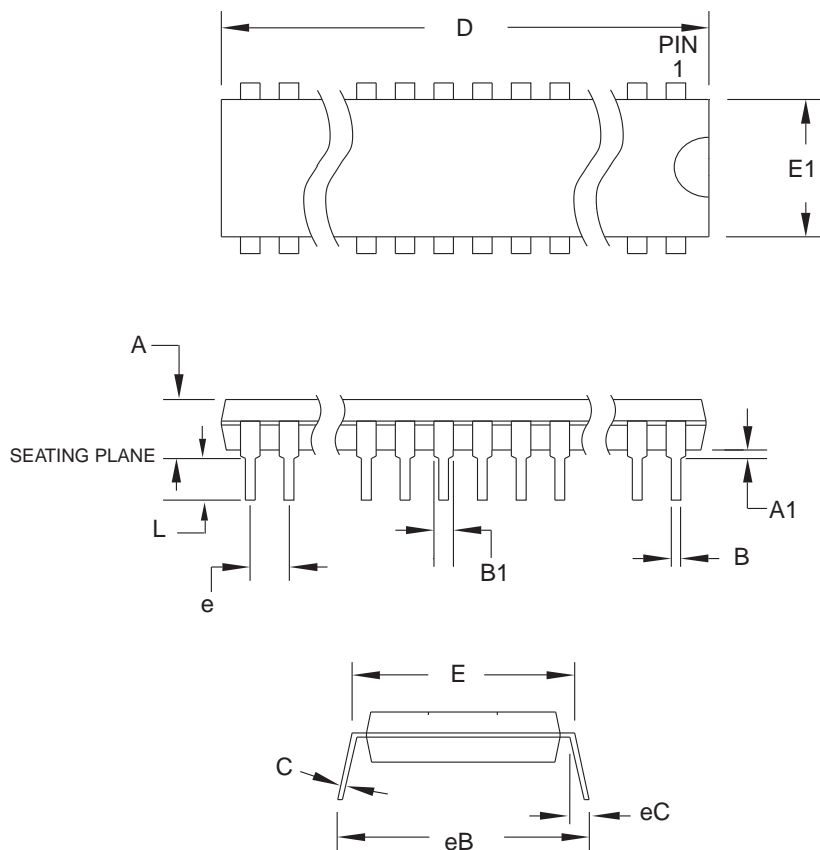
TITLE
20M2, 20-pad, 3 x 3 x 0.85 mm Body, Lead Pitch 0.45 mm,
1.55 x 1.55 mm Exposed Pad, Thermally Enhanced
Plastic Very Thin Quad Flat No Lead Package (VQFN)

GPC
ZFC

DRAWING NO.
20M2

REV.
B

7.3 14P3



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----------|-----|--------|--------|
| A | – | – | 5.334 | |
| A1 | 0.381 | – | – | |
| D | 18.669 | – | 19.685 | Note 2 |
| E | 7.620 | – | 8.255 | |
| E1 | 6.096 | – | 7.112 | Note 2 |
| B | 0.356 | – | 0.559 | |
| B1 | 1.143 | – | 1.778 | |
| L | 2.921 | – | 3.810 | |
| C | 0.203 | – | 0.356 | |
| eB | – | – | 10.922 | |
| eC | 0.000 | – | 1.524 | |
| e | 2.540 TYP | | | |

- Notes: 1. This package conforms to JEDEC reference MS-001, Variation AA.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

11/02/05



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TITLE

14P3, 14-lead (0.300"/7.62 mm Wide) Plastic Dual In-line Package (PDIP)

DRAWING NO.

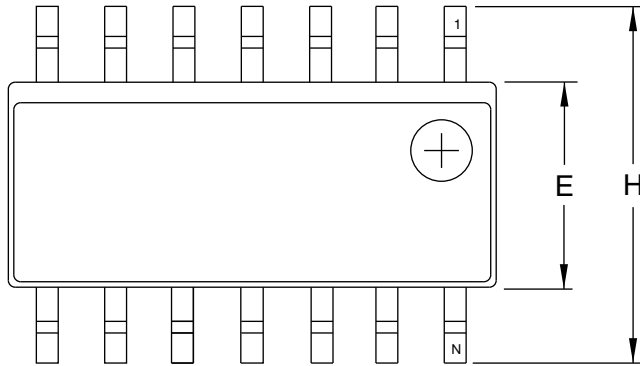
14P3

REV.

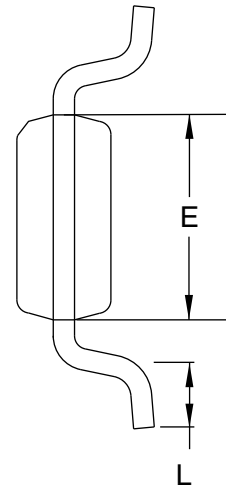
A



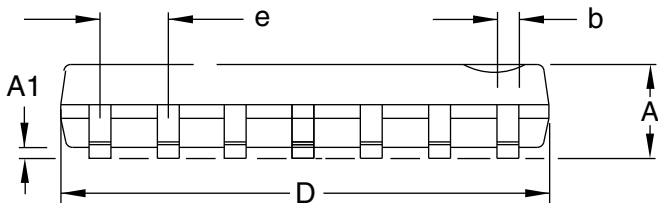
7.4 14S1



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm/inches)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|----------------|-----|-------------|------|
| A | 1.35/0.0532 | – | 1.75/0.0688 | |
| A1 | 0.1/0.0040 | – | 0.25/0.0098 | |
| b | 0.33/0.0130 | – | 0.5/0.02005 | |
| D | 8.55/0.3367 | – | 8.74/0.3444 | 2 |
| E | 3.8/0.1497 | – | 3.99/0.1574 | 3 |
| H | 5.8/0.2284 | – | 6.19/0.2440 | |
| L | 0.41/0.0160 | – | 1.27/0.0500 | 4 |
| e | 1.27/0.050 BSC | | | |

- Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-012, Variation AB for additional information.
 2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusion and gate burrs shall not exceed 0.15 mm (0.006") per side.
 3. Dimension E does not include inter-lead Flash or protrusion. Inter-lead flash and protrusions shall not exceed 0.25 mm (0.010") per side.
 4. L is the length of the terminal for soldering to a substrate.
 5. The lead width B, as measured 0.36 mm (0.014") or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024") per side.

2/5/02



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TITLE

14S1, 14-lead, 0.150" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)

DRAWING NO.

14S1

REV.

A

8. Errata

The revision letters in this section refer to the revision of the corresponding ATtiny24A/44A device.

8.1 ATtiny24A

8.1.1 Rev. G

Not sampled.

8.1.2 Rev. F

Not sampled.



8.2 ATtiny44A

8.2.1 Rev. F

No known errata.

8.2.2 Rev. E

Not sampled.

9. Datasheet Revision History

9.1 Rev A. 12/08

1. Initial revision. Created from document 8006H.
2. Updated "Ordering Information" on [page 17](#) and [page 18](#). Pb-plated packages are no longer offered and there are no separate ordering codes for commercial operation range, the only available option now is industrial. Also, updated some order codes to reflect changes in leadframe composition and added VQFN package option.
3. Updated data sheet template.
4. Removed all references to 8K device.
5. Updated characteristic plots of section "Typical Characteristics", starting on [page 182](#).
6. Added characteristic plots:
 - "Internal Bandgap Voltage vs. Supply Voltage" on [page 202](#)
 - "Internal Bandgap Voltage vs. Temperature" on [page 202](#)
7. Updated sections:
 - "Features" on [page 1](#)
 - "Power Reduction Register" on [page 34](#)
 - "Analog Comparator" on [page 128](#)
 - "Features" on [page 132](#)
 - "Operation" on [page 133](#)
 - "Starting a Conversion" on [page 134](#)
 - "ADC Voltage Reference" on [page 139](#)
 - "Speed Grades" on [page 174](#)
8. Updated Figures:
 - "Program Memory Map" on [page 15](#)
 - "Data Memory Map" on [page 16](#)
9. Update Tables:
 - "Device Signature Bytes" on [page 161](#)
 - "DC Characteristics. $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ " on [page 173](#)
 - "Additional Current Consumption for the different I/O modules (absolute values)" on [page 182](#)
 - "Additional Current Consumption (percentage) in Active and Idle mode" on [page 183](#)

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