Advance Information

MC9328MX1/D
Rev. 0, 06/2002

MC9328MX1, 1.8 V (DragonBall™ MX1) Integrated Portable System Processor

Contents Listing

1 Introduction

Motorola’s DragonBall™ family of microprocessors has demonstrated leadership in the portable handheld market. Continuing this legacy, the DragonBall MX (Media Extensions) series provides a leap in performance with an ARM9™ microprocessor core and highly integrated system functions. DragonBall MX products specifically address the requirements of the personal, portable product market by providing intelligent integrated peripherals, an advanced processor core, and power management capabilities.

The new MC9328MX1 features the advanced and power-efficient ARM920T™ core that operates at speeds up to 200 MHz. Integrated modules, which include an LCD controller, static RAM, USB support, an A/D converter (with touch panel control), and an MMC/SD host controller, support a suite of peripherals to enhance any product seeking to provide a rich multimedia experience. In addition, the MC9328MX1 is the first Bluetooth™ technology-ready applications processor. It is packaged in a 256-pin Mold Array Process-Ball Grid Array (MAPBGA).

Figure 1 on page 2 shows a functional block diagram of the MC9328MX1 and includes feature comparisons with existing DragonBall processors.

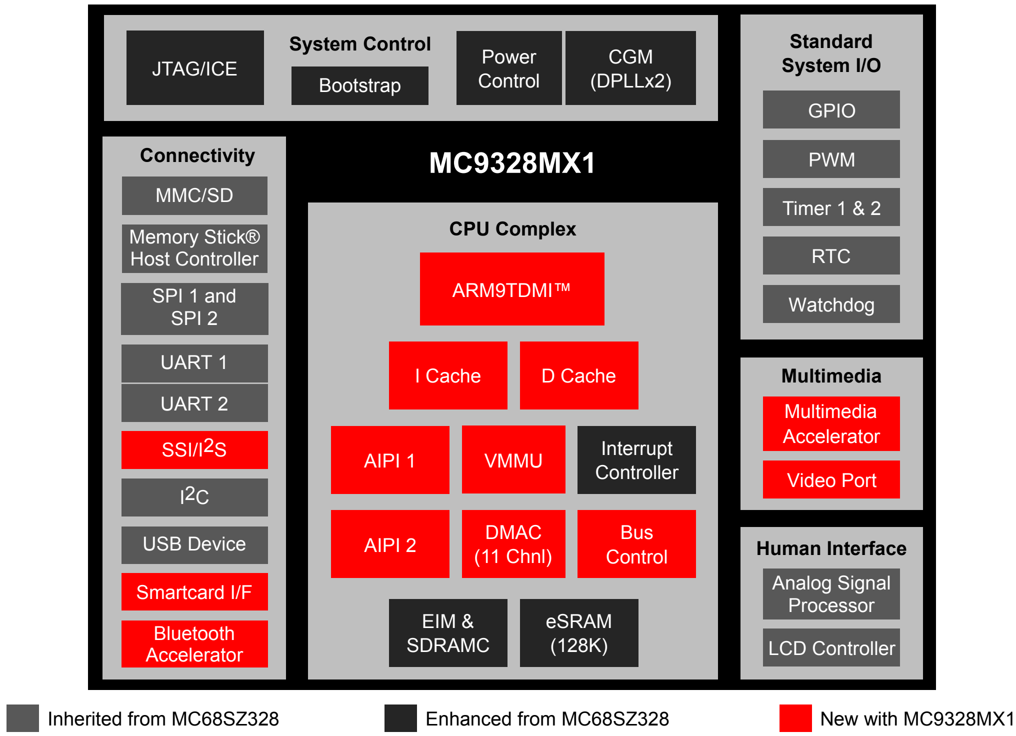


Figure 1. MC9328MX1 Functional Block Diagram

1.1 Conventions

This reference manual uses the following conventions:

- $\overline{\text{OVERBAR}}$ is used to indicate a signal that is active when pulled low: for example, $\overline{\text{RESET}}$.
- *Logic level one* is a voltage that corresponds to Boolean true (1) state.
- *Logic level zero* is a voltage that corresponds to Boolean false (0) state.
- To *set* a bit or bits means to establish logic level one.
- To *clear* a bit or bits means to establish logic level zero.
- A *signal* is an electronic construct whose state conveys or changes in state convey information.
- A *pin* is an external physical connection. The same pin can be used to connect a number of signals.
- *Asserted* means that a discrete signal is in active logic state.
  — *Active low* signals change from logic level one to logic level zero.
  — *Active high* signals change from logic level zero to logic level one.
- *Negated* means that an asserted discrete signal changes logic state.
  — *Active low* signals change from logic level zero to logic level one.
  — *Active high* signals change from logic level one to logic level zero.
- LSB means *least significant bit* or *bits*, and MSB means *most significant bit* or *bits*. References to low and high bytes or words are spelled out.
- Numbers preceded by a percent sign (%) are binary. Numbers preceded by a dollar sign ($) or *0x* are hexadecimal.

1.2 Features

To support a wide variety of applications, the MC9328MX1 provides a robust array of features, including the following:

- ARM920T Microprocessor Core
- AHB to IP Bus Interfaces (AIPIs)
- External Interface Module (EIM)
- SDRAM Controller (SDRAMC)
- Clock Generation Module (CGM) and Power Control Module
- Two Universal Asynchronous Receiver/Transmitters (UART 1 and UART 2)
- Two Serial Peripheral Interfaces (SPI)
- Two General-Purpose 32-bit Counters/Timers
- Watchdog Timer
- Real-Time Clock/Sampling Timer (RTC)
- LCD Controller (LCDC)
- Pulse-Width Modulation (PWM) Module
- Universal Serial Bus (USB) Device
- Multimedia Card and Secure Digital (MMC/SD) Host Controller Module
- Memory Stick® Host Controller (MSHC)
- Smartcard Interface Module (SIM)
- Direct Memory Access Controller (DMAC)
- Synchronous Serial Interface and Inter-IC Sound (SSI/I^2S) Module
- Inter-IC (I^2C) Bus Module
- Video Port
- General-Purpose I/O (GPIO) Ports
- Bootstrap Mode
- Analog Signal Processing (ASP) Module
- Bluetooth Accelerator (BTA)
- Multimedia Accelerator (MMA)
- 256-pin MAPBGA Package

1.3 Target Applications

The MC9328MX1 is targeted for advanced information appliances, smart phones, Web browsers, digital MP3 audio players, handheld computers based on the popular Palm OS platform, and messaging applications such as Motorola's wireless cellular products, including the Accompli™ 008 GSM/GPRS interactive communicator.

1.4 Product Documentation

The following documents are required for a complete description of the MC9328MX1 and are necessary to design properly with the device. Especially for those not familiar with the ARM920T processor or previous DragonBall products, the following documents will be helpful when used in conjunction with this manual.

ARM Architecture Reference Manual (ARM Ltd., order number ARM DDI 0100)

ARM9DT1 Data Sheet Manual (ARM Ltd., order number ARM DDI 0029)

ARM Technical Refines Manual (ARM Ltd., order number ARM DDI 0151C)

EMT9 Technical Reference Manual (ARM Ltd., order number DDI O157E)

MC9328MX1 Product Brief (order number MC9328MX1P/D)

MC9328MX1 Reference Manual (order number MC9328MX1RM/D)

MC68VZ328 Product Brief (order number MC68VZ328P/D)

MC68VZ328 User's Manual (order number MC68VZ328UM/D)

MC68VZ328 User's Manual Addendum (order number MC68VZ328UMAD/D)

MC68SZ328 Product Brief (order number MC68SZ328P/D)

MC68SZ328 User's Manual (order number MC68SZ328UM/D)

The Motorola manuals are available on the Motorola Semiconductors Web site at http://www.motorola.com/semiconductors. These documents may be downloaded directly from the Motorola Web site, or printed versions may be ordered. The ARM documentation is available from http://www.arm.com.

1.5 Ordering Information

Table 1 provides ordering information for the 256-lead mold array process ball grid array (MAPBGA) package.

Table 1. MC9328MX1 Ordering Information

Package Type	Frequency	Temperature	Order Number
256-lead MAPBGA	150 MHz	$0^{O}C$ to $70^{O}C$	PC9328MX1VH

2 Signals and Connections

Table 2 identifies and describes the MC9328MX1 signals that are assigned to package pins. The signals are grouped by the internal module that they are connected to.

Table 2. MC9328MX1 Signal Descriptions

Signal Name	Function/Notes
External Bus/Chip-Select (EIM)	
A [24:0]	Address bus signals
D [31:0]	Data bus signals

Table 2. MC9328MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
$\overline{\text{EB0}}$	MSB Byte Strobe—Active low external enable byte signal that controls D [31:24]
$\overline{\text{EB1}}$	Byte Strobe—Active low external enable byte signal that controls D [23:16]
$\overline{\text{EB2}}$	Byte Strobe—Active low external enable byte signal that controls D [15:8]
$\overline{\text{EB3}}$	LSB Byte Strobe—Active low external enable byte signal that controls D [7:0]
$\overline{\text{OE}}$	Memory Output Enable—Active low output enables external data bus
$\overline{\text{CS}}$ [5:0]	Chip-Select—The chip-select signals $\overline{\text{CS}}$ [3:2] are multiplexed with $\overline{\text{CSD}}$ [1:0] and are selected by the Function Multiplexing Control Register (FMCR). By default $\overline{\text{CSD}}$ [1:0] is selected.
$\overline{\text{ECB}}$	Active low input signal sent by a flash device to the EIM whenever the flash device must terminate an on-going burst sequence and initiate a new (long first access) burst sequence.
$\overline{\text{LBA}}$	Active low signal sent by a flash device causing the external burst device to latch the starting burst address.
BCLK	Clock signal sent to external synchronous memories (such as burst flash) during burst mode.
$\overline{\text{RW}}$	$\overline{\text{RW}}$ signal—Indicates whether external access is a read (high) or write (low) cycle. Used as a $\overline{\text{WE}}$ input signal by external DRAM.
Bootstrap	
BOOT [3:0]	System Boot Mode Select—The operational system boot mode of the MC9328MX1 upon system reset is determined by the settings of these pins.
SDRAM Controller	
SDBA [4:0]	SDRAM/SyncFlash non-interleave mode bank address multiplexed with address signals A [15:11]. These signals are logically equivalent to core address p_addr [25:21] in SDRAM/SyncFlash cycles.
SDIBA [3:0]	SDRAM/SyncFlash interleave addressing mode bank address multiplexed with address signals A [19:16]. These signals are logically equivalent to core address p_addr [12:9] in SDRAM/SyncFlash cycles.
MA [11:10]	SDRAM address signals
MA [9:0]	SDRAM address signals which are multiplexed with address signals A [10:1]. MA [9:0] are selected on SDRAM/SyncFlash cycles.
DQM [3:0]	SDRAM data enable
CSD0	SDRAM/SyncFlash Chip-select signal which is multiplexed with the $\overline{\text{CS2}}$ signal. These two signals are selectable by programming the system control register.
CSD1	SDRAM/SyncFlash Chip-select signal which is multiplexed with $\overline{\text{CS3}}$ signal. These two signals are selectable by programming the system control register. By default, $\overline{\text{CSD1}}$ is selected, so it can be used as SyncFlash boot chip-select by properly configuring BOOT [3:0] input pins.

Table 2. MC9328MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
RAS	SDRAM/SyncFlash Row Address Select signal
CAS	SDRAM/SyncFlash Column Address Select signal
SDWE	SDRAM/SyncFlash Write Enable signal
SDCKE0	SDRAM/SyncFlash Clock Enable 0
SDCKE1	SDRAM/SyncFlash Clock Enable 1
SDCLK	SDRAM/SyncFlash Clock
RESET_SF	SyncFlash Reset
Clocks and Resets	
EXTAL16M	Crystal input (4 MHz to 16 MHz), or a 16 MHz oscillator input when the internal oscillator circuit is shut down.
XTAL16M	Crystal output
EXTAL32K	32 KHz crystal input
XTAL32K	32 KHz crystal output
CLKO	Clock Out signal selected from internal clock signals.
RESET_IN	Master Reset—External active low Schmitt trigger input signal. When this signal goes active, all modules (except the reset module and the clock control module) are reset.
RESET_OUT	Reset Out—Internal active low output signal from the Watchdog Timer module and is asserted from the following sources: Power-on reset, External reset (RESET_IN), and Watchdog time-out.
POR	Power On Reset—Internal active high Schmitt trigger input signal. The POR signal is normally generated by an external RC circuit designed to detect a power-up event.
JTAG	
TRST	Test Reset Pin—External active low signal used to asynchronously initialize the JTAG controller.
TDO	Serial Output for test instructions and data. Changes on the falling edge of TCK.
TDI	Serial Input for test instructions and data. Sampled on the rising edge of TCK.
TCK	Test Clock to synchronize test logic and control register access through the JTAG port.
TMS	Test Mode Select to sequence the JTAG test controller's state machine. Sampled on the rising edge of TCK.
DMA	

Table 2. MC9328MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
BIG_ENDIAN	Big Endian—Input signal that determines the configuration of the external chip-select space. If it is driven logic-high at reset, the external chip-select space will be configured to little endian. If it is driven logic-low at reset, the external chip-select space will be configured to big endian.
ETM	
ETMTRACESYNC	ETM sync signal which is multiplexed with A24. ETMTRACESYNC is selected in ETM mode.
ETMTRACECLK	ETM clock signal which is multiplexed with A23. ETMTRACECLK is selected in ETM mode.
ETMPIPESTAT [2:0]	ETM status signals which are multiplexed with A [22:20]. ETMPIPESTAT [2:0] are selected in ETM mode.
ETMTRACEPKT [7:0]	ETM packet signals which are multiplexed with $\overline{ECB}$, $\overline{LBA}$, BCLK, PA17, A [19:16]. ETMTRACEPKT [7:0] are selected in ETM mode.
CMOS Sensor Interface	
CSI_D [7:0]	Sensor port data
CSI_MCLK	Sensor port master clock
CSI_VSYNC	Sensor port vertical sync
CSI_HSYNC	Sensor port horizontal sync
CSI_PIXCLK	Sensor port data latch clock
LCD Controller	
LD [15:0]	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
FLM/VSYNC	Frame Sync or Vsync—This signal also serves as the clock signal output for the gate driver (dedicated signal SPS for Sharp panel HR-TFT).
LP/HSYNC	Line pulse or H sync
LSCLK	Shift clock
ACD/OE	Alternate crystal direction/output enable
CONTRAST	This signal is used to control the LCD bias voltage as contrast control.
SPL_SPR	Program horizontal scan direction (Sharp panel dedicated signal).
PS	Control signal output for source driver (Sharp panel dedicated signal).
CLS	Start signal output for gate driver. This signal is an inverted version of PS (Sharp panel dedicated signal).
REV	Signal for common electrode driving signal preparation (Sharp panel dedicated signal).
SIM	

Table 2. MC9328MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
SIM_CLK	SIM Clock
SIM_RST	SIM Reset
SIM_RX	Receive Data
SIM_TX	Transmit Data
SIM_PD	Presence Detect Schmitt trigger input
SIM_SVEN	SIM Vdd Enable
SPI	
SPI1_MOSI	Master Out/Slave In
SPI1_MISO	Slave In/Master Out
SPI1_SS	Slave Select (Selectable polarity)
SPI1_SCLK	Serial Clock
SPI1_$\overline{\text{SPI_RDY}}$	Serial Data Ready
SPI2_TXD	SPI2 Master TxData Output—This signal is multiplexed with a GPI/O pin but does show up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the MC9328MX1 Reference Manual for information about how to bring this signal to the assigned pin.
SPI2_RXD	SPI2 master RxData input—This signal is multiplexed with a GPI/O pin but does show up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the MC9328MX1 Reference Manual for information about how to bring this signal to the assigned pin.
SPI2_$\overline{\text{SS}}$	SPI2 Slave Select—This signal is multiplexed with a GPI/O pin but does show up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the MC9328MX1 Reference Manual for information about how to bring this signal to the assigned pin.
SPI2_SCLK	SPI2 Serial Clock—This signal is multiplexed with a GPI/O pin but does show up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the MC9328MX1 Reference Manual for information about how to bring this signal to the assigned pin.
General Purpose Timers	
TIN	Timer Input Capture or Timer Input Clock—The signal on this input is applied to both timers simultaneously.
TMR2OUT	Timer 2 Output
USB Device	
USBD_VMO	USB Minus Output
USBD_VPO	USB Plus Output

Table 2. MC9328MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
USBD_VM	USB Minus Input
USBD_VP	USB Plus Input
USBD_SUSPND	USB Suspend Output
USBD_RCV	USB RxD
USBD_OE	USB $\overline{\text{OE}}$
USBD_AFE	USB Analog Front End Enable
Secure Digital Interface	
SD_CMD	SD Command—If the system designer does not wish to make use of the internal pull-up, via the Pull-up enable register, a 4.7K–69K external pull up resistor must be added.
SD_CLK	MMC Output Clock
SD_DAT [3:0]	Data—If the system designer does not wish to make use of the internal pull-up, via the Pull-up enable register, a 50K–69K external pull up resistor must be added
Memory Stick Interface	
MS_BS	Memory Stick Bus State (Output)—Serial bus control signal
MS_SDIO	Memory Stick Serial Data (Input/Output)
MS_SCLKO	Memory Stick External Clock (Input)—External clock source for SCLK Divider
MS_SCLKI	Memory Stick Serial Clock (Output)—Serial Protocol clock signal
MS_PI0	General purpose Input0—Can be used for Memory Stick Insertion/Extraction detect
MS_PI1	General purpose Input1—Can be used for Memory Stick Insertion/Extraction detect
UARTs – IrDA/Auto-Bauding	
UART1_RXD	Receive Data
UART1_TXD	Transmit Data
$\overline{\text{UART1\_RTS}}$	Request to Send
$\overline{\text{UART1\_CTS}}$	Clear to Send
UART2_RXD	Receive Data
UART2_TXD	Transmit Data
UART2_RTS	Request to Send
UART2_CTS	Clear to Send
UART2_DSR	Data Set Ready
UART2_RI	Ring Indicator

Table 2. MC9328MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
UART2_DCD	Data Carrier Detect
UART2_DTR	Data Terminal Ready
Serial Audio Port – SSI (configurable to I2S protocol)	
SSI_TXDAT	TxD
SSI_RXDAT	RxD
SSI_TXCLK	Transmit Serial Clock
SSI_RXCLK	Receive Serial Clock
SSI_TXFS	Transmit Frame Sync
SSI_RXFS	Receive Frame Sync
I^2C	
I2C_SCL	I^2C Clock
I2C_SDA	I^2C Data
PWM	
PWMO	PWM Output
ASP	
UIN	Positive U analog input (for low voltage, temperature measurement)
UIP	Negative U analog input (for low voltage, temperature measurement)
PX1	Positive pen-X analog input
PY1	Positive pen-Y analog input
PX2	Negative pen-X analog input
PY2	Negative pen-Y analog input
R1A	Positive resistance input (a)
R1B	Positive resistance input (b)
R2A	Negative resistance input (a)
R2B	Negative resistance input (b)
MIP	Positive voice analog input
MIM	Negative voice analog input
RVP	Positive reference for pen ADC
RVM	Negative reference for pen ADC

Table 2. MC9328MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
RVP1	Positive reference for voice ADC
RVM1	Negative reference for voice ADC
RP	Positive bandgap reference
RM	Negative bandgap reference
DAC_OP	Voice DAC positive output
DAC_OM	Voice DAC negative output
AVDD	Analog power supply
AGND	Analog ground
Bluetooth	
BT1	I/O clock signal
BT2	Output
BT3	Input
BT4	Input
BT5	Output
BT6	Output
BT7	Output
BT8	Output
BT9	Output
BT10	Output
BT11	Output
BT12	Output
BT13	Output
TRISTATE	Sets all I/O pins to tri-state; May be used for FLASH loading and is pulled low for normal operations.
BTRF VDD	Power supply from external BT RFIC
BTRF GND	Ground from external BT RFIC
Noisy Supply Pins	
NVDD	Noisy Supply for the I/O pins
NVSS	Noisy Ground for the I/O pins

Table 2. MC9328MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
Supply Pins – Analog Modules	
AVDD	Supply for analog blocks
AVSS	Quiet GND for analog blocks
Internal Power Supply	
QVDD	Power supply pins for silicon internal circuitry
QVSS	GND pins for silicon internal circuitry
Substrate Supply Pins	
SVDD	Supply routed through substrate of package; not to be bonded
SGND	Ground routed through substrate of package; not to be bonded

3 Specifications

This section contains the electrical specifications and timing diagrams for the MC9328MX1 processor.

3.1 Maximum Ratings

Table 3 provides information on maximum ratings.

Table 3. Maximum Ratings

Rating	Symbol	Minimum	Maximum	Unit
Supply voltage	V_{dd}	-0.3	3.3	V
Maximum operating temperature range	T_A	0	70	°C
Storage temperature	Test	-55	150	°C

3.2 Recommended Operating Range

Table 4 provides the recommended operating ranges for the supply voltages. MX1 has multiple pairs of VDD and VSS power supply and return pins. QVDD and QVSS pins are used for internal logic. All other VDD and VSS pins are for the I/O pads voltage supply, and each pair of VDD and VSS provides power to the enclosed I/O pads. This design allows different peripheral supply voltage levels in a system.

Since AVDD pins are supply voltages to the analog pads, it is suggested the AVDD pins are isolated or noise-filtered from the other VDD pins.

BTRFVDD is the supply voltage for the Bluetooth interface signals. It is quite sensitive to the data transmit/receive accuracy. Please refer to Bluetooth RF spec for special handling. If Bluetooth is not used in the system, these Bluetooth pins can be used as GPI/O and BTRFVDD can be treated like other NVDD pins.

For more information about I/O pads grouping per VDD, please refer to Table 2 on page 4.

Table 4. Recommended Operating Range

Rating	Symbol	Minimum	Maximum	Unit
I/O supply voltage, BTA, USBd, LCD and CSI are only 3v interface only	NVDD	2.70	3.3	V
I/O supply voltage	NVDD	1.70	1.90	V
Internal supply voltage	QVDD	1.70	1.90	V
Analog supply voltage	AVDD	1.70	1.90	V
Bluetooth I/O voltage (Bluetooth)	BTRFVDD	1.70	3.1	V
Bluetooth I/O voltage (Non Bluetooth applications)	BTRFVDD	1.70	3.3	V

3.3 DC Electrical Characteristics

Table 5 contains both maximum and minimum DC characteristics of the MC9328MX1.

Table 5. Maximum and Minimum DC Characteristics

Number or Symbol	Parameter	Minimum	Typical	Maximum	Unit
Iop	Full running operating current at 1.8V, 1.8V I/O (Core = 96 MHz, System = 96 MHz, program running in internal SRAM, cache disabled)	—	90	—	mA
Sidd	Standby current (VDD = 1.8V)	—	15	—	µA
V_{IH}	Input high voltage	$0.7V_{DD}$	—	Vdd+0.2	V
V_{IL}	Input low voltage	—	—	0.4	V
V_{OH}	Output high voltage (I_{OH} = 2.0 mA)	$0.7V_{DD}$	—	Vdd	V
V_{OL}	Output low voltage (I_{OL} = -2.5 mA)	—	—	0.4	V
I_{IL}	Input low leakage current (V_{IN} = GND, no pull-up or pull-down)	—	—	±1	µA
I_{IH}	Input high leakage current ($V_{IN} = V_{DD}$, no pull-up or pull-down)	—	—	±1	µA
I_{OH}	Output high current ($V_{OH} = 0.8V_{DD}$, V_{DD} = 1.8V)	4.0	—	—	mA

Table 5. Maximum and Minimum DC Characteristics (Continued)

Number or Symbol	Parameter	Minimum	Typical	Maximum	Unit
I_{OL}	Output low current (V_{OL} = 0.4V, V_{DD} = 1.8V)	—	—	-4.0	mA
I_{OZ}	Output leakage current (V_{out} = V_{DD}, output is tri-stated)	—	—	±5	µA

3.4 AC Electrical Characteristics

The AC characteristics consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of other signals. All timing specifications are specified at a system operating frequency from 0 MHz to 96 MHz (core operating frequency 150 MHz) with an operating supply voltage from $V_{DD\ min}$ to $V_{DD\ max}$ under an operating temperature from T_L to T_H. All timing is measured at pF loading.

3.5 Embedded Trace Macrocell

All registers in the ETM9 are programmed through a JTAG interface. The interface is an extension of the ARM920T processor’s TAP controller, and is assigned scan chain 6. The scan chain consists of a 40-bit shift register comprising:

- 32-bit data field
- 7-bit address field
- A read/write bit

The data to be written is scanned into the 32-bit data field, the address of the register into the 7-bit address field, and a 1 into the read/write bit.

A register is read by scanning its address into the address field and a 0 into the read/write bit. The 32-bit data field is ignored. A read or a write takes place when the TAP controller enters the UPDATE-DR state. The timing diagram for the ETM9 is shown in Figure 2. See Table 6 on page 15 for the ETM9 timing parameters used in Figure 2.

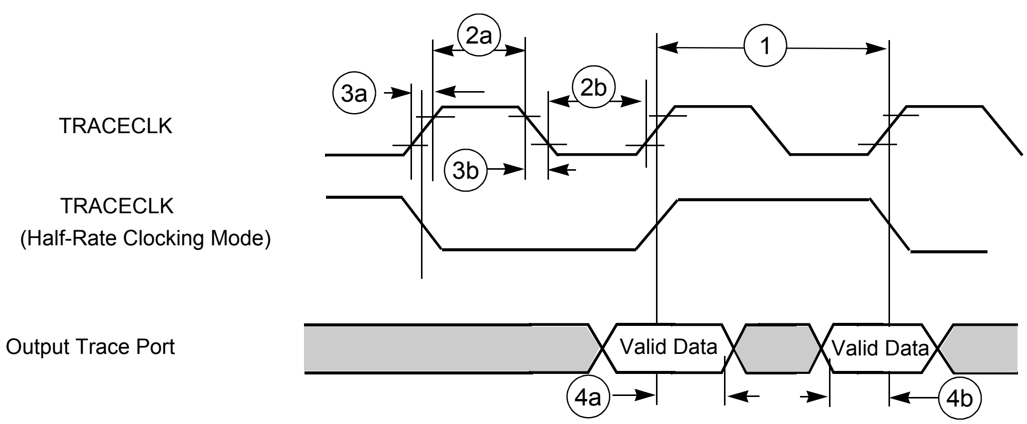


Figure 2. Trace Port Timing Diagram

Table 6. Trace Port Timing Diagram Parameter Table

Ref No.	Parameter	1.8 +/- 0.10V		Unit
		Minimum	Maximum	
1	CLK frequency	0	85	MHz
2a	Clock high time	1.3	—	ns
2b	Clock low time	3	—	ns
3a	Clock rise time	—	4	ns
3b	Clock fall time	—	3	ns
4a	Output hold time	2.28	—	ns
4b	Output setup time	3.42	—	ns

3.6 DPLL Timing Specifications

Parameters of the DPLL are given in Table 7. In this table, T_{ref} is a reference clock period after the pre-divider and T_{dck} is the output double clock period.

Table 7. DPLL Specifications

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
Reference clock freq range	Vcc = 1.8V	5	—	100	MHz
Pre-divider output clock freq range	Vcc = 1.8V	5	—	30	MHz
Double clock freq range	Vcc = 1.8V	80	—	220	MHz
Pre-divider factor (PD)	—	1	—	16	—
Total multiplication factor (MF)	Includes both integer and fractional parts	5	—	15	—
MF integer part	—	5	—	15	—
MF numerator	Should be less than the denominator	0	—	1022	—
MF denominator	—	1	—	1023	—
Freq lock-in time after full reset	FOL mode for non-integer MF	250	280 (56 µs)	300	T_{ref}
Freq lock-in time after partial reset	FOL mode or non-integer MF	220	250 (~50 µs)	270	T_{ref}
Phase lock-in time after full reset	FPL mode and integer MF	300	350 (70 µs)	400	T_{ref}

Table 7. DPLL Specifications (Continued)

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
Phase lock-in time after partial reset	FPL mode and integer MF	270	320 (64 µs)	370	T_{ref}
Freq jitter (p-p)	—	—	0.005 (0.01%)	0.01	$2 \bullet T_{dck}$
Phase jitter (p-p)	Integer MF, FPL mode, Vcc=1.8V	—	1.0 (10%)	1.5	ns
Power supply voltage	—	1.8	—	2.5	V
Power dissipation	FOL mode, integer MF, f_{dck} = 200 MHz, Vcc = 1.8V	—	—	4	mW

3.7 Reset Module

The timing relationships of the Reset module with the POR and $\overline{\text{RESET\_IN}}$ are shown in Figure 3 and Figure 4.

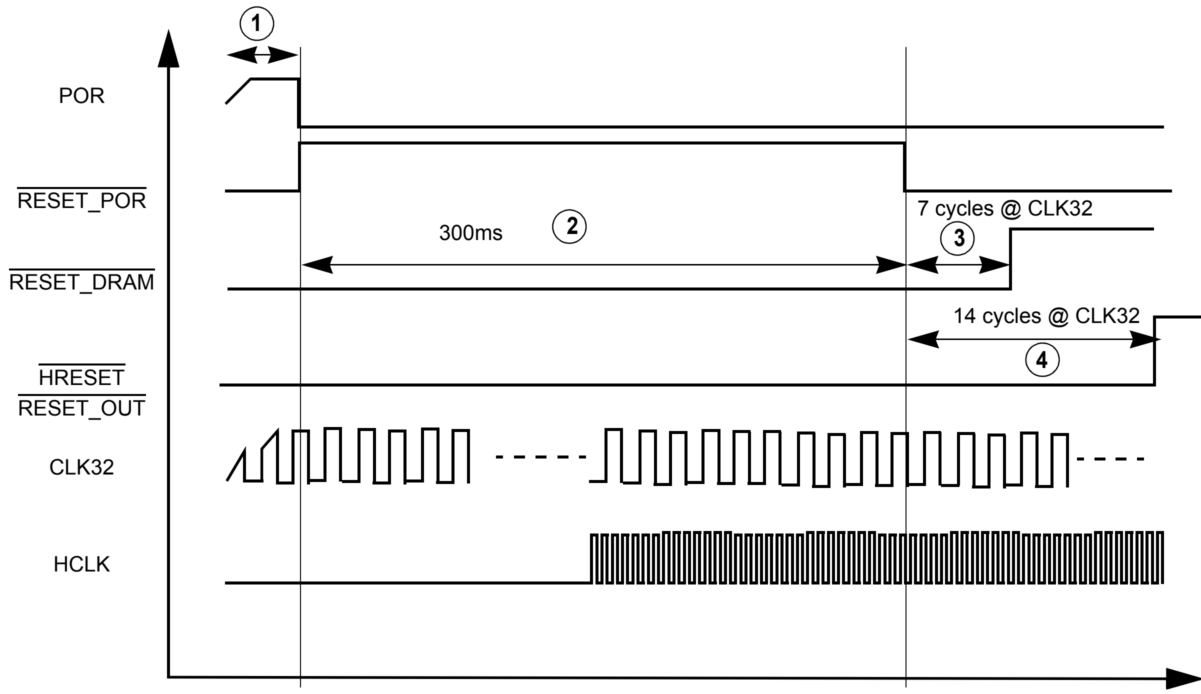


Figure 3. Timing Relationship with POR

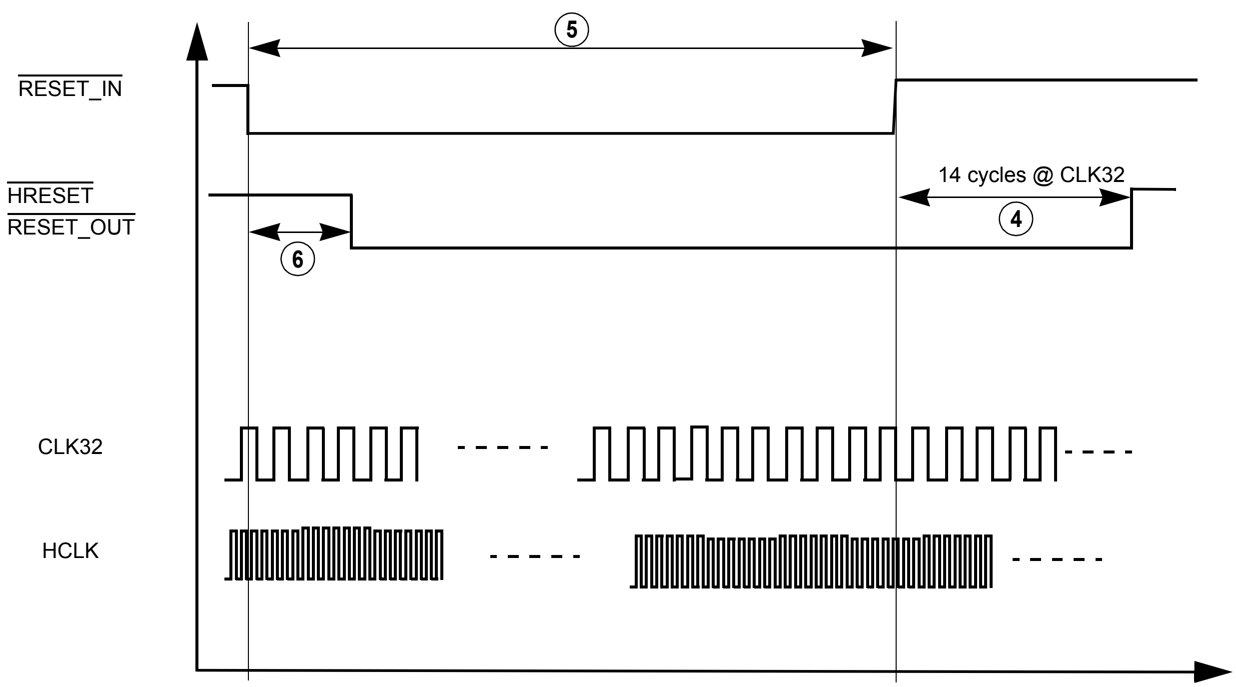


Figure 4. Timing Relationship with $\overline{\text{RESET\_IN}}$

Table 8. Reset Module Timing Parameter Table

Ref No.	Parameter	1.8 +/- 0.10V		Unit
		Minimum	Maximum	
1	Width of input POWER_ON_RESET	100	—	ns
2	Width of internal POWER_ON_RESET (CLK32 at 32 KHz)	300	300	ms
3	7K to 32K-cycle stretcher for SDRAM reset	7	7	cycles of CLK32
4	14K to 32K-cycle stretcher for internal system reset HRESERT and output reset at pin RESET_OUT	14	14	cycles of CLK32
5	Width of external hard-reset RESET_IN	4	—	cycles of CLK32
6	4K to 32K-cycle qualifier	4	4	cycles of CLK32

3.8 External Interface Module (EIM)

The External Interface Module (EIM) handles the interface to devices external to the MC9328MX1, including generation of chip-selects for external peripherals and memory. The timing diagram for the EIM is shown in Figure 5, and Table 9 defines the parameters of signals.

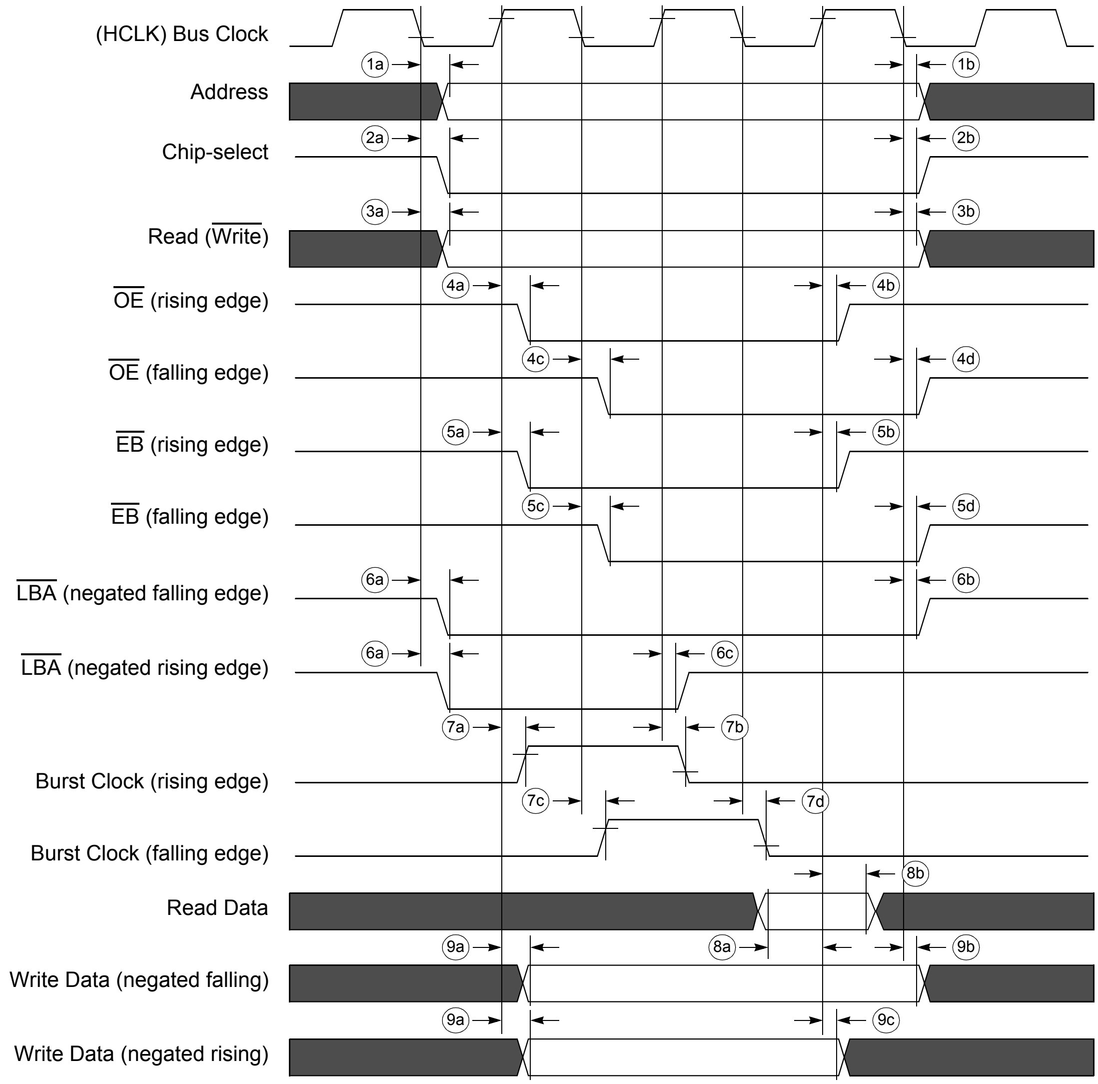


Figure 5. EIM Bus Timing Diagram

Table 9. EIM Bus Timing Parameter Table

Ref No.	Parameter	1.8 +/- 0.10V		Unit
		Minimum	Maximum	
1a	Clock fall to address valid	—	9.33	ns
1b	Clock fall to address invalid	3.40	—	ns
2a	Clock fall to chip-select valid	—	8.23	ns
2b	Clock fall to chip-select invalid	2.33	—	ns

Table 9. EIM Bus Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 +/- 0.10V		Unit
		Minimum	Maximum	
3a	Clock fall to Read ($\overline{\text{Write}}$) Valid	—	6.76	ns
3b	Clock fall to Read ($\overline{\text{Write}}$) Invalid	2.09	—	ns
4a	Clock[1] rise to Output Enable Valid	—	9.00	ns
4b	Clock[1] rise to Output Enable Invalid	3.48	—	ns
4c	Clock[1] fall to Output Enable Valid	—	9.00	ns
4d	Clock[1] fall to Output Enable Invalid	2.34	—	ns
5a	Clock[1] rise to Enable Bytes Valid	—	8.71	ns
5b	Clock[1] rise to Enable Bytes Invalid	2.76	—	ns
5c	Clock[1] fall to Enable Bytes Valid	—	8.71	ns
5d	Clock[1] fall to Enable Bytes Invalid	1.62	—	ns
6a	Clock[1] fall to Load Burst Address Valid	—	7.55	ns
6b	Clock[1] fall to Load Burst Address Invalid	1.89	—	ns
6c	Clock[1] rise to Load Burst Address Invalid	3.03	—	ns
7a	Clock[1] rise to Burst Clock rise	—	8.73	ns
7b	Clock[1]rise to Burst Clock fall	—	8.80	ns
7c	Clock[1] fall to Burst Clock rise	—	8.73	ns
7d	Clock[1] fall to Burst Clock fall	—	8.80	ns
8a	Read Data setup time	8.78	—	ns
8b	Read Data hold time	4.38	—	ns
9a	Clock[1] rise to Write Data Valid	—	7.25	ns
9b	Clock[1] fall to Write Data Invalid	0	—	ns
9c	Clock[1] rise to Write Data Invalid	1.62	—	ns

1. Clock refers to the system clock signal, HCLK, generated from the System PLL

3.9 EIM External Bus Timing Diagrams

The following timing diagrams show the timing of accesses to memory or a peripheral.

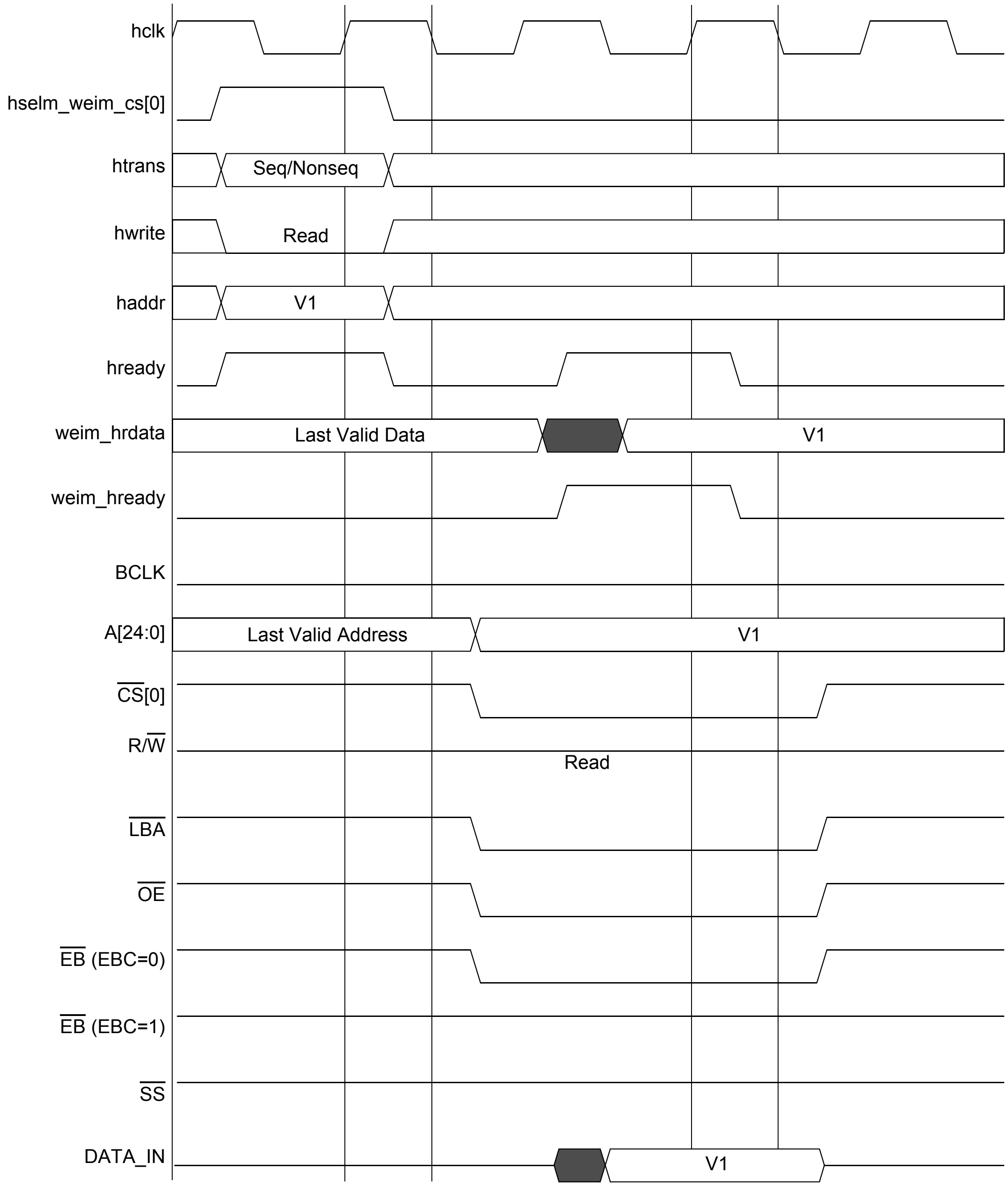


Figure 6. WSC = 1, A.HALF/E.HALF

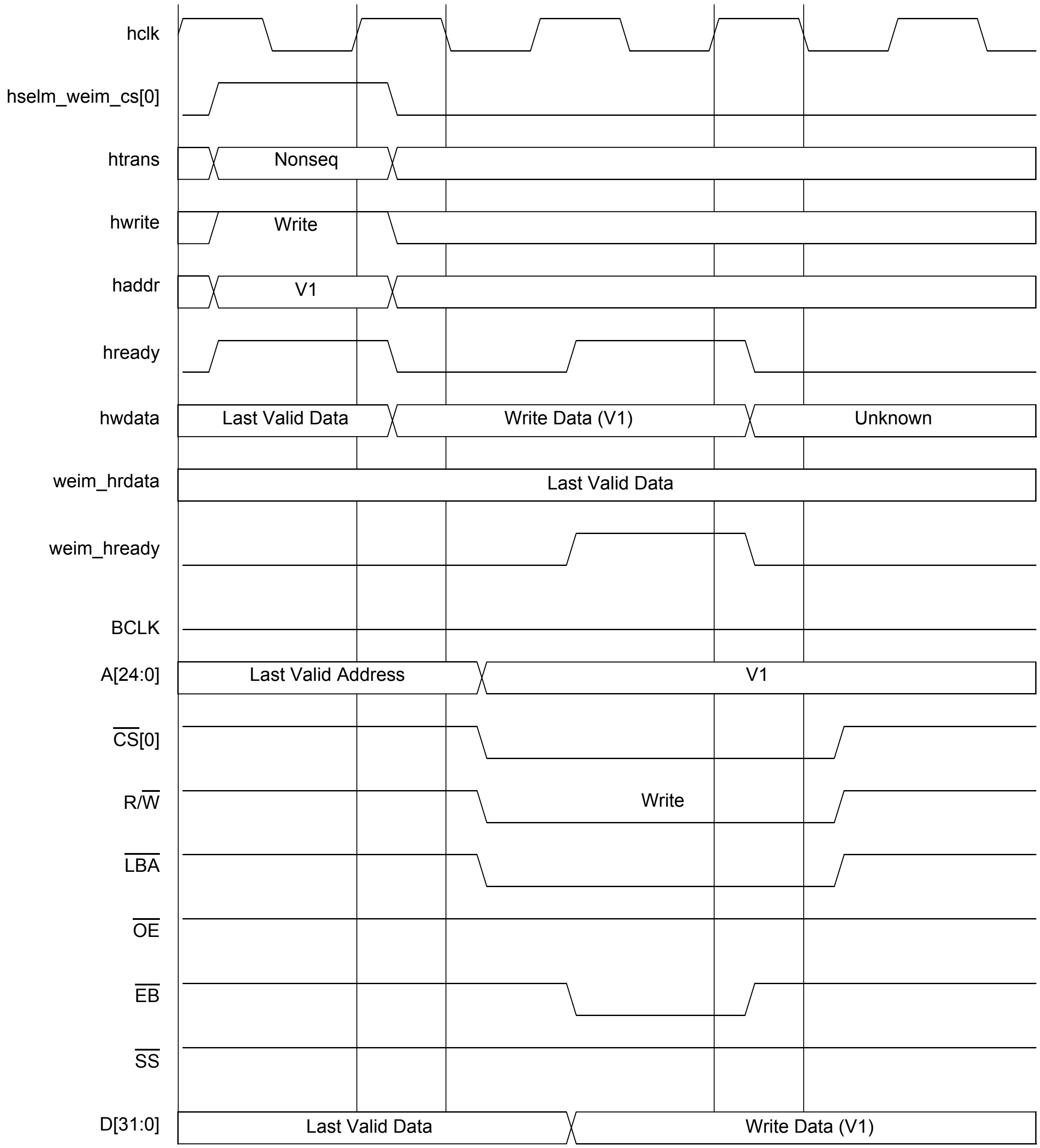


Figure 7. WSC = 1, WEA = 1, WEN = 1, A.HALF/E.HALF

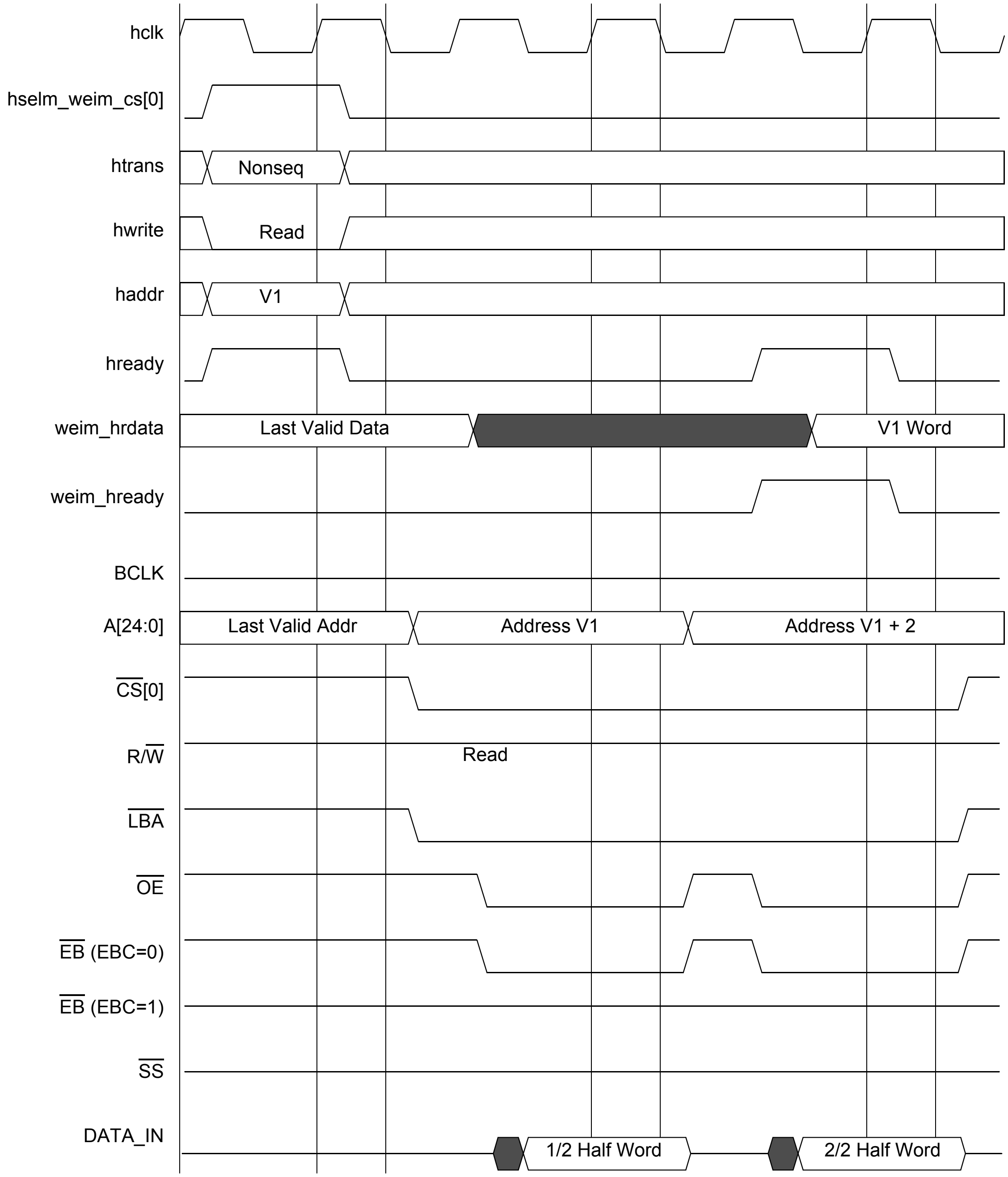


Figure 8. WSC = 1, OEA = 1, A.WORD/E.HALF

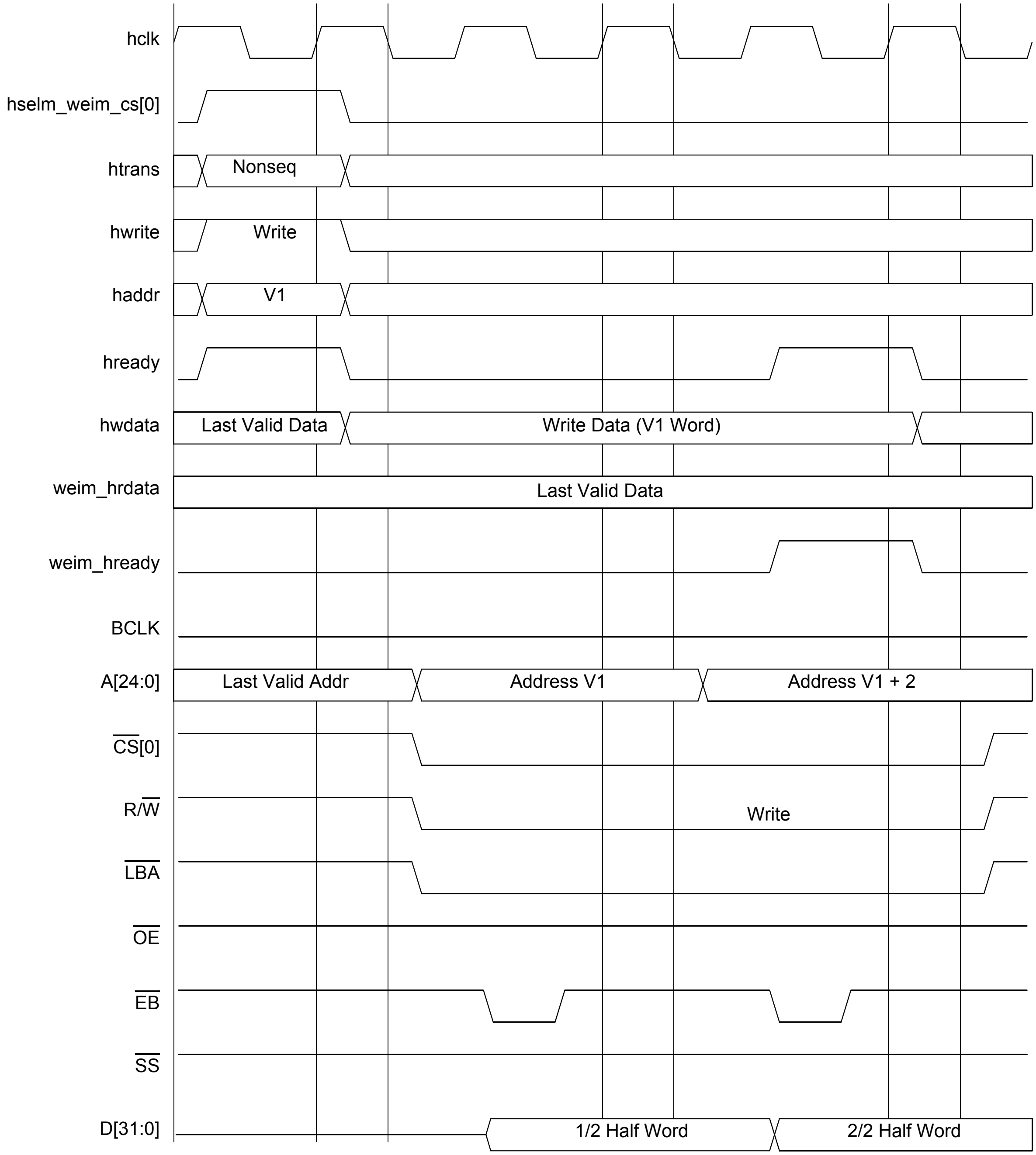


Figure 9. WSC = 1, WEA = 1, WEN = 2, A.WORD/E.HALF

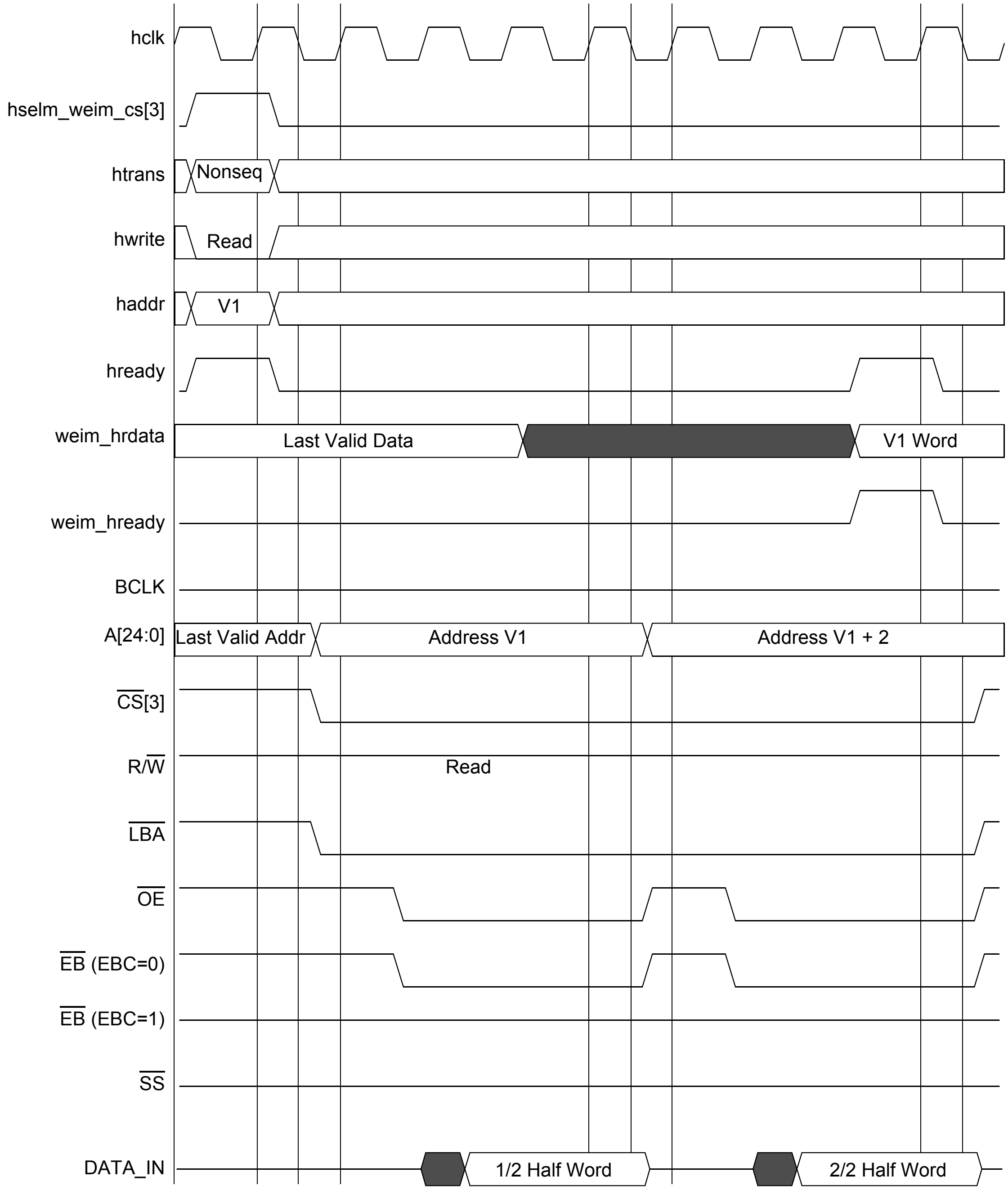


Figure 10. WSC = 3, OEA = 2, A.WORD/E.HALF

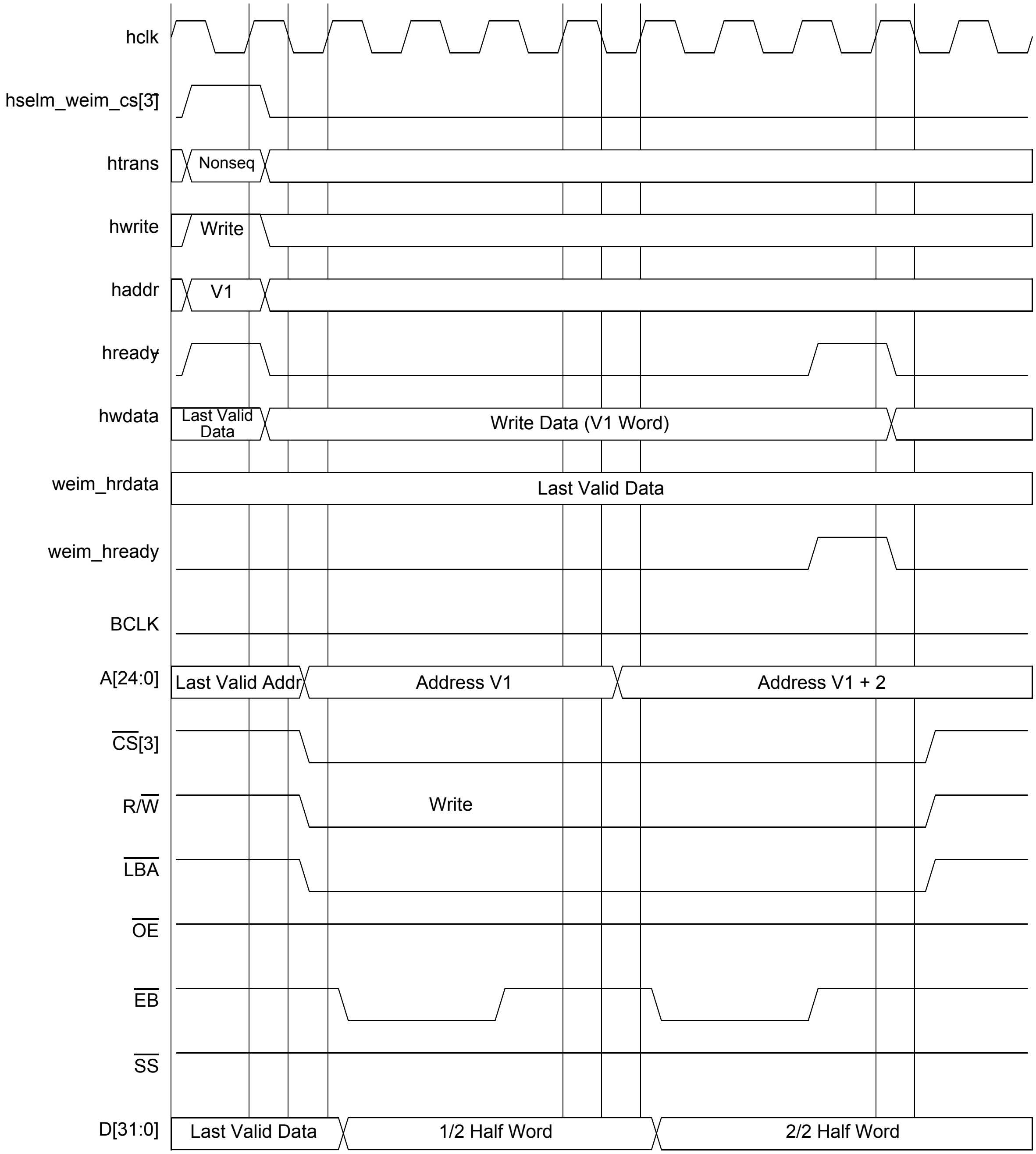


Figure 11. WSC = 3, WEA = 1, WEN = 3, A.WORD/E.HALF

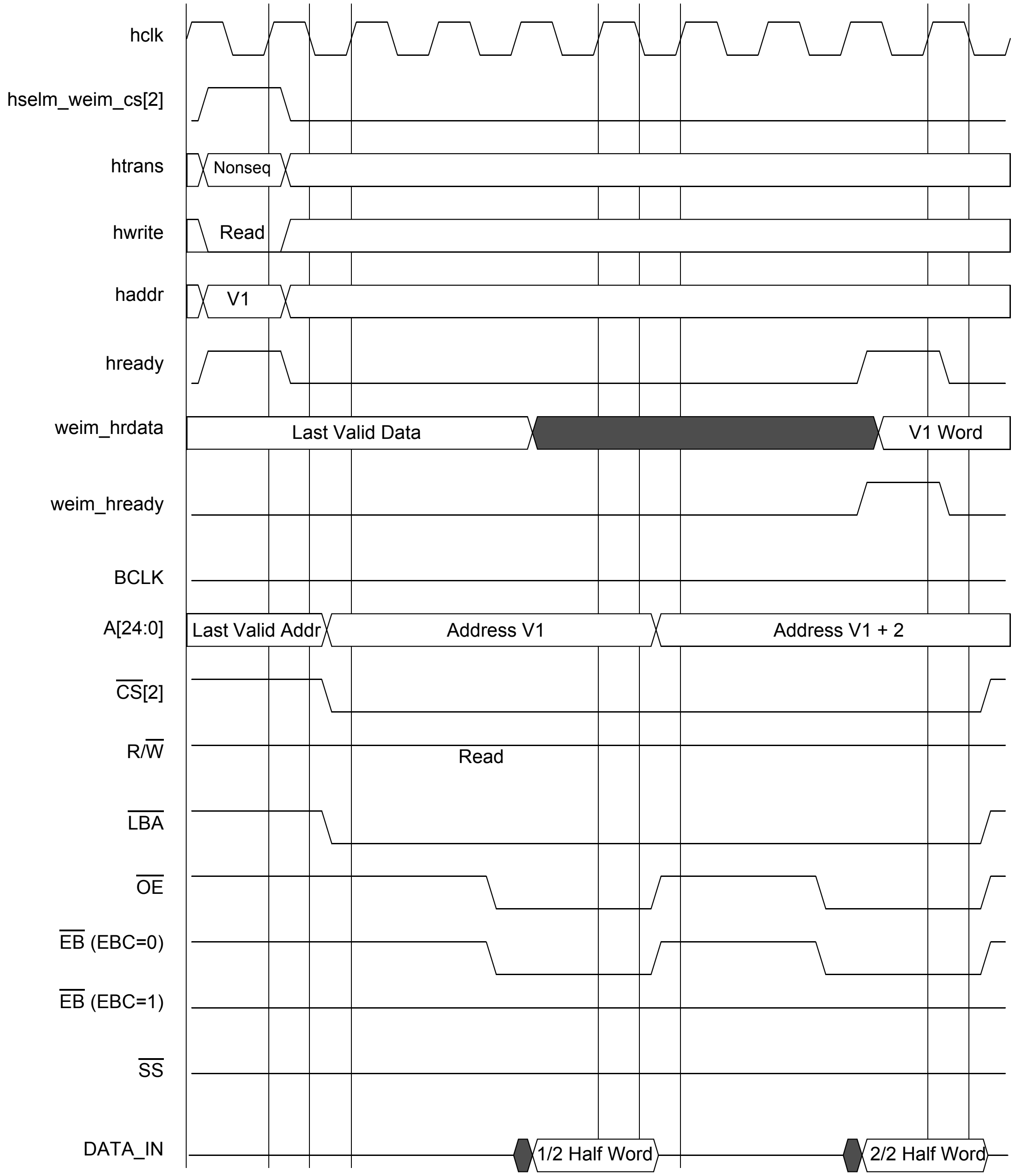


Figure 12. WSC = 3, OEA = 4, A.WORD/E.HALF

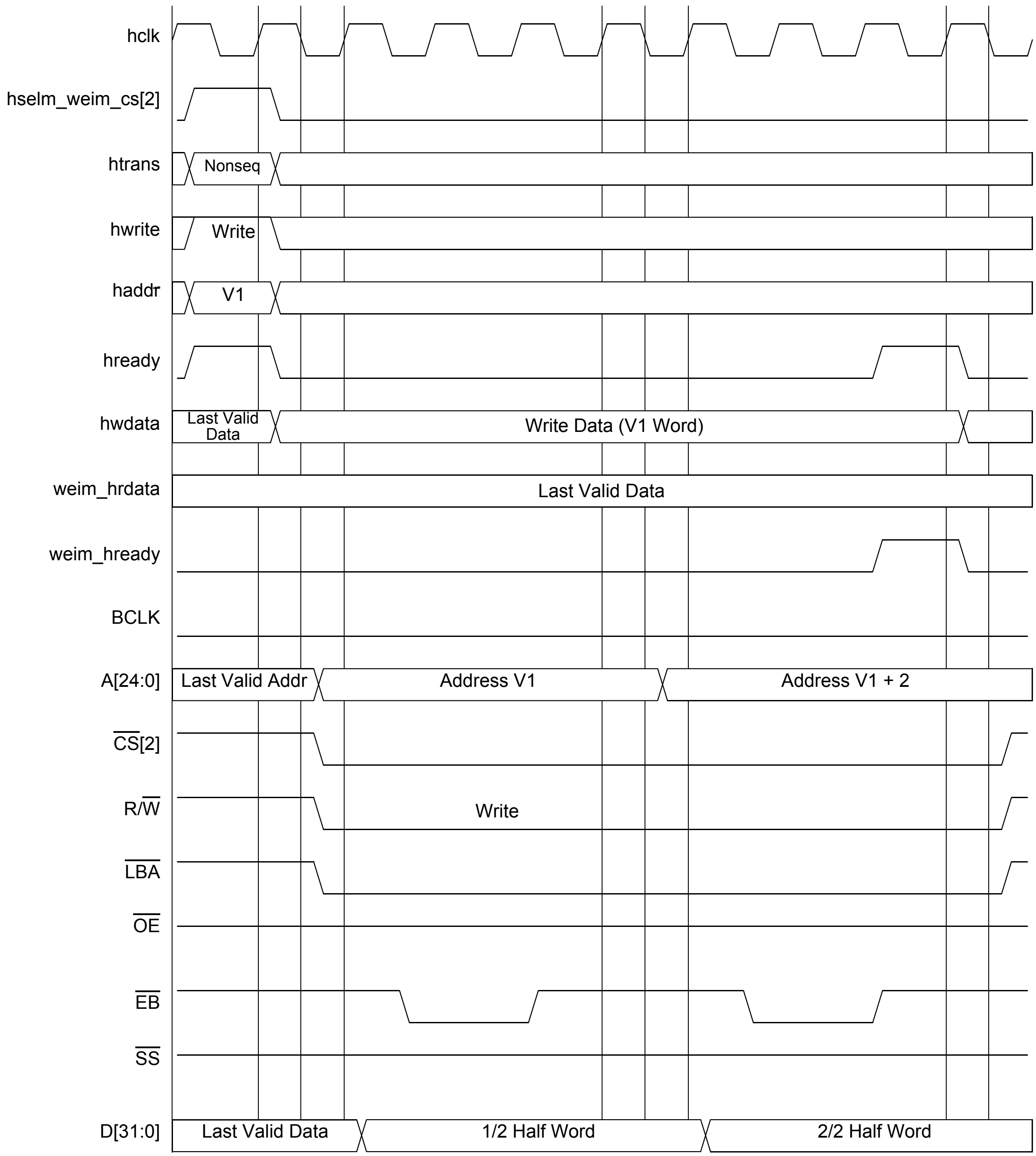


Figure 13. WSC = 3, WEA = 2, WEN = 3, A.WORD/E.HALF

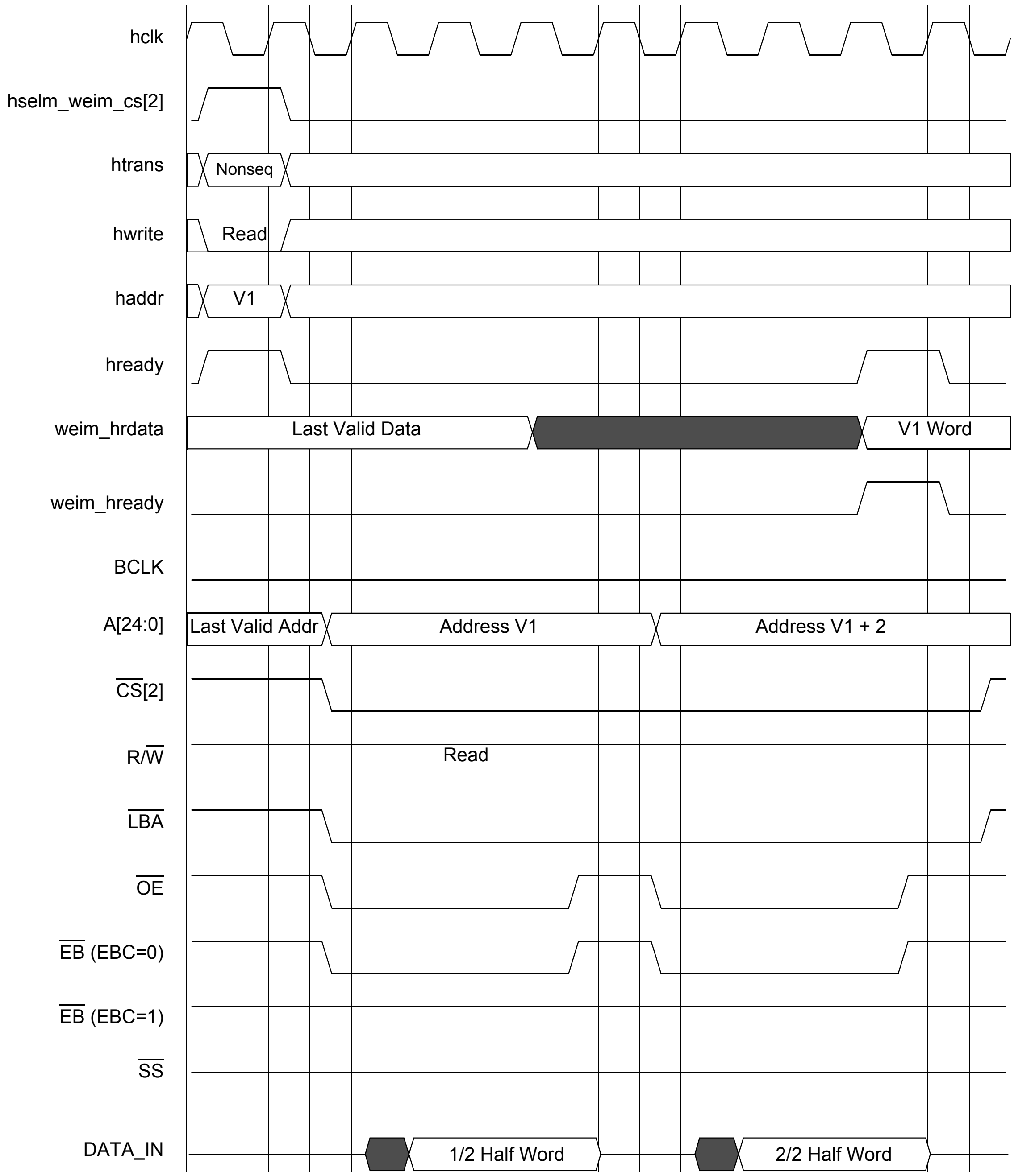


Figure 14. WSC = 3, OEN = 2, A.WORD/E.HALF

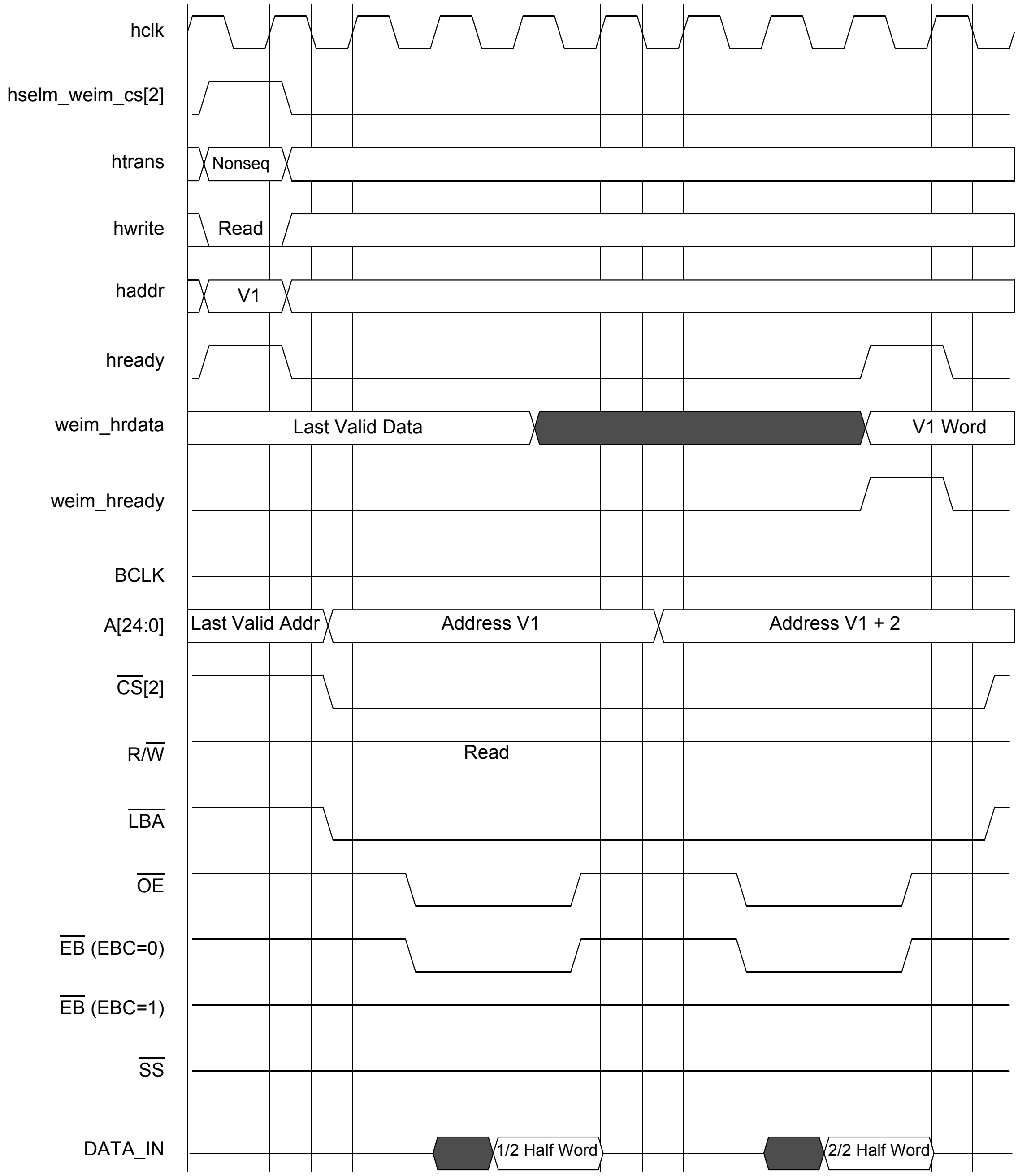


Figure 15. WSC = 3, OEA = 2, OEN = 2, A.WORD/E.HALF

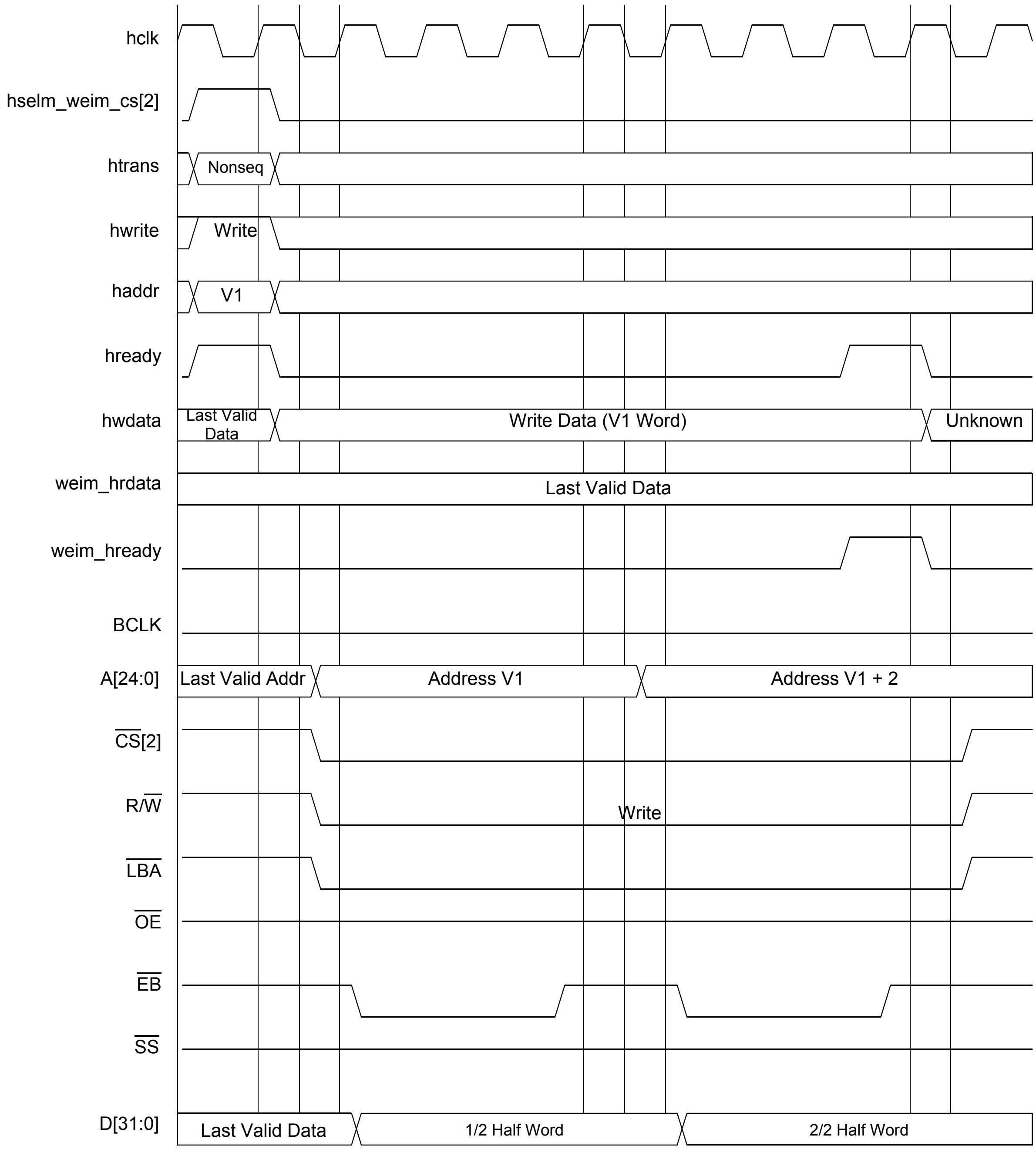


Figure 16. WSC = 2, WWS = 1, WEA = 1, WEN = 2, A.WORD/E.HALF

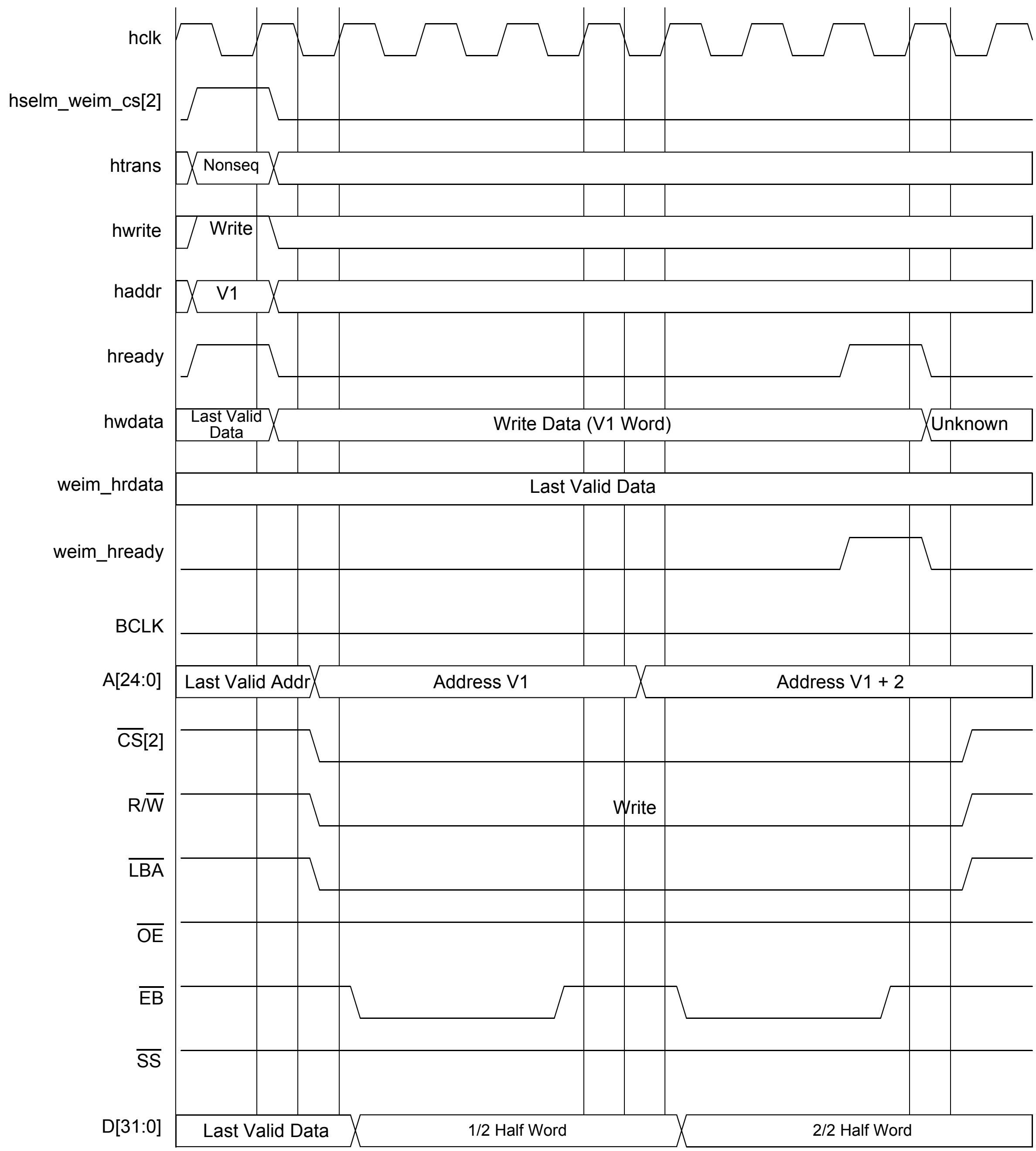


Figure 17. WSC = 1, WWS = 2, WEA = 1, WEN = 2, A.WORD/E.HALF

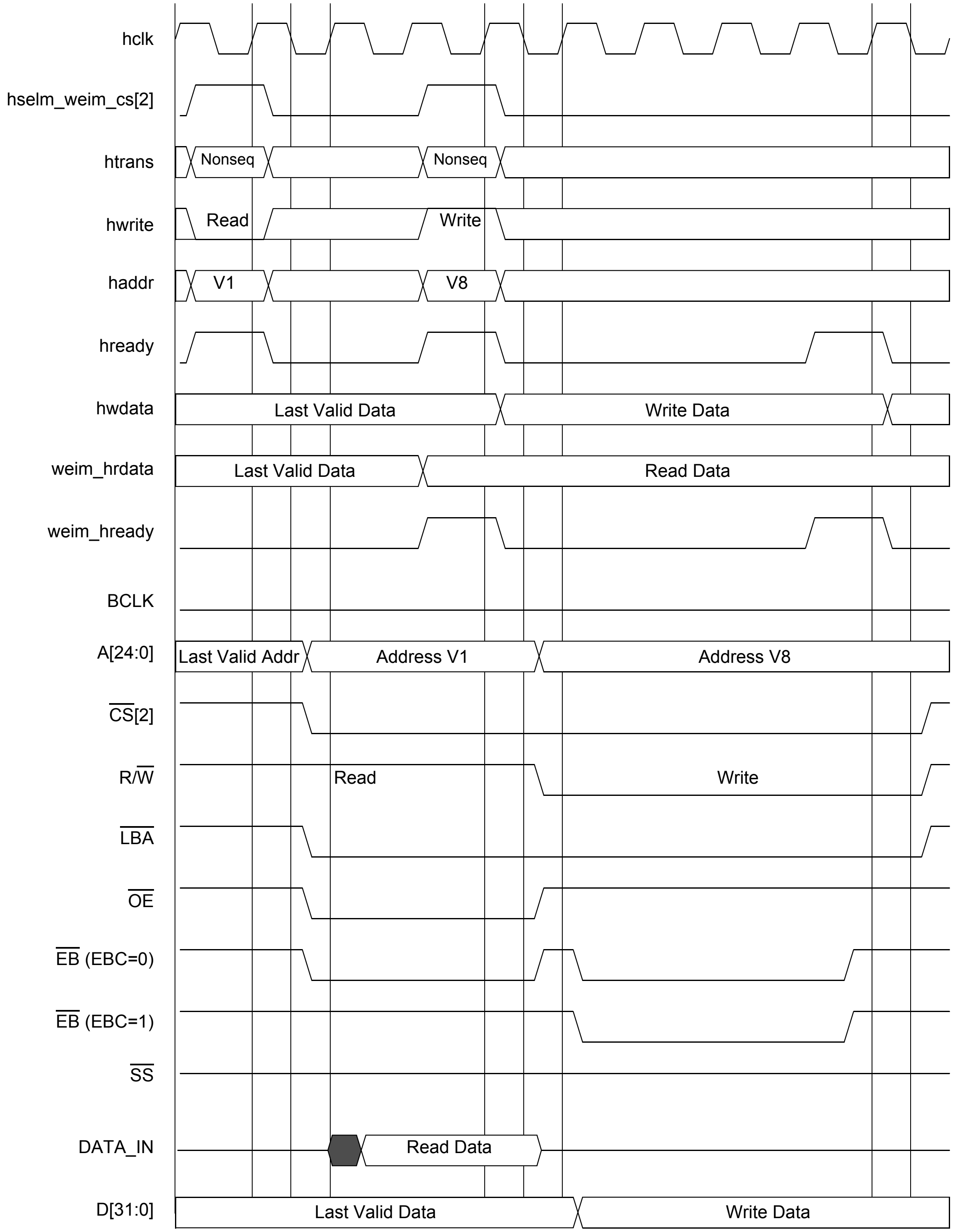


Figure 18. WSC = 2, WWS = 2, WEA = 1, WEN = 2, A.HALF/E.HALF

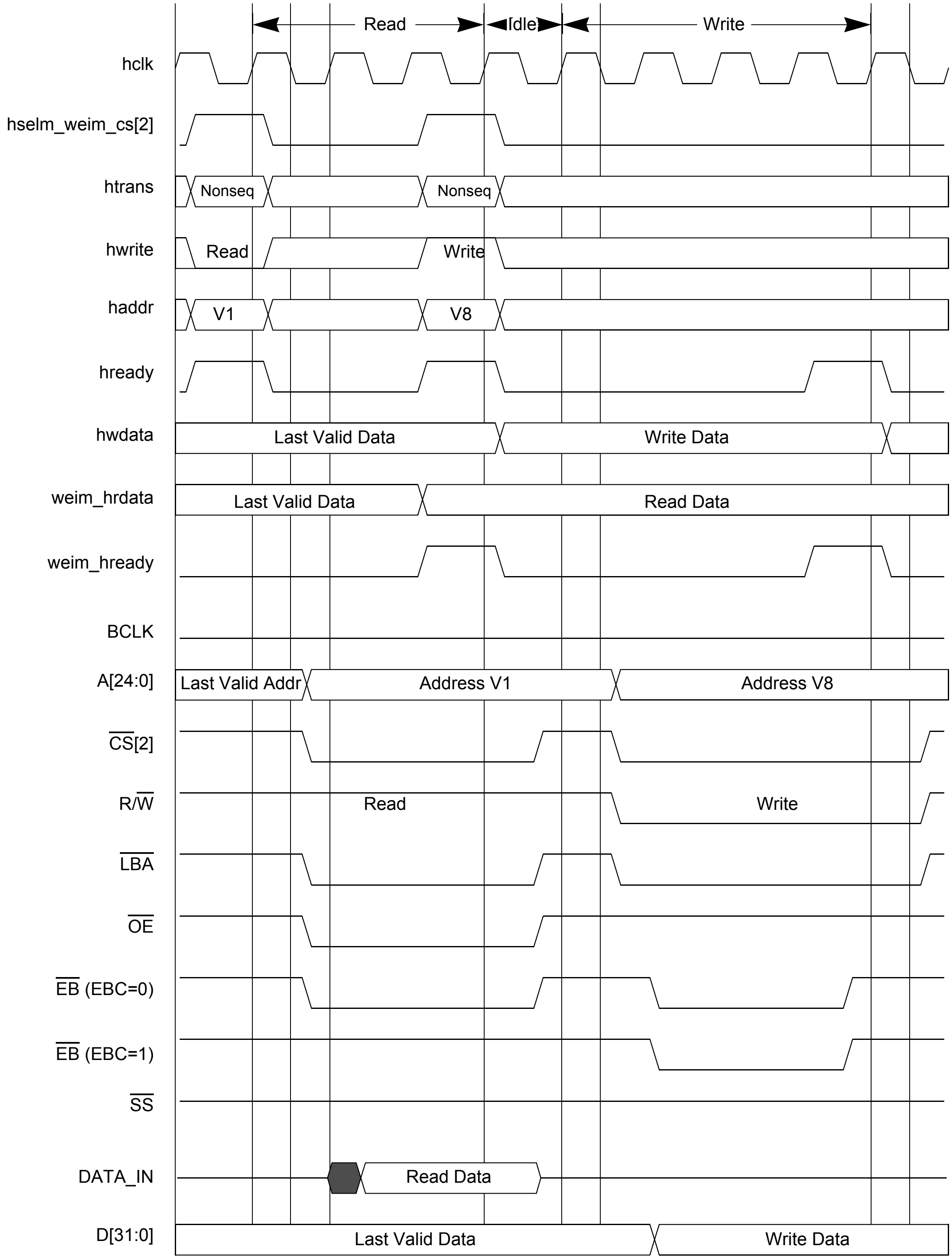


Figure 19. WSC = 2, WWS = 1, WEA = 1, WEN = 2, EDC = 1, A.HALF/E.HALF

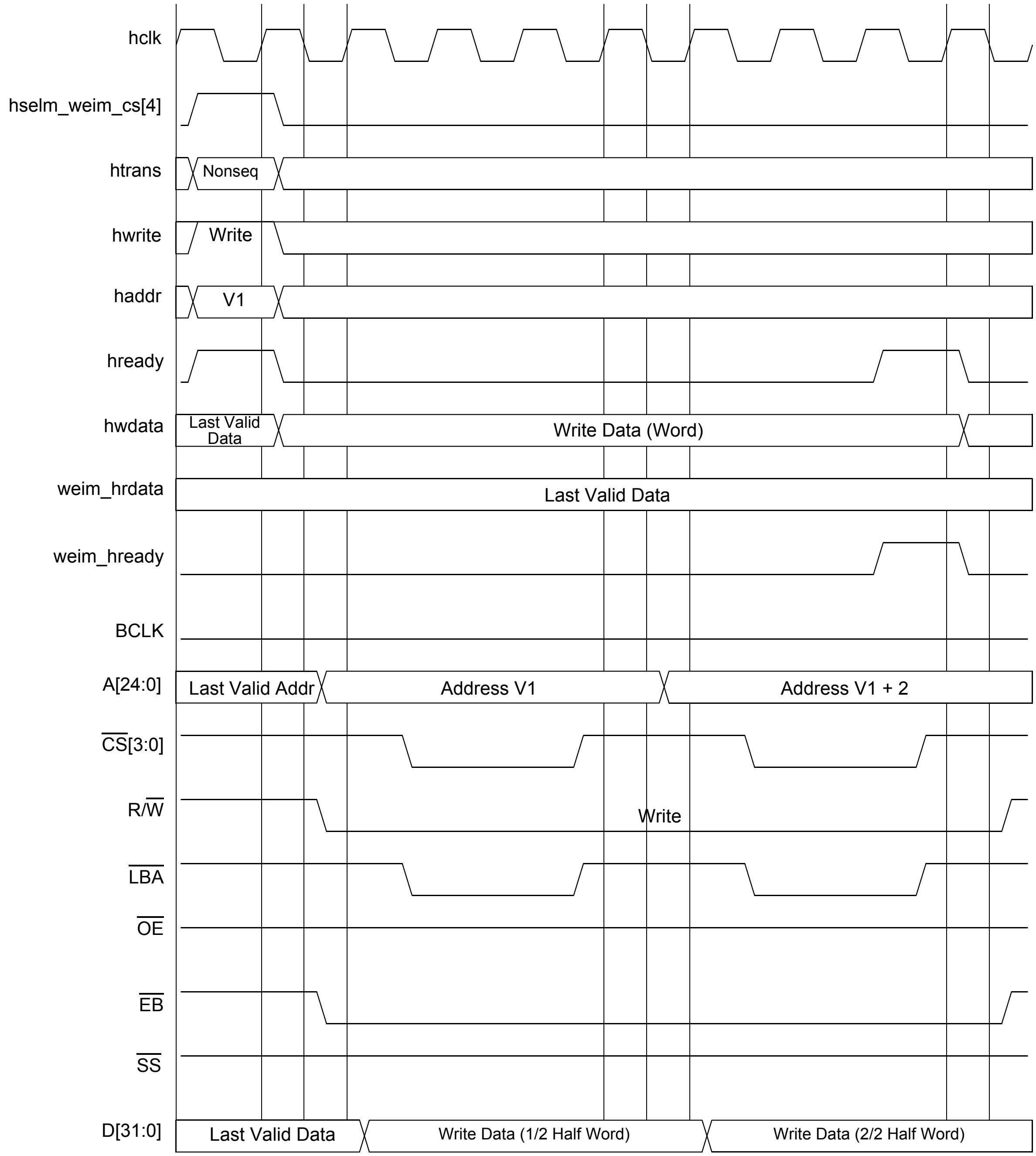


Figure 20. WSC = 2, CSA = 1, WWS = 1, A.WORD/E.HALF

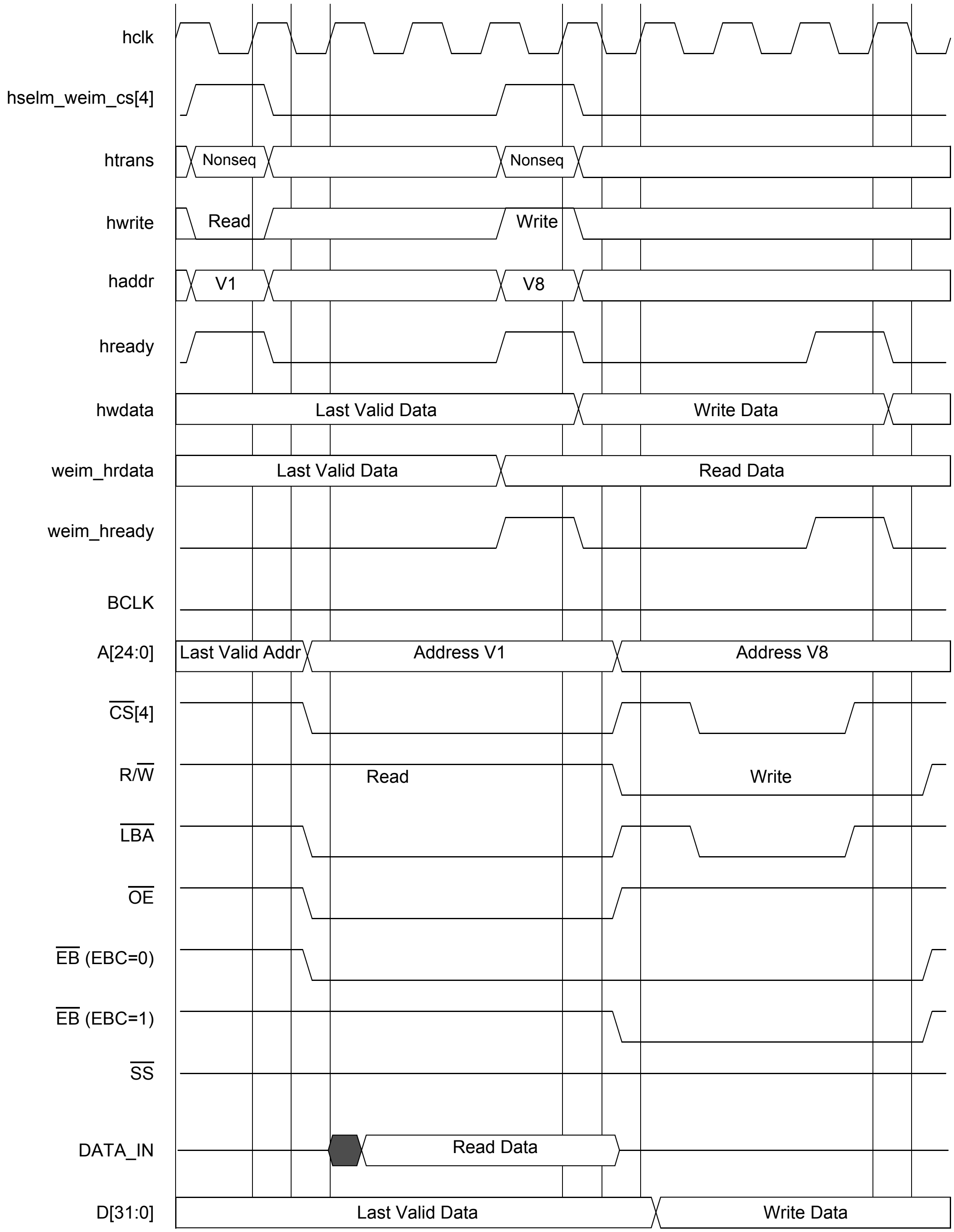


Figure 21. WSC = 3, CSA = 1, A.HALF/E.HALF

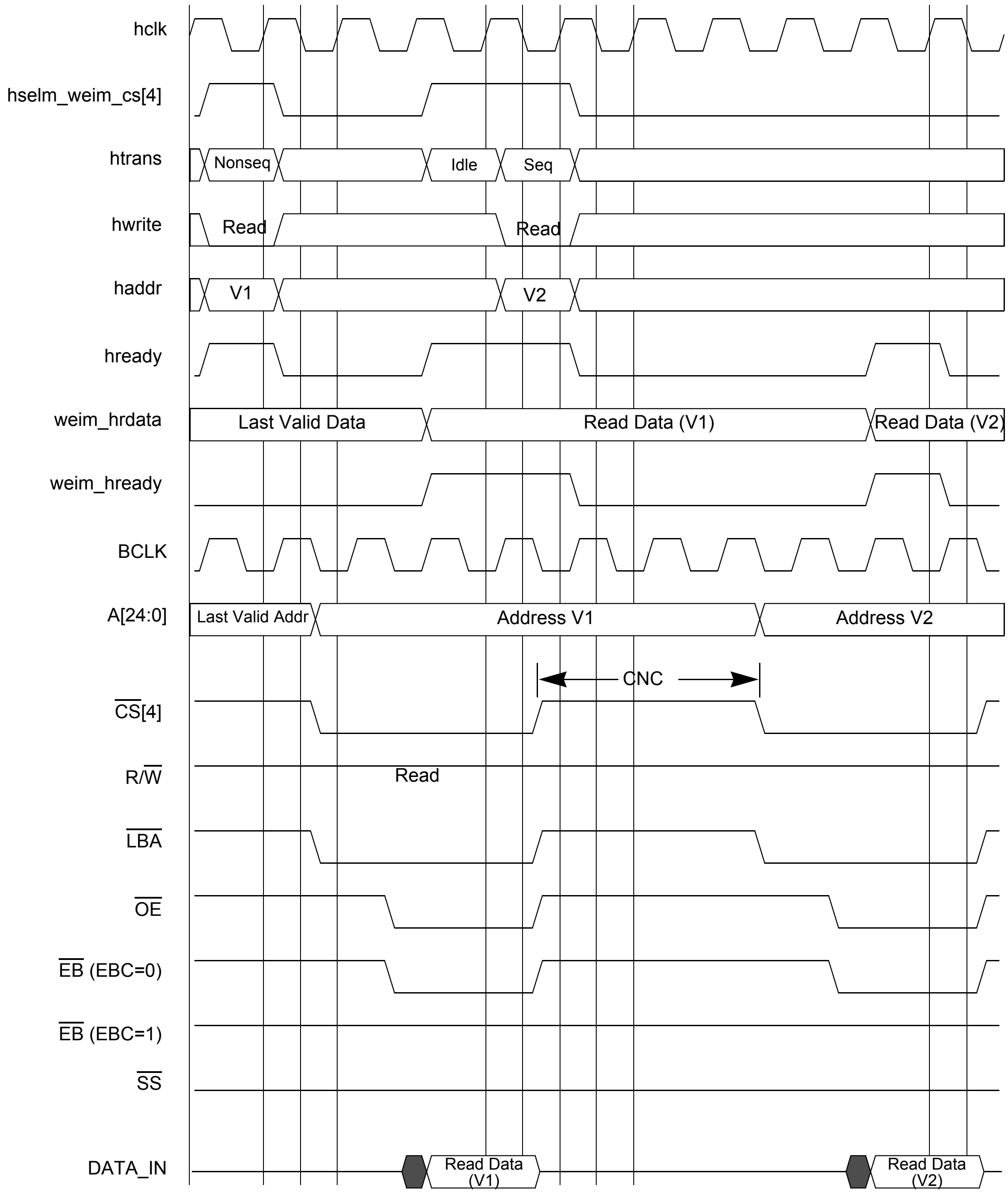


Figure 22. WSC = 2, OEA = 2, CNC = 3, BCM = 1, A.HALF/E.HALF

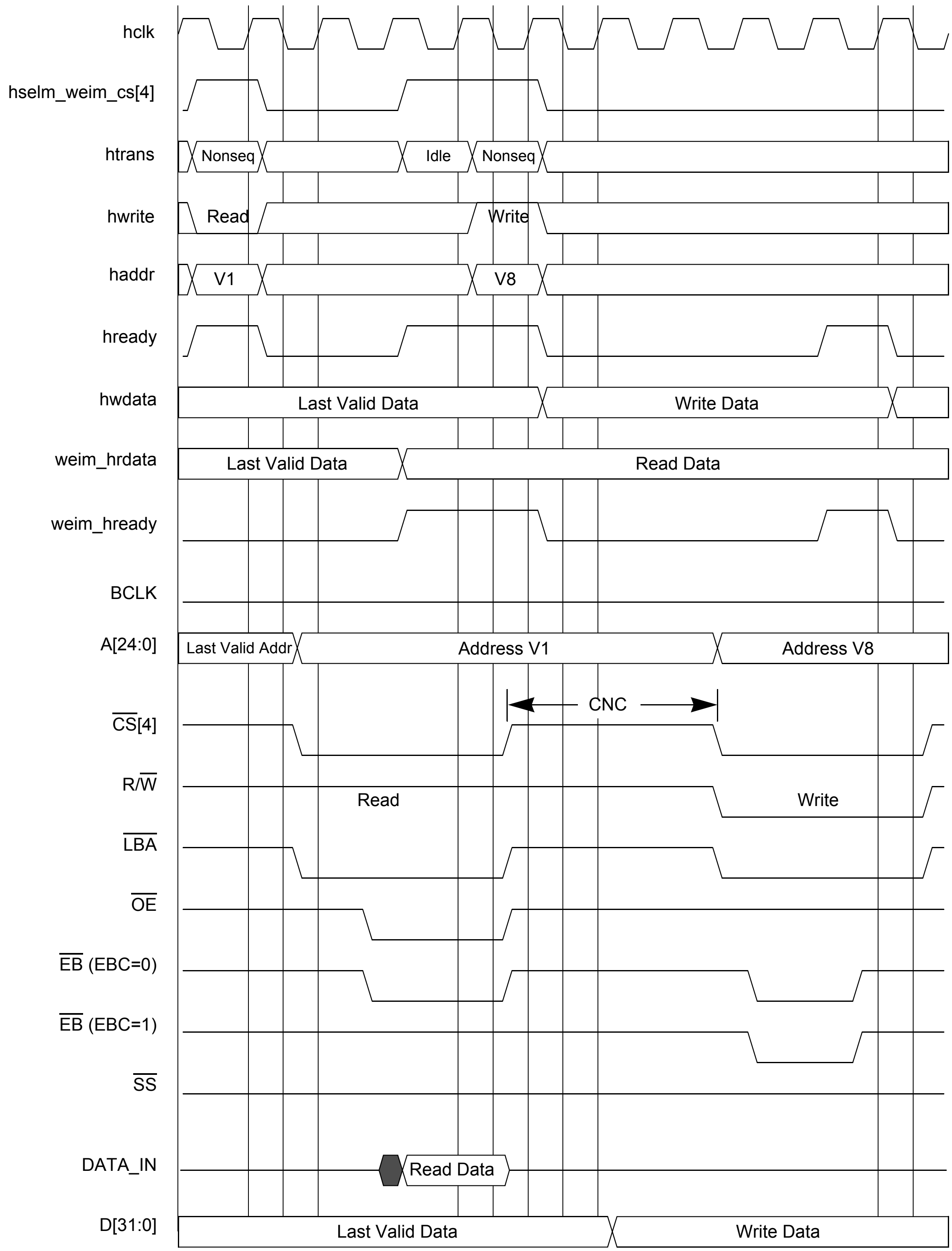


Figure 23. WSC = 2, OEA = 2, WEA = 1, WEN = 2, CNC = 3, A.HALF/E.HALF

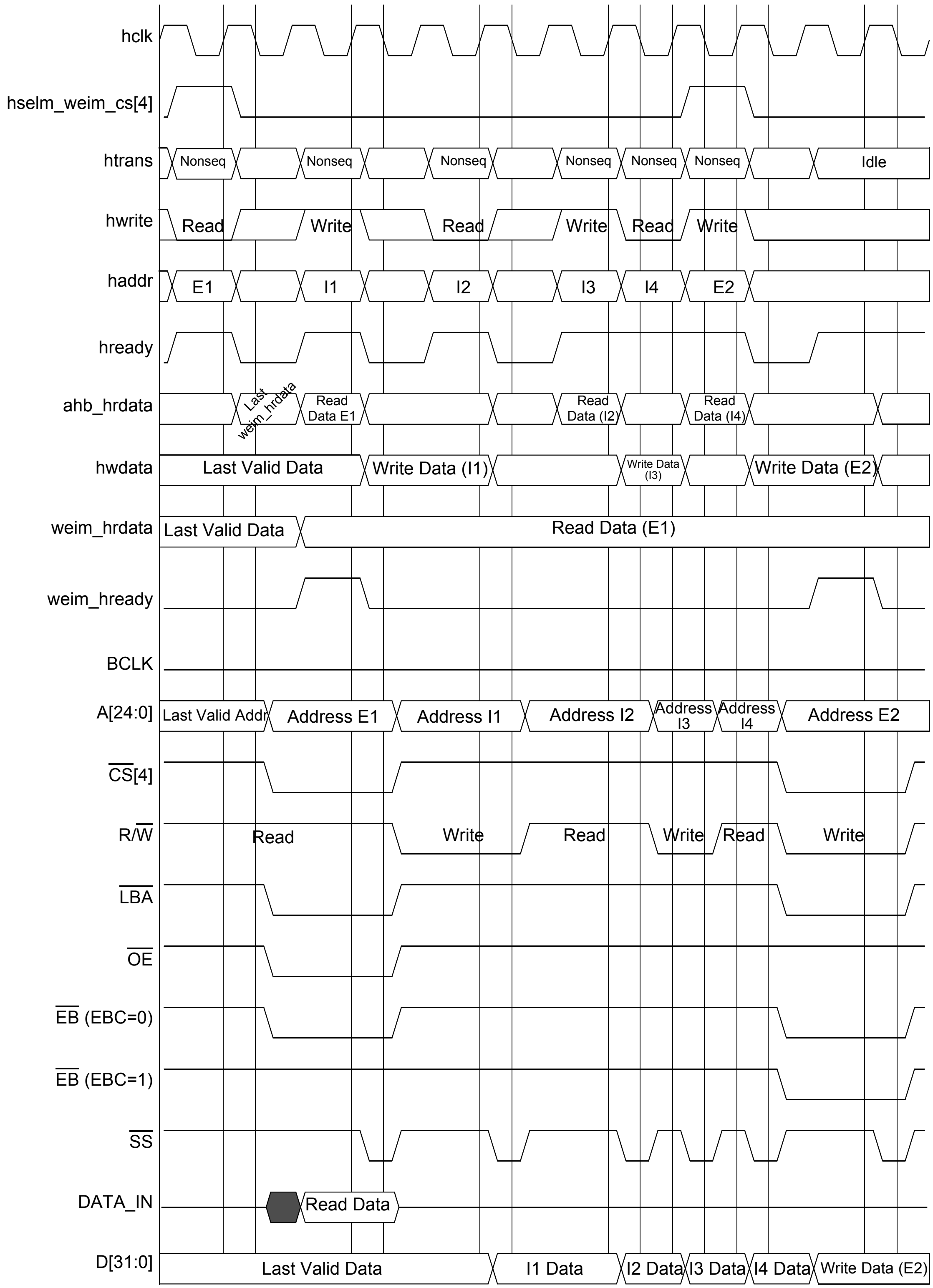


Figure 24. WSC = 1, WEA = 1, WEN = 1, SHEN = 01 or SHEN = 10, A.HALF/E.HALF

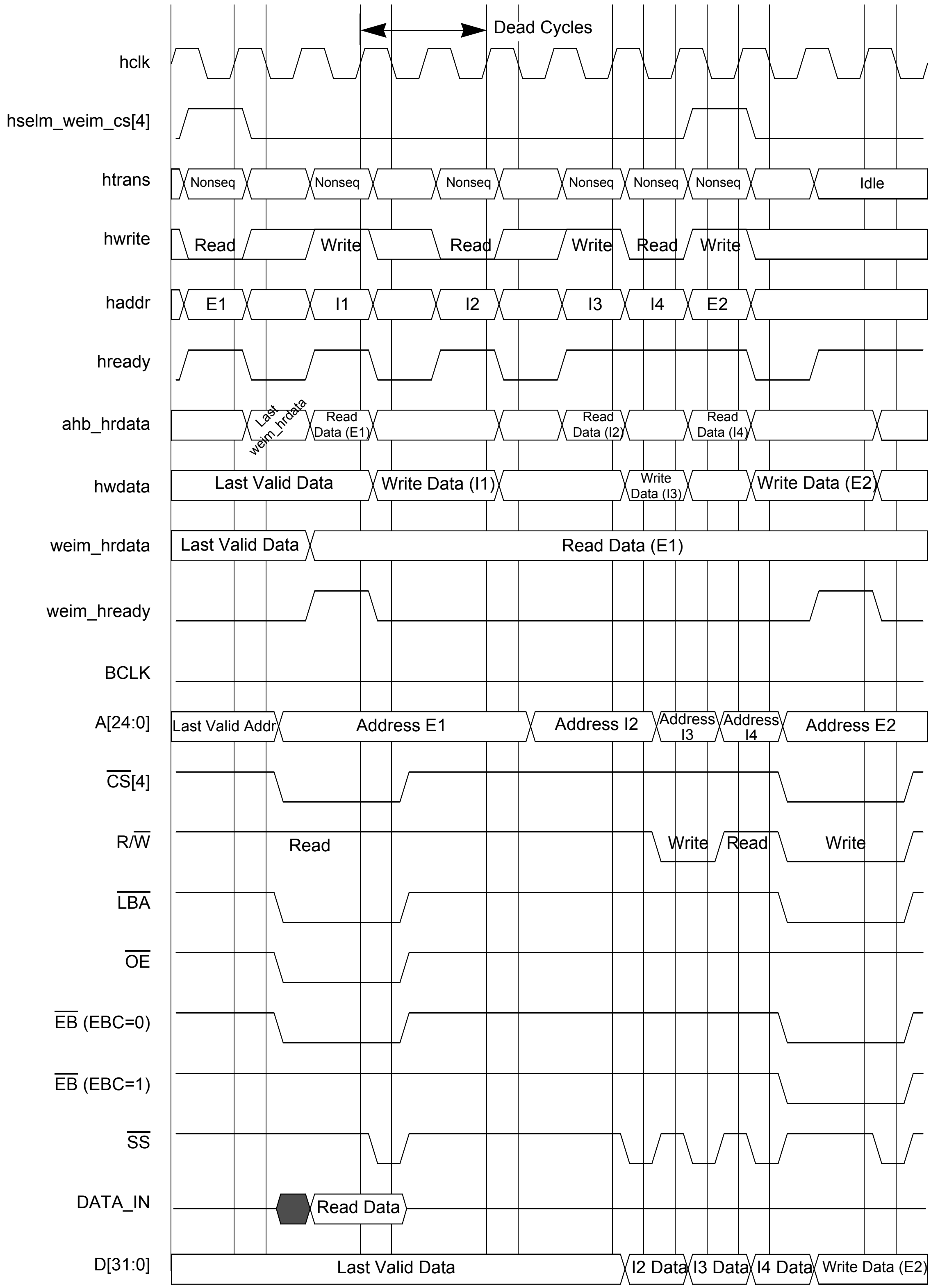


Figure 25. WSC = 1, WEA = 1, WEN = 1, EDC = 2, SHEN = 01, A.HALF/E.HALF

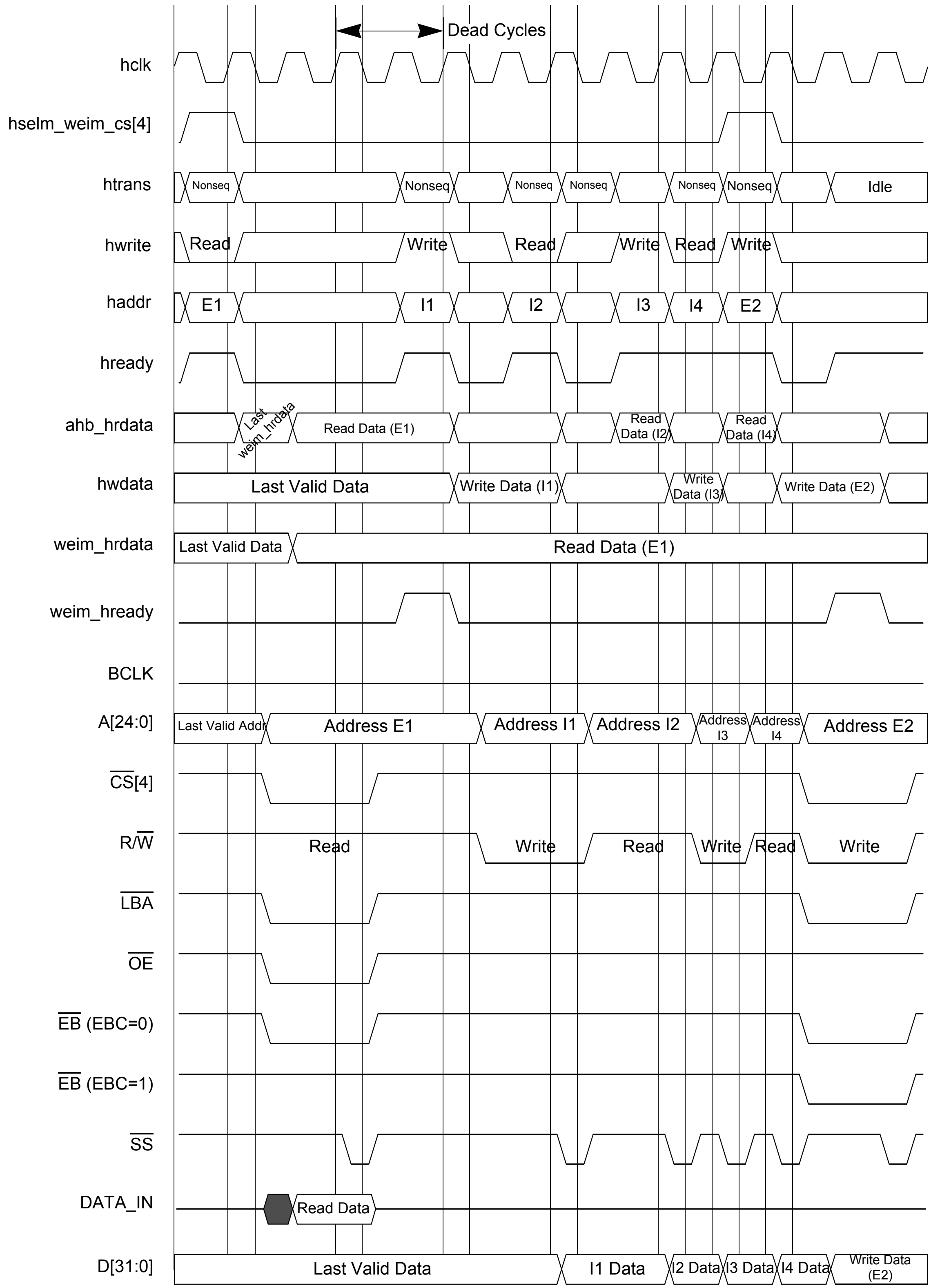


Figure 26. WSC = 1, WEA = 1, WEN = 1, EDC = 2, SHEN = 10, A.HALF/E.HALF

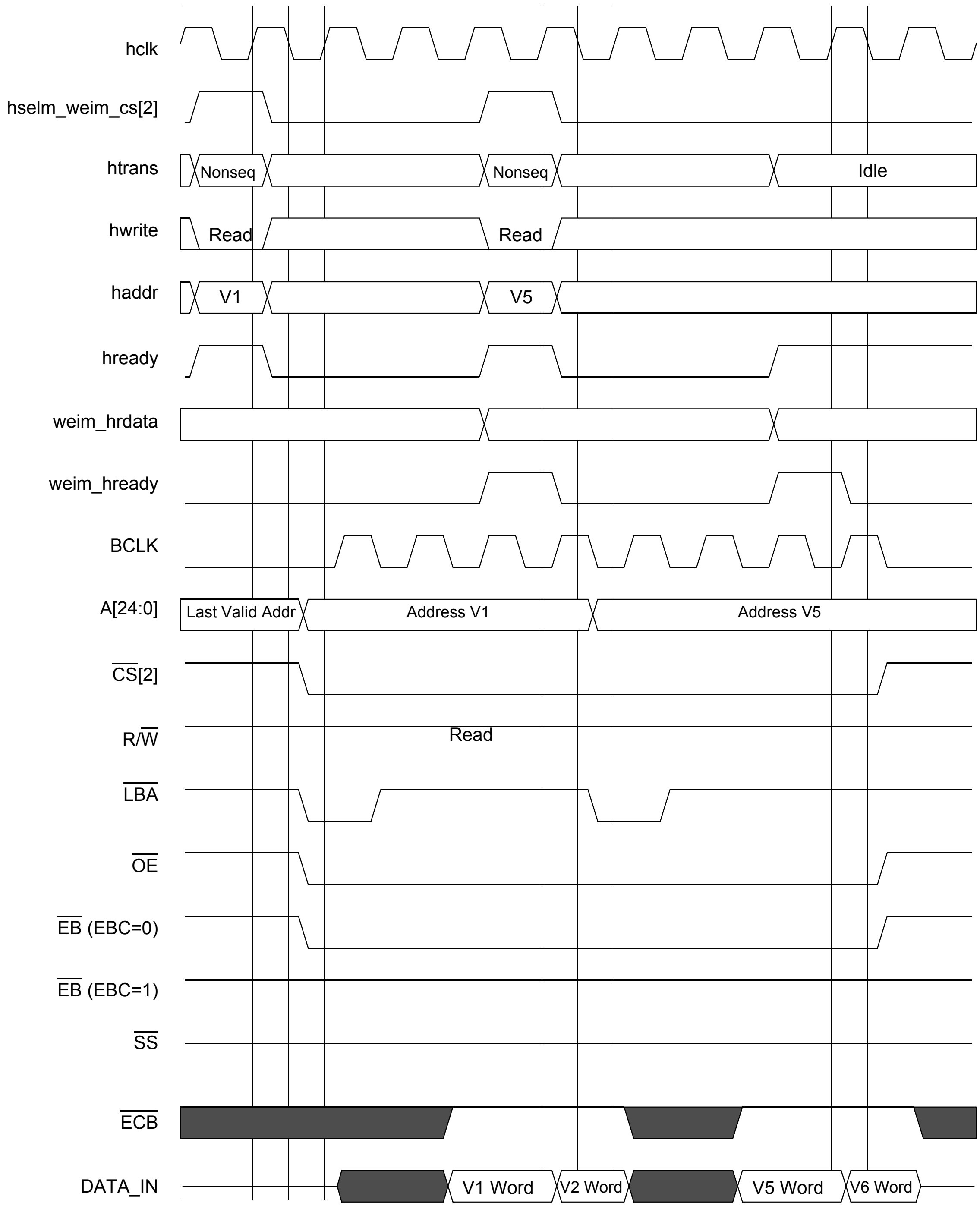


Figure 27. WSC = 3, SYNC = 1, A.HALF/E.HALF

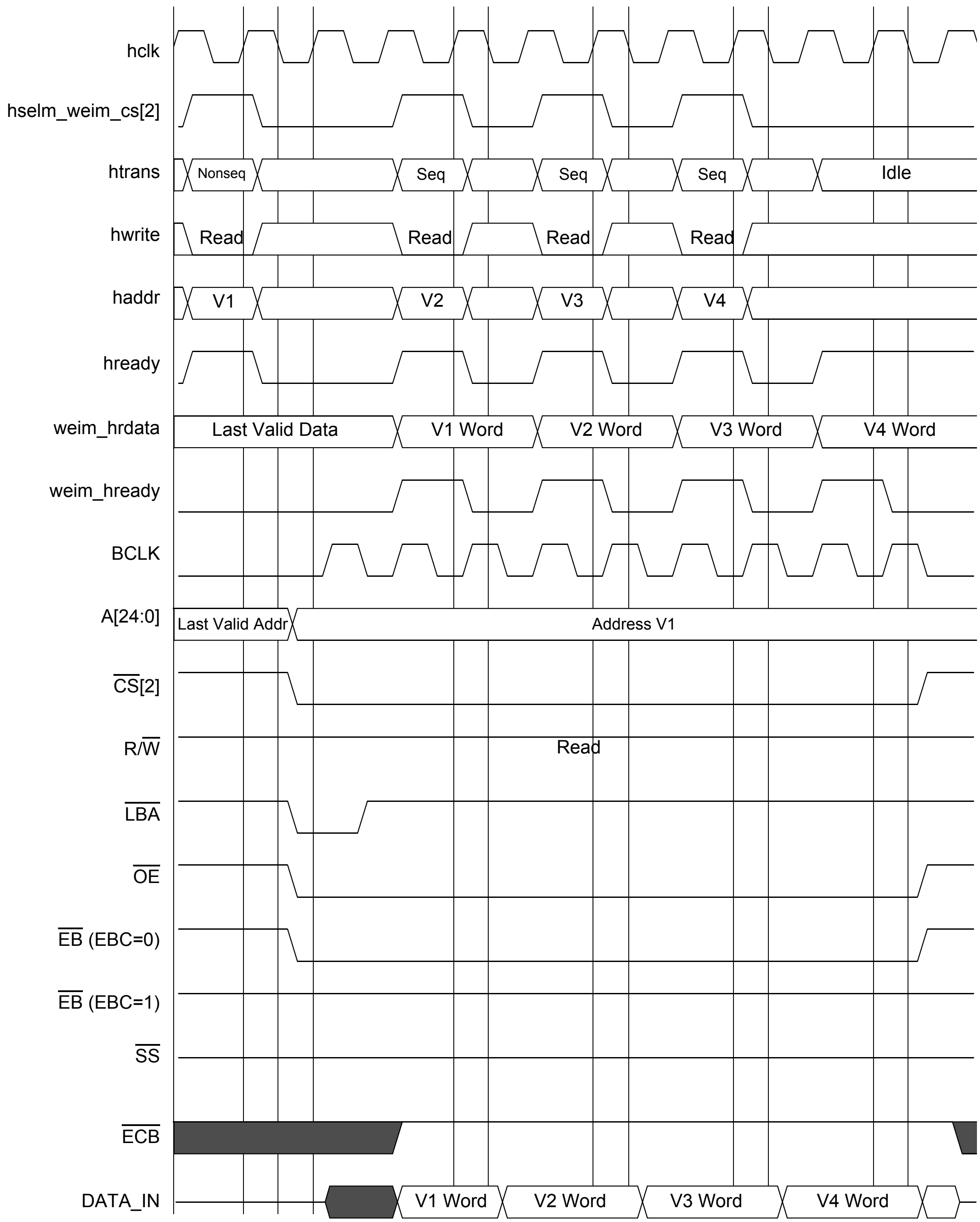


Figure 28. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.WORD

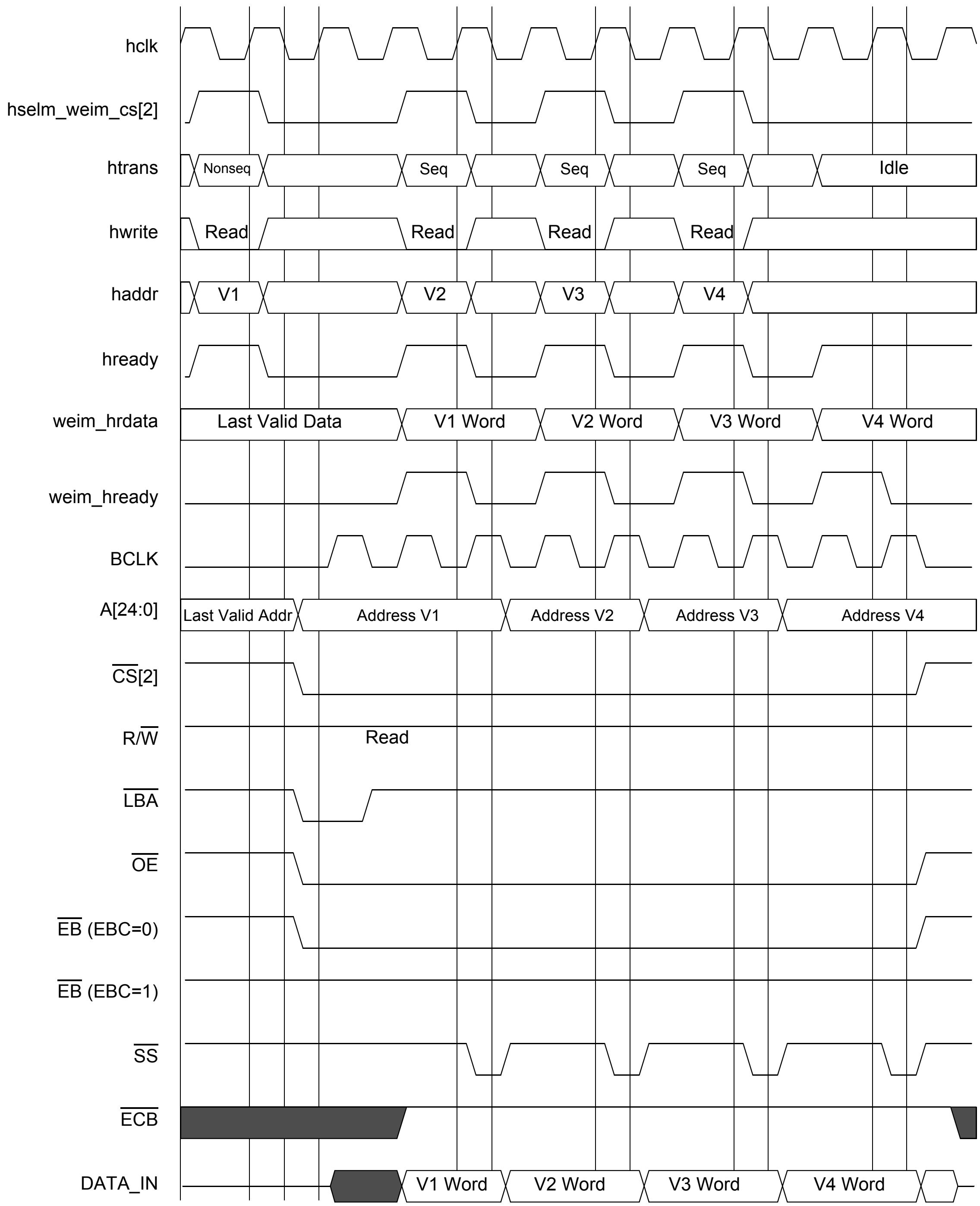


Figure 29. WSC = 2, SYNC = 1, DOL = [1/0], SHEN = 01, A.WORD/E.WORD

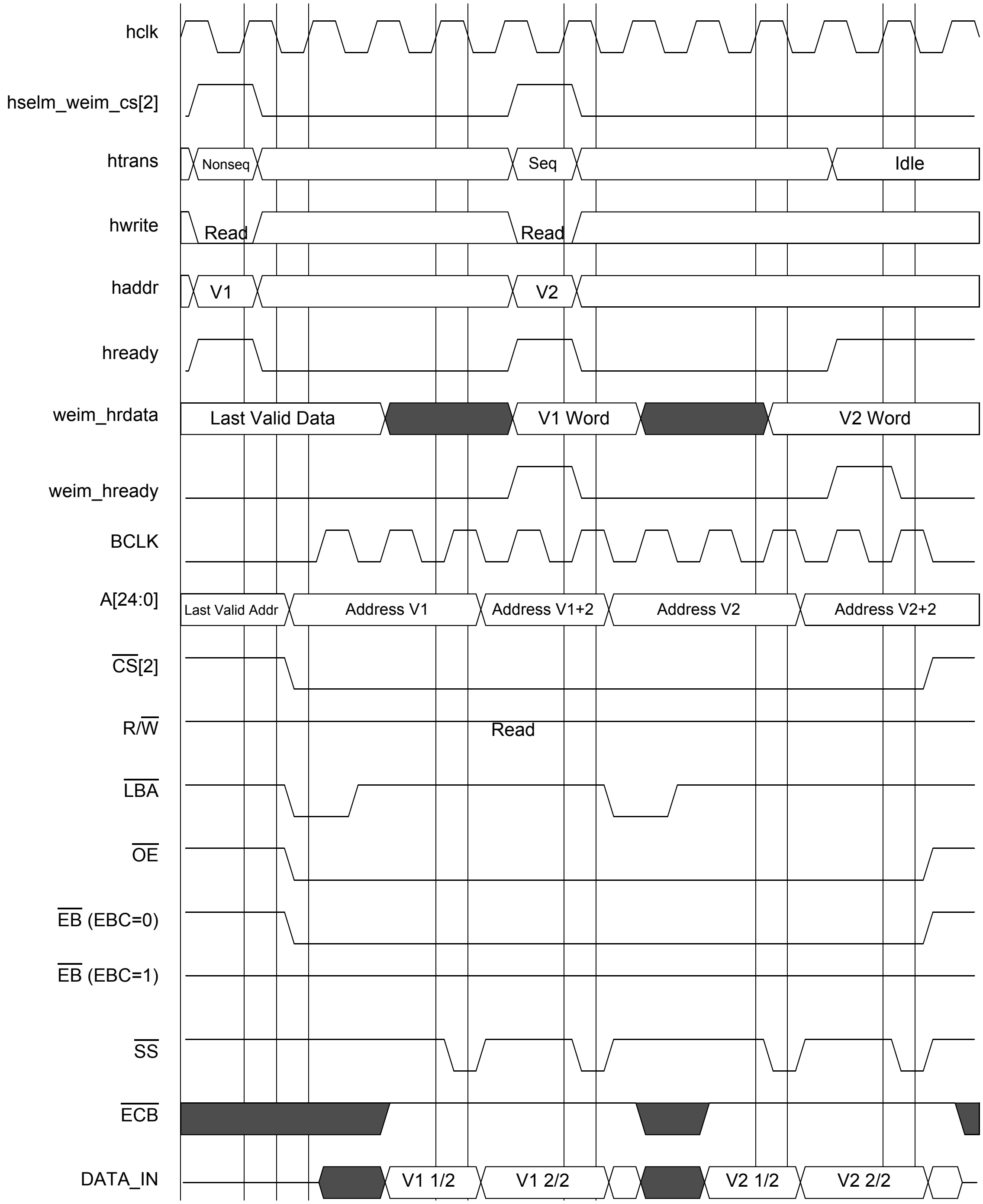


Figure 30. WSC = 2, SYNC = 1, DOL = [1/0], SHEN = 10, A.WORD/E.HALF

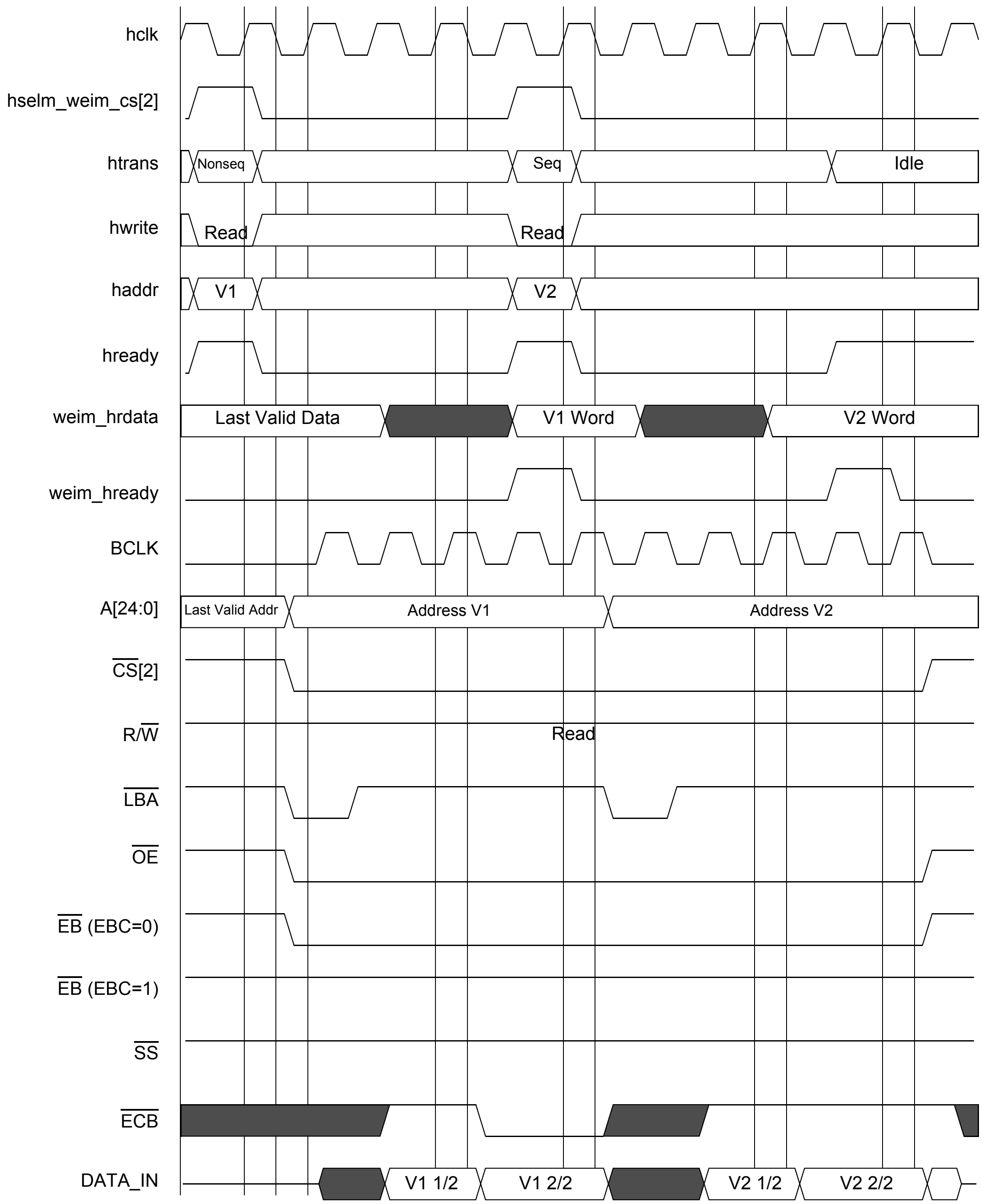


Figure 31. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.HALF

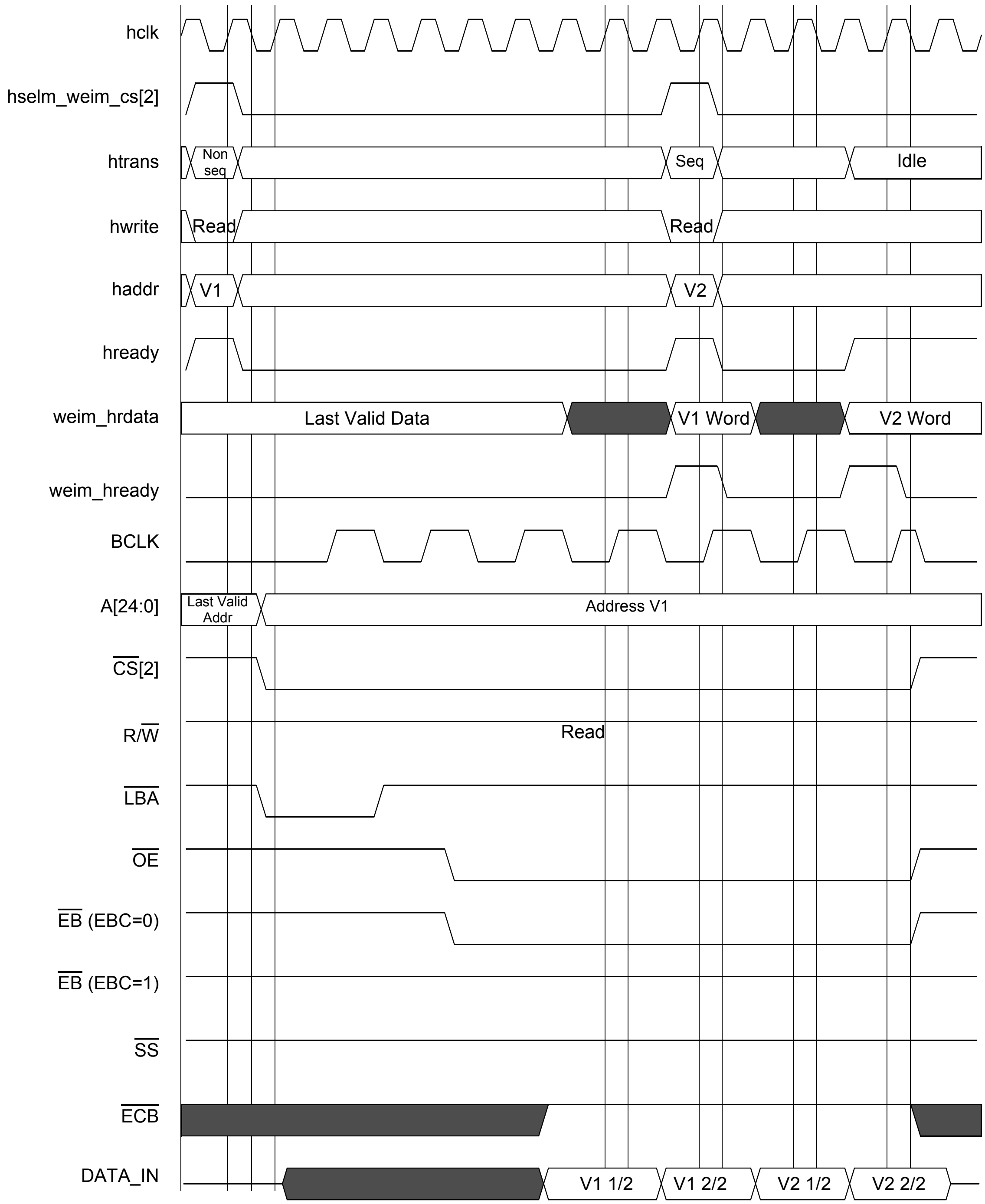


Figure 32. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 2, A.WORD/E.HALF

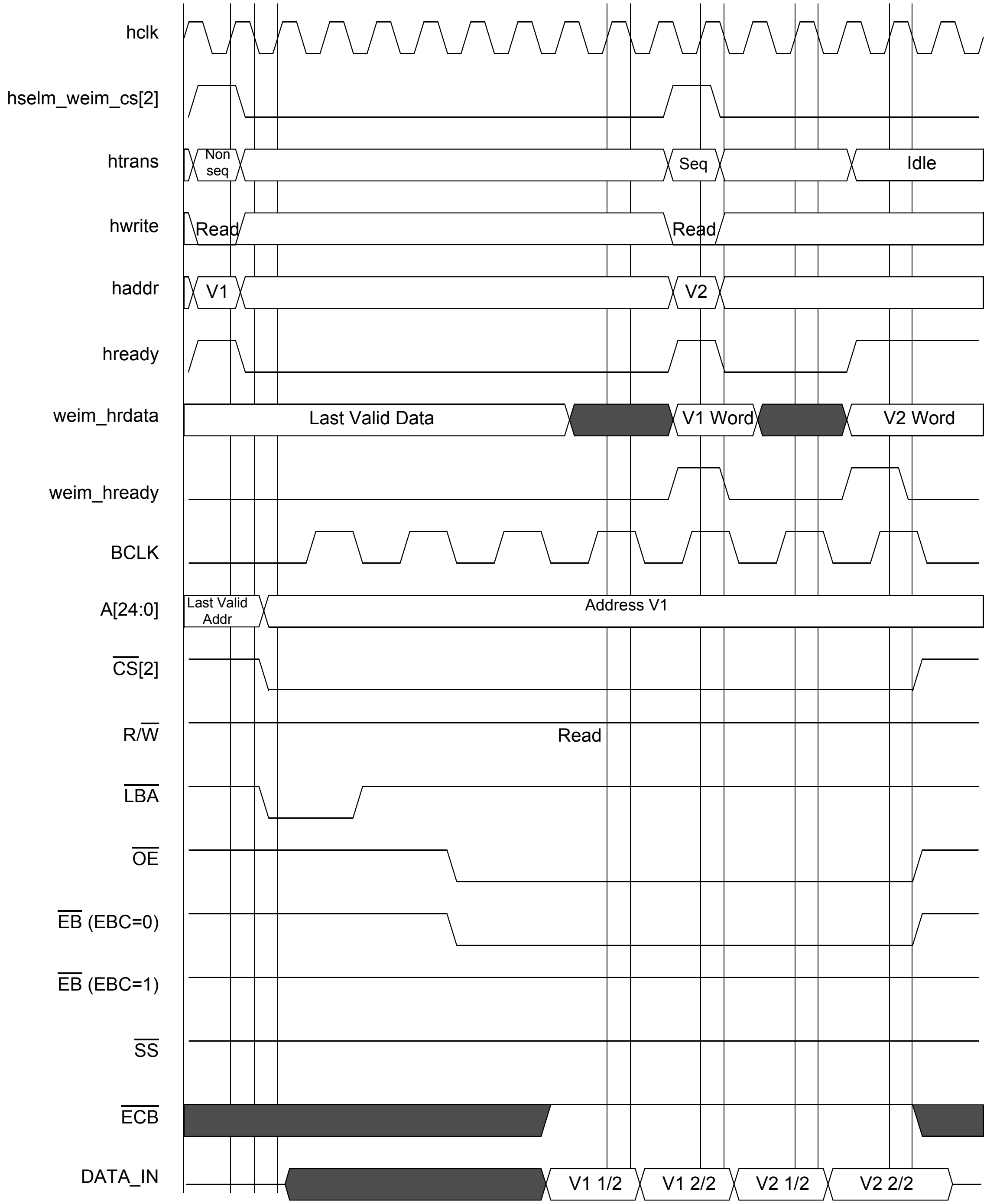


Figure 33. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 1, A.WORD/E.HALF

3.10 Pen ADC Specifications

The specifications for the pen ADC are shown in Table 10 through Table 12.

Table 10. Pen ADC System Performance

Full Range Resolution[1]	13 bits
Non-Linearity Error[1]	4 bits
Accuracy [1]	9 bits

1. Tested under input = 0~1.8V at 25°C

Table 11. Pen ADC Test Conditions

Vp max	1800 mV	ip max	+7 μA
Vp min	GND	ip min	1.5 μA
Vn	GND	in	1.5 μA
Sample frequency		12 MHz	
Sample rate		1.2 KHz	
Input frequency		100 Hz	
Input range		0–1800 mV	
Note: Ru1 = Ru2 = 200K			

Table 12. Pen ADC Absolute Rating

ip max	+9.5 μA
ip min	-2.5 μA
in max	+9.5 μA
in min	-2.5 μA

3.11 Voice Codec Specifications

The specifications for the voice Codec are shown in Table 13 through Table 14.

Table 13. Voice Codec

Full Range Resolution[1]	13 bits
Non-Linearity Error[1]	TBD
Accuracy [1]	9 bits

1. Tested under input = 0~1.8V at 25°C

Table 14. Voice Codec Test Conditions

Sample rate	8 kHz
Input frequency	1 kHz
Input range	0–1800 mV

3.12 Bluetooth Accelerator (BTA)

The Bluetooth Accelerator (BTA) radio interface supports two RF front-ends:

- Motorola Radio, MC13180, SPI Interface
- SiliconWave Radio, SiW1502, SPI Interface

3.12.1 Timing Diagrams for Silicon Wave Radio, SiW1502

The timing diagrams for the SiliconWave™ SiW1502 are shown in Figure 34 and Figure 35.

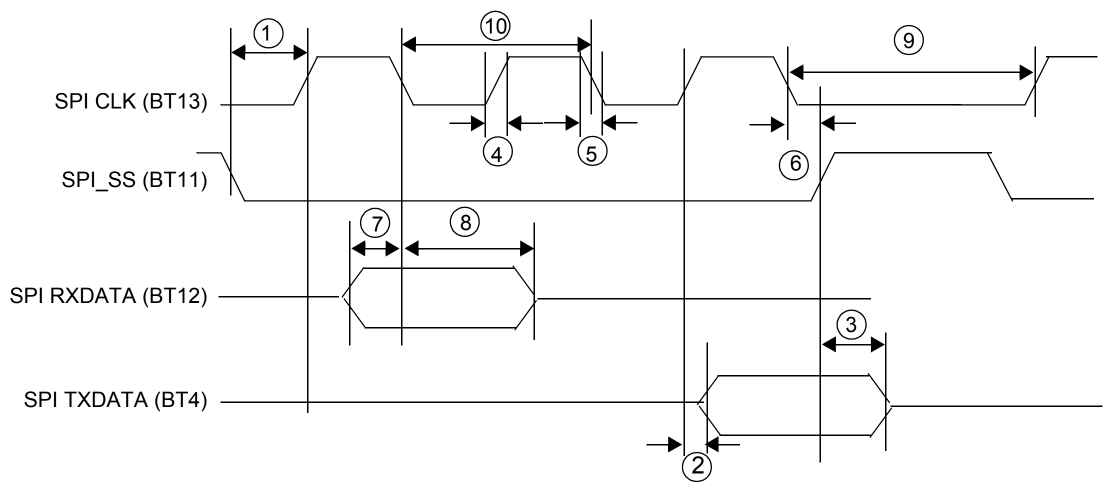


Figure 34. SPI Interface Timing Diagram Using Silicon Wave Radio, SiW 1502

Table 15. SPI Interface Timing Parameter Table Using Silicon Wave Radio, SiW 1502

Ref No.	Parameter	Minimum	Maximum	Unit
1	SPI_SS setup time relative to rising edge of SPI_CLK	15	—	ns
2	Transmit data delay time relative to rising edge of SPI_CLK	0	15	ns
3	Transmit data hold time relative to rising edge of SPI_SS	0	15	ns
4	SPI_CLK Rise time	0	25	ns
5	SPI_CLK Fall time	0	25	ns
6	SPI_SS hold time relative to falling edge of SPI_CLK	15	—	ns
7	Receive data setup time relative to falling edge of SPI_CLK[1]	15	—	ns

Table 15. SPI Interface Timing Parameter Table Using Silicon Wave Radio, SiW 1502 (Continued)

Ref No.	Parameter	Minimum	Maximum	Unit
8	Receive data hold time relative to falling edge of SPI_CLK[1]	15	—	ns
9	Turnaround time between address write and data read[2]	375	—	ns
10	SPI_CLK frequency, 50% duty cycle required[1]	—	4	MHz

1. The clock frequency, duty cycle, setup and hold of SPI_SS and receive data can be set by programming SPI_Control register (0x00216138) together with system clock.
2. The requirement of turnaround time is needed only when SPI_CLK is running over 1.33 MHz. When the SPI_CLK speed is lower than 1.33 MHz, no delay for turnaround is necessary.

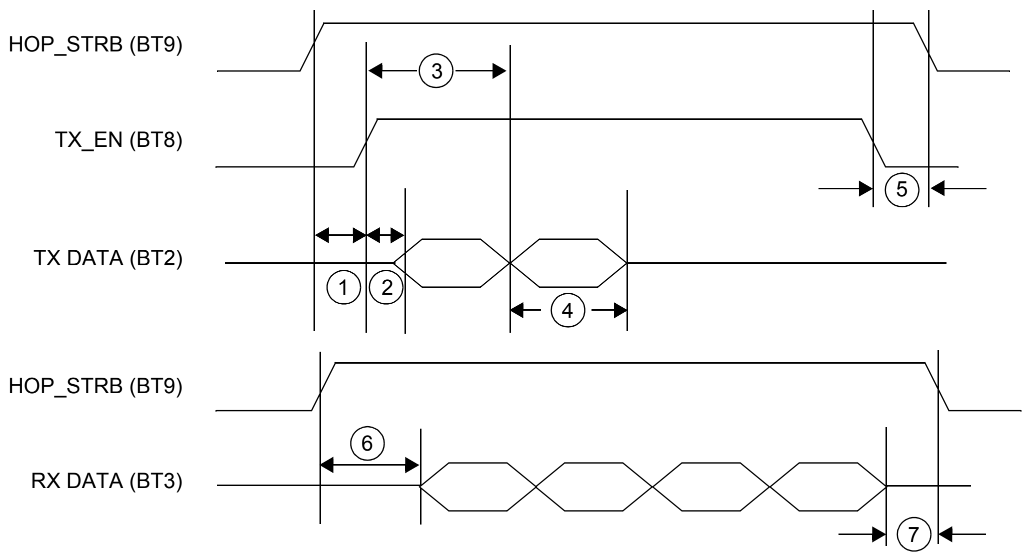


Figure 35. Silicon Wave SiW 1502 Data Bus Timing Diagram

Table 16. Silicon Wave SiW 1502 Data Bus Timing Parameter Table

Ref No.	Parameter	Minimum	Maximum	Unit
1	Setup time from HOP_STRB valid to TX_EN valid[1]	750	—	ns
2	TX DATA setup time relative to TX_EN	-100	100	ns
3	TX DATA hold time	900	—	ns
4	TX DATA period	1000 +/- 0.02		ns
5	Hold time from TX_EN invalid to HOP_STRB invalid	250	—	ns
6	Delay from rising edge of HOP_STRB to data appearing at RX DATA	32	43	us
7	Hold time required for HOP_STRB after last bit of data	10	—	ns

1. The setup and hold times of HOP_STRB and TX_EN can be set by programming TIME_A_B (0x00216050), TIME_C_D (0x00216054) and RF_Status (0x0021605C) registers

3.12.2 Timing Diagrams for Motorola MC13180

The timing diagrams for the Motorola MC13180 are shown in Figure 36 and Figure 37 on page 53.

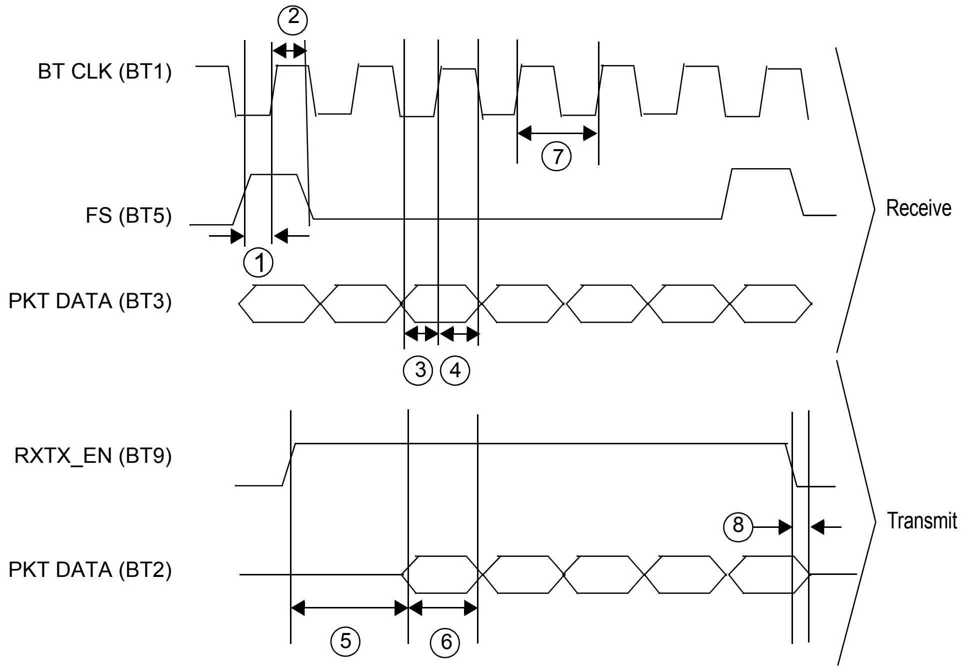


Figure 36. Data Bus Timing Diagram Using Motorola MC13180

Table 17. Data Bus Timing Parameter Table Using Motorola MC13180

Ref No.	Parameter	Minimum	Maximum	Unit
1	FrameSync setup time relative to BT CLK rising edge[1]	—	—	ns
2	FrameSync hold time relative to BT CLK rising edge[1]	—	—	ns
3	Receive Data setup time relative to BT CLK rising edge[1]	—	—	ns
4	Receive Data hold time relative to BT CLK rising edge[1]	—	—	ns
5	Transmit Data setup time relative to RXTX_EN rising edge[2]	172.5	192.5	us
6	TX DATA period	1000 +/- 0.02		ns
7	BT CLK duty cycle	40	60	%
8	Transmit Data hold time relative to RXTX_EN falling edge	4	10	us

1. Please refer to Motorola 2.4 GHz RF Transceiver Module (MC13180) Technical Data documentation.
2. The setup and hold times of RX_TX_EN can be adjusted by programming Time_A_B register (0x00216050) and RF_Status (0x0021605C) registers.

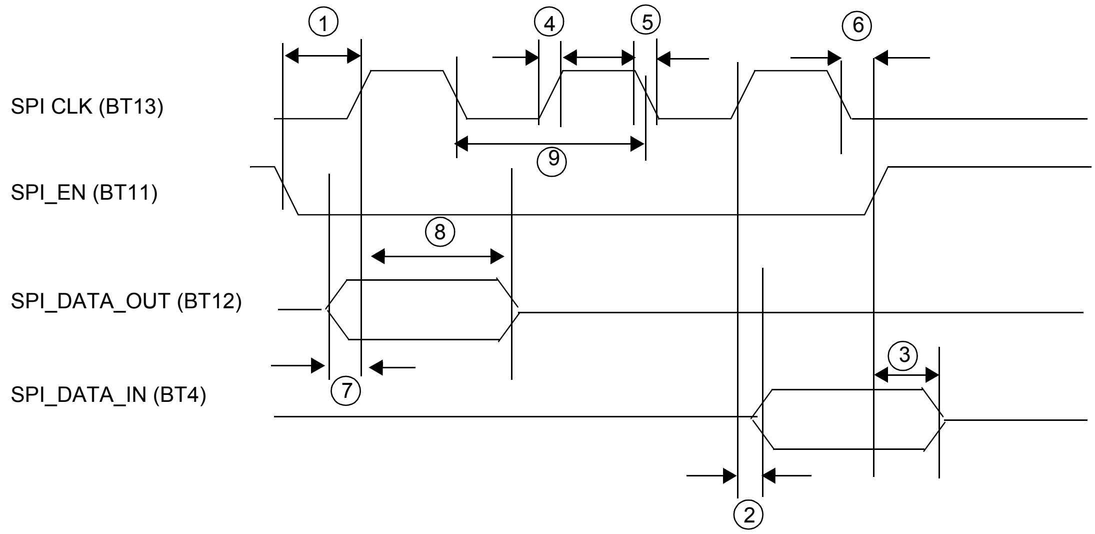


Figure 37. SPI Interface Timing Diagram Using Motorola MC13180

Table 18. SPI Interface Timing Parameter Table Using Motorola MC13180

Ref No.	Parameter	Minimum	Maximum	Unit
1	SPI_EN setup time relative to rising edge of SPI_CLK	15	—	ns
2	Transmit data delay time relative to rising edge of SPI_CLK	0	15	ns
3	Transmit data hold time relative to rising edge of SPI_EN	0	15	ns
4	SPI_CLK rise time	0	25	ns
5	SPI_CLK fall time	0	25	ns
6	SPI_EN hold time relative to falling edge of SPI_CLK	15	—	ns
7	Receive data setup time relative to falling edge of SPI_CLK[1]	15	—	ns
8	Receive data hold time relative to falling edge of SPI_CLK[1]	15	—	ns
9	SPI_CLK frequency, 50% duty cycle required[1]	—	20	MHz

1. The SPI_CLK clock frequency and duty cycle, setup and hold times of receive data can be set by programming SPI_Control (0x00216138) register together with system clock.

3.13 SPI Timing Diagrams

To utilize the internal transmit (TX) and receive (RX) data FIFOs when the SPI 1 module is configured as a master, two control signals are used for data transfer rate control: the $\overline{\text{SS}}$ signal (output) and the $\overline{\text{SPI\_RDY}}$ signal (input). The SPI 1 Sample Period Control Register (PERIODREG1) and the SPI 2 Sample Period Control Register (PERIODREG2) also can be programmed to a fixed data transfer rate for either SPI 1 or SPI 2. When the SPI 1 module is configured as a slave, the user can configure the SPI 1 Control Register (CONTROLREG1) to match the external SPI master's timing. In this configuration, $\overline{\text{SS}}$ becomes an input signal, and is used to latch data into or load data out to the internal data shift registers, as well as to increment the data FIFO

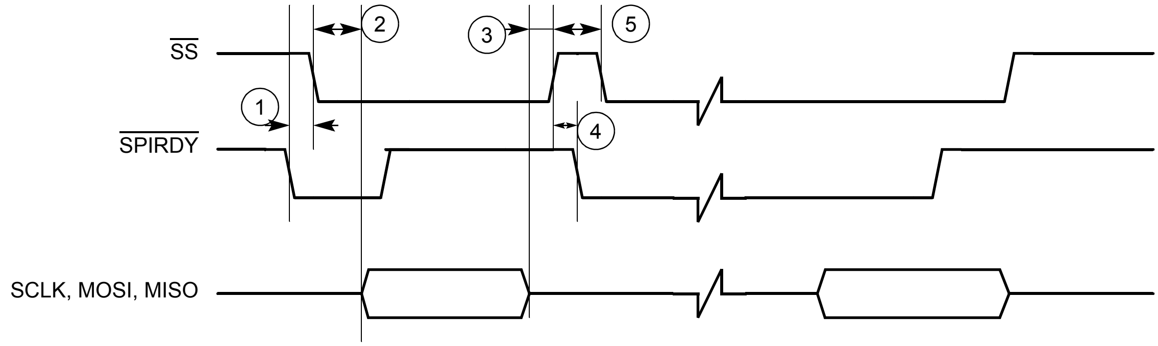


Figure 38. Master SPI Timing Diagram Using $\overline{\text{SPI\_RDY}}$ Edge Trigger

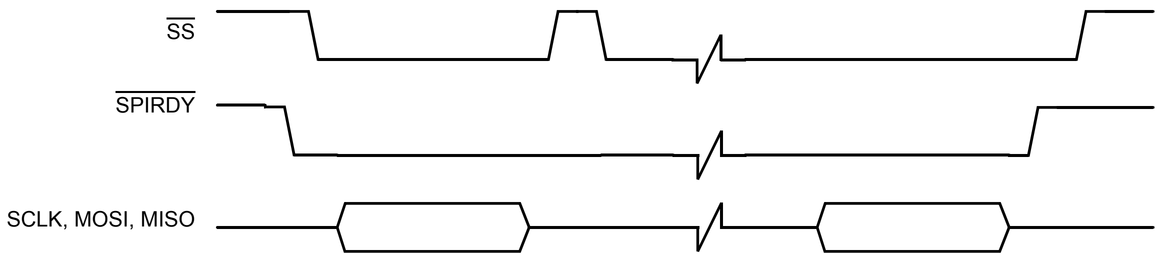


Figure 39. Master SPI Timing Diagram Using $\overline{\text{SPI\_RDY}}$ Level Trigger

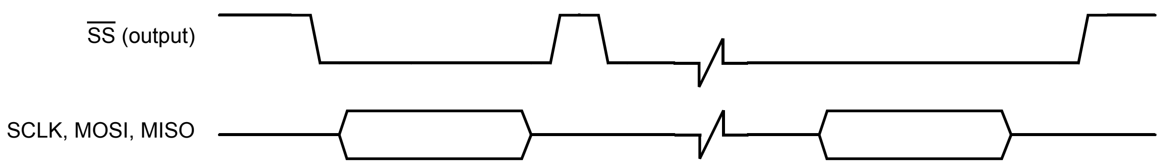


Figure 40. Master SPI Timing Diagram Ignore $\overline{\text{SPI\_RDY}}$ Level Trigger

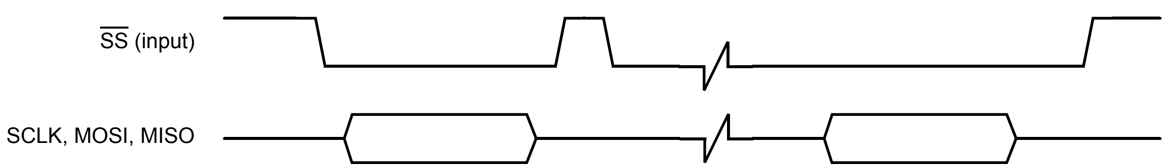


Figure 41. Slave SPI Timing Diagram FIFO Advanced by BIT COUNT

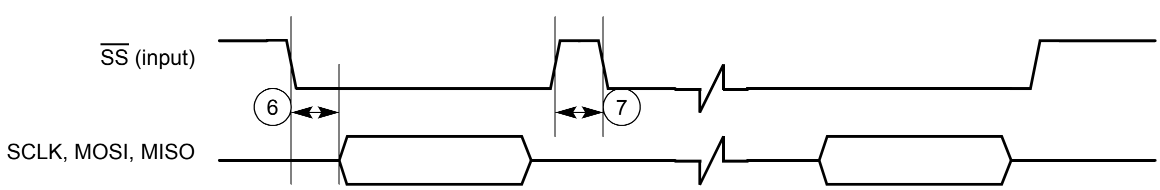


Figure 42. Slave SPI Timing Diagram FIFO Advanced by $\overline{\text{SS}}$ Rising Edge

Table 19. Timing Parameter Table for Figure 38 through Figure 42

Ref No.	Parameter	1.8 +/- 0.10V		Unit
		Minimum	Maximum	
1	$\overline{\text{SPI\_RDY}}$ to $\overline{\text{SS}}$ output low	2T [1]	—	ns
2	$\overline{\text{SS}}$ output low to first SCLK edge	3·Tsclk [2]	—	ns
3	Last SCLK edge to $\overline{\text{SS}}$ output high	2·Tsclk	—	ns
4	$\overline{\text{SS}}$ output high to $\overline{\text{SPI\_RDY}}$ low	0	—	ns
5	$\overline{\text{SS}}$ output pulse width	Tsclk + WAIT [3]	—	ns
6	$\overline{\text{SS}}$ input low to first SCLK edge	T	—	ns
7	$\overline{\text{SS}}$ input pulse width	T	—	ns

1. T = CSPI system clock period (PERCLK2)
2. Tsclk = Period of SCLK
3. WAIT = Number of bit clocks (SCLK) or 32.768 KHz clocks per Sample Period Control Register

3.14 LCD Controller

This section includes timing diagrams for the LCD controller. For detailed timing diagrams of the LCD Controller with various display configurations, refer to the LCD controller chapter of the *MC9328MX1 Reference Manual*.

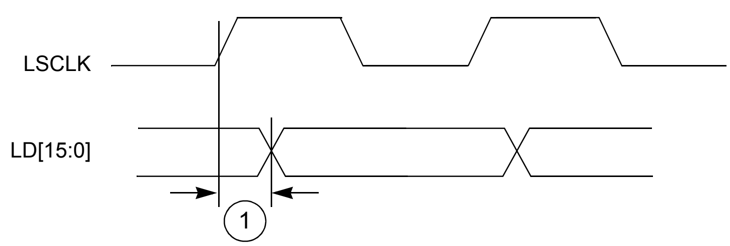


Figure 43. SCLK to LD Timing Diagram

Table 20. LCDC SCLK Timing Parameter Table

Ref No.	Parameter	1.8 V		Unit
		Minimum	Maximum	
1	SCLK to LD valid	—	2	ns

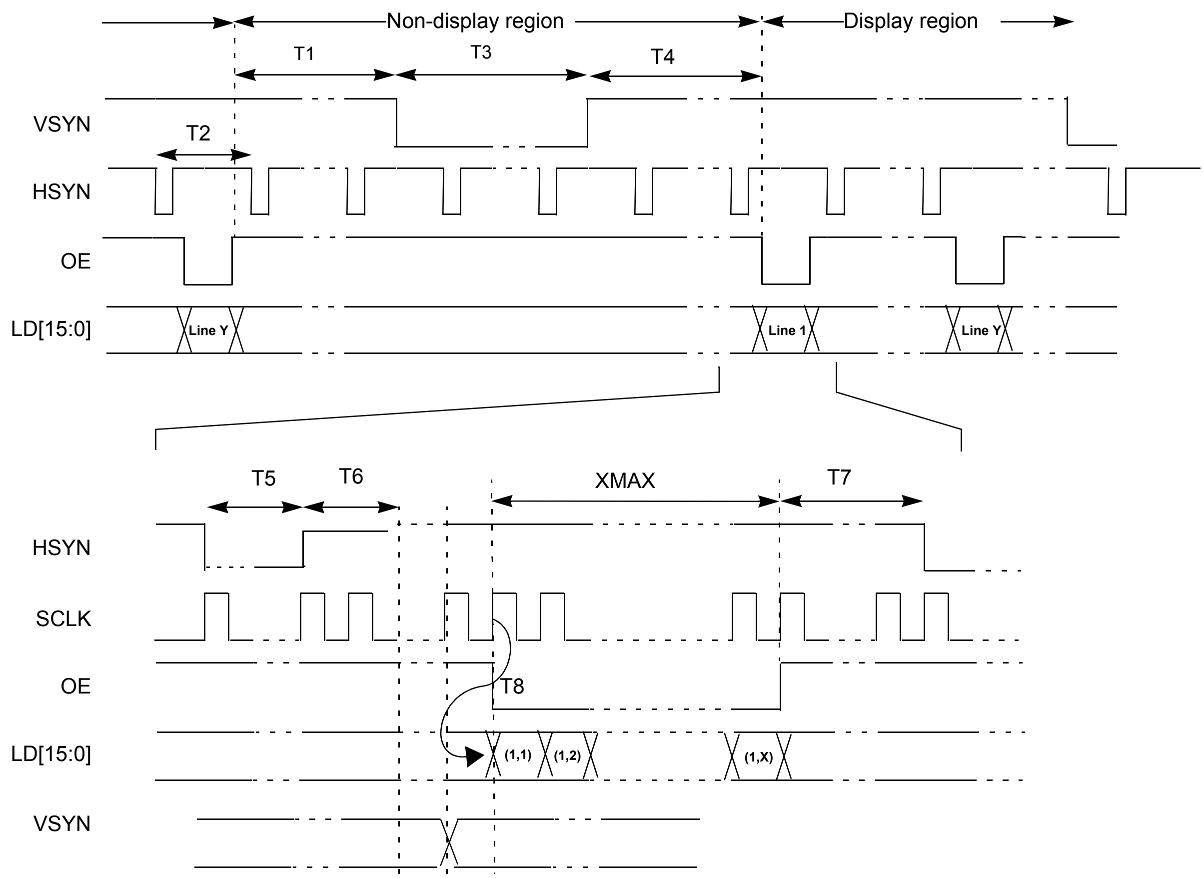


Figure 44. 4/8/16 Bit/Pixel TFT Color Mode Panel Timing

Table 21. 4/8/16 Bit/Pixel TFT Color Mode Panel Timing

Symbol	Description	Minimum	Corresponding Register Value	Unit
T1	End of OE to beginning of VSYN	T5+T6 +T7+T9	(VWAIT1·T2)+T5+T6+T7+T9	Ts
T2	HSYN period	XMAX+5	XMAX+T5+T6+T7+T9+T10	Ts
T3	VSYN pulse width	T2	VWIDTH·(T2)	Ts
T4	End of VSYN to beginning of OE	2	VWAIT2·(T2)	Ts
T5	HSYN pulse width	1	HWIDTH+1	Ts
T6	End of HSYN to beginning to T9	1	HWAIT2+1	Ts
T7	End of OE to beginning of HSYN	1	HWAIT1+1	Ts
T8	SCLK to valid LD data	-3	3	ns
T9	End of HSYN idle2 to VSYN edge (for non-display region)	2	2	Ts
T9	End of HSYN idle2 to VSYN edge (for Display region)	1	1	Ts

Table 21. 4/8/16 Bit/Pixel TFT Color Mode Panel Timing (Continued)

Symbol	Description	Minimum	Corresponding Register Value	Unit
T10	VSYN to OE active (Sharp = 0), when VWAIT2 = 0	1	1	Ts
T10	VSYN to OE active (Sharp = 1) when VWAIT2 = 0	2	2	Ts

Note:

- Ts is the SCLK period which equals LCDC_CLK / (PCD + 1). Normally LCDC_CLK = 15ns.
- VSYN, HSYN and OE can be programmed as active high or active low. In Figure 44, all 3 signals are active low.
- The polarity of SCLK and LD[15:0] can also be programmed.
- SCLK can be programmed to be deactivated during the VSYN pulse or the OE deasserted period. In Figure 44, SCLK is always active.
- For T9 non-display region, VSYN is non-active. It is used as an reference.
- XMAX is defined in pixels.

3.15 Multimedia Card/Secure Digital Host Controller

The DMA interface block controls all data routing between the external data bus (DMA access), internal MMC/SD module data bus, and internal system FIFO access through a dedicated state machine that monitors the status of FIFO content (empty or full), FIFO address, and byte/block counters for the MMC/SD module (inner system) and the application (user programming).

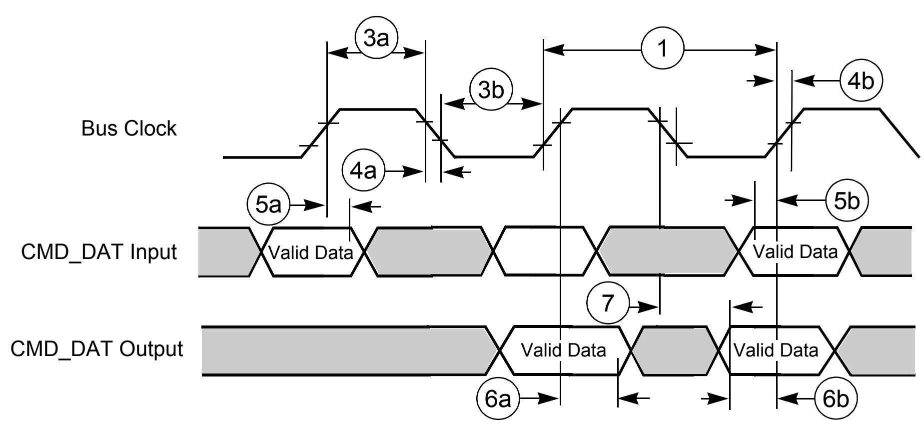


Figure 45. Chip-Select Read Cycle Timing Diagram

Table 22. SDHC Bus Timing Parameter Table

Ref No.	Parameter	1.8 +/- 0.10V		Unit
		Minimum	Maximum	
1	CLK frequency at Data transfer Mode (PP)[1] - 10/30 cards	0	25/5	MHz
2	CLK frequency at Identification Mode[2]	0	400	KHz
3a	Clock high time[1] - 10/30 cards	6/33	—	ns
3b	Clock low time[1] - 10/30 cards	15/75	—	ns
4a	Clock fall time[1] - 10/30 cards	—	10/50 (5.00)[3]	ns
4b	Clock rise time[1] - 10/30 cards	—	14/67 (6.67)[3]	ns
5a	Input hold time[3] - 10/30 cards	5.7/5.7	—	ns
5b	Input setup time[3] - 10/30 cards	5.7/5.7	—	ns
6a	Output hold time[3] - 10/30 cards	5.7/5.7	—	ns
6b	Output setup time[3] - 10/30 cards	5.7/5.7	—	ns
7	Output delay time[3]	0	16	ns

1. $C_L \leq$ 100 pF / 250 pF (10/30 cards)
2. $C_L \leq$ 250 pF (21 cards)
3. $C_L \leq$ 25 pF (1 card)

3.15.1 Command Response Timing on MMC/SD Bus

The card identification and card operation conditions timing are processed in open-drain mode. The card response to the host command starts after exactly N_{ID} clock cycles. For the card address assignment, SET_RCA is also processed in the open-drain mode. The minimum delay between the host command and card response is NCR clock cycles as illustrated in Figure 46. The symbols for Figure 46 through Figure 50 are defined in Table 23.

Table 23. State Signal Parameters for Figure 46 through Figure 50

Card Active		Host Active	
Symbol	Definition	Symbol	Definition
Z	High impedance state	S	Start bit (0)
D	Data bits	T	Transmitter bit (Host = 1, Card = 0)
*	Repetition	P	One-cycle pull-up (1)
CRC	Cyclic redundancy check bits (7 bits)	E	End bit (1)

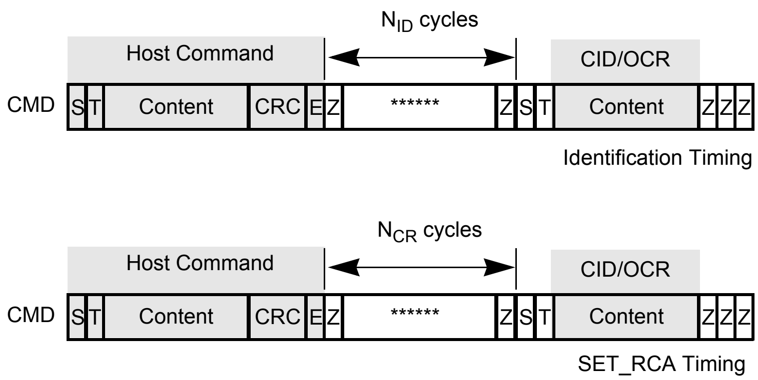


Figure 46. Timing Diagrams at Identification Mode

After a card receives its RCA, it will switch to data transfer mode. As shown on the first diagram in Figure 47 on page 59, SD_CMD lines in this mode are driven with push-pull drivers. The command is followed by a period of two Z bits (allowing time for direction switching on the bus) and then by P bits pushed up by the responding card. The other two diagrams show the separating periods N_{RC} and N_{CC}.

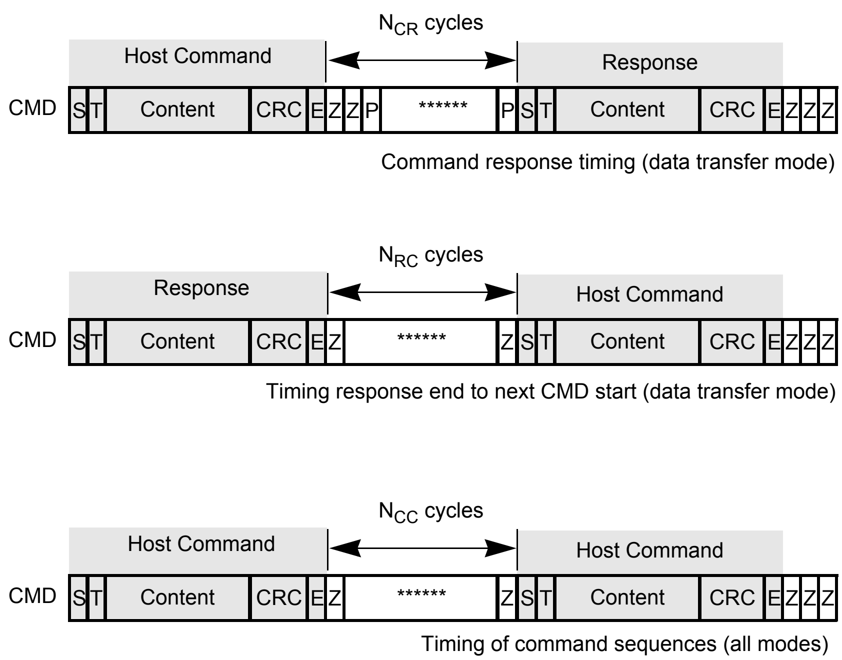


Figure 47. Timing Diagrams at Data Transfer Mode

Figure 48 on page 60 shows basic read operation timing. In a read operation, the sequence starts with a single block read command (which specifies the start address in the argument field). The response is sent on the SD_CMD lines as usual. Data transmission from the card starts after the access time delay N_{AC}, beginning from the last bit of the read command. If the system is in multiple block read mode, the card sends a continuous flow of data blocks with distance N_{AC} until the card sees a stop transmission command. The data stops two clock cycles after the end bit of the stop command.

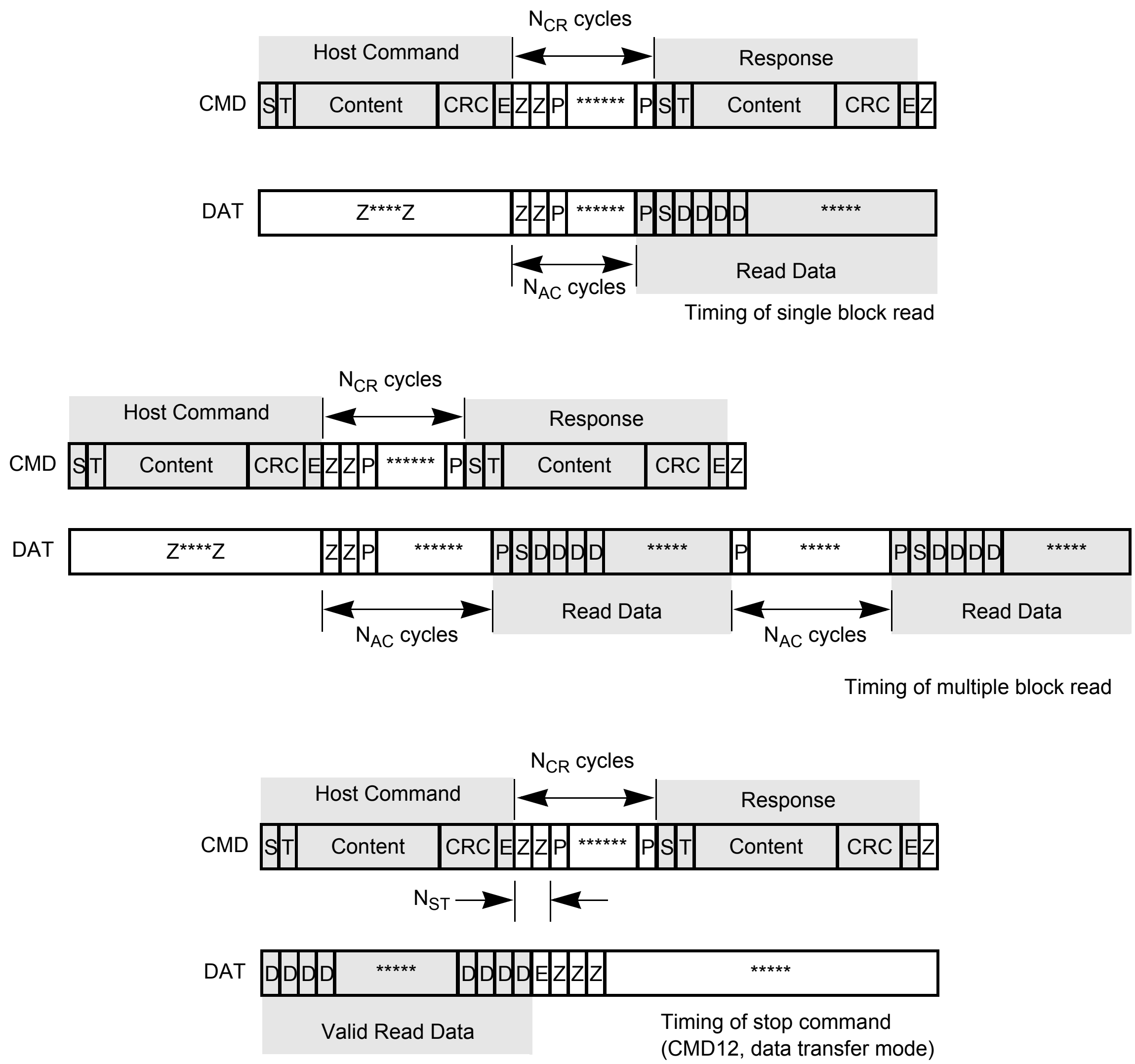


Figure 48. Timing Diagrams at Data Read

Figure 49 on page 61 shows the basic write operation timing. As with the read operation, after the card response, the data transfer starts after N_{WR} cycles. The data is suffixed with CRC check bits to allow the card to check for transmission errors. The card sends back the CRC check result as a CC status token on the data line. If there was a transmission error, the card sends a negative CRC status (101); otherwise, a positive CRC status (010) is returned. The card expects a continuous flow of data blocks if it is configured to multiple block mode, with the flow terminated by a stop transmission command.

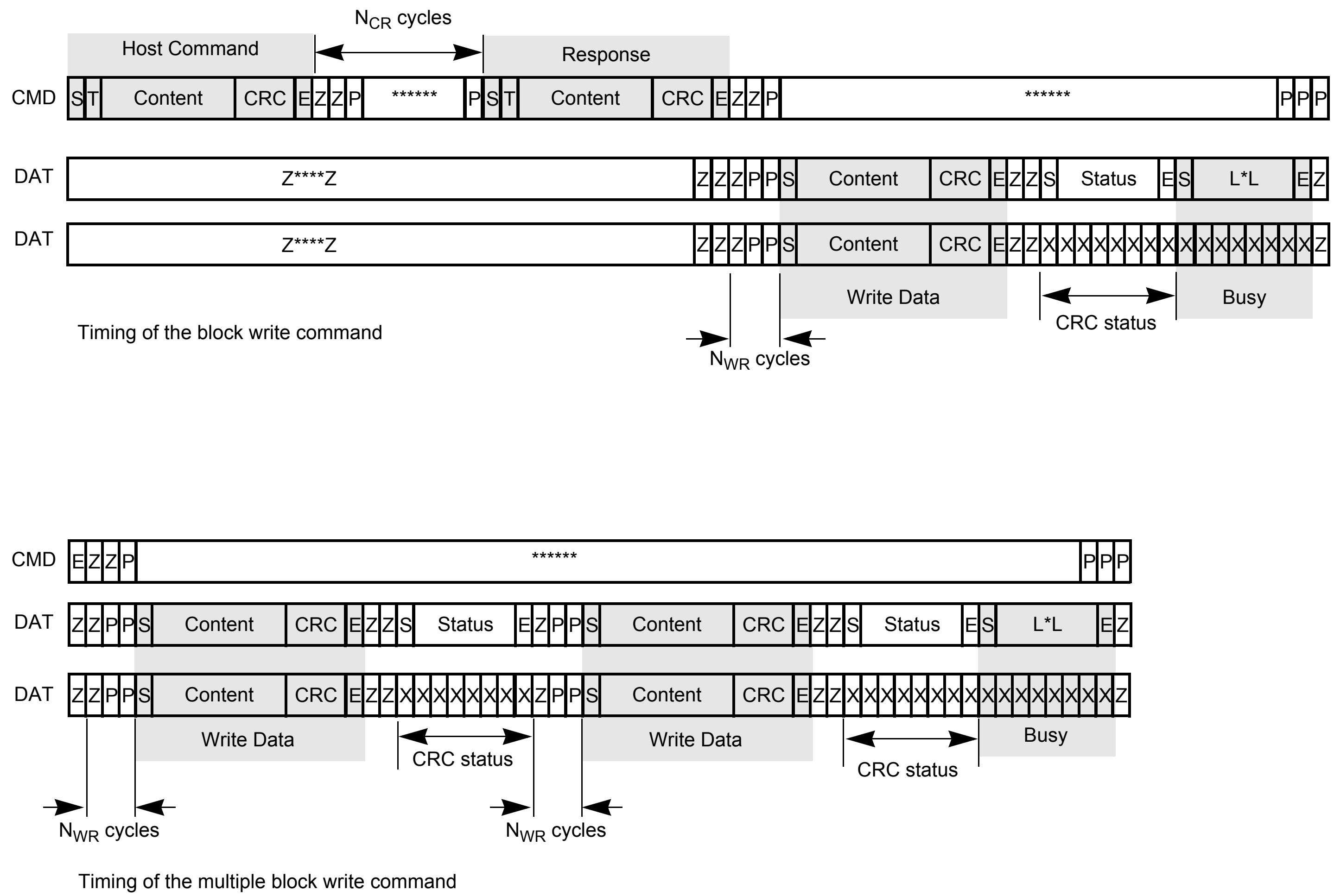


Figure 49. Timing Diagrams at Data Write

The stop transmission command may occur while the card is in different states. Figure 50 shows the different scenarios on the bus.

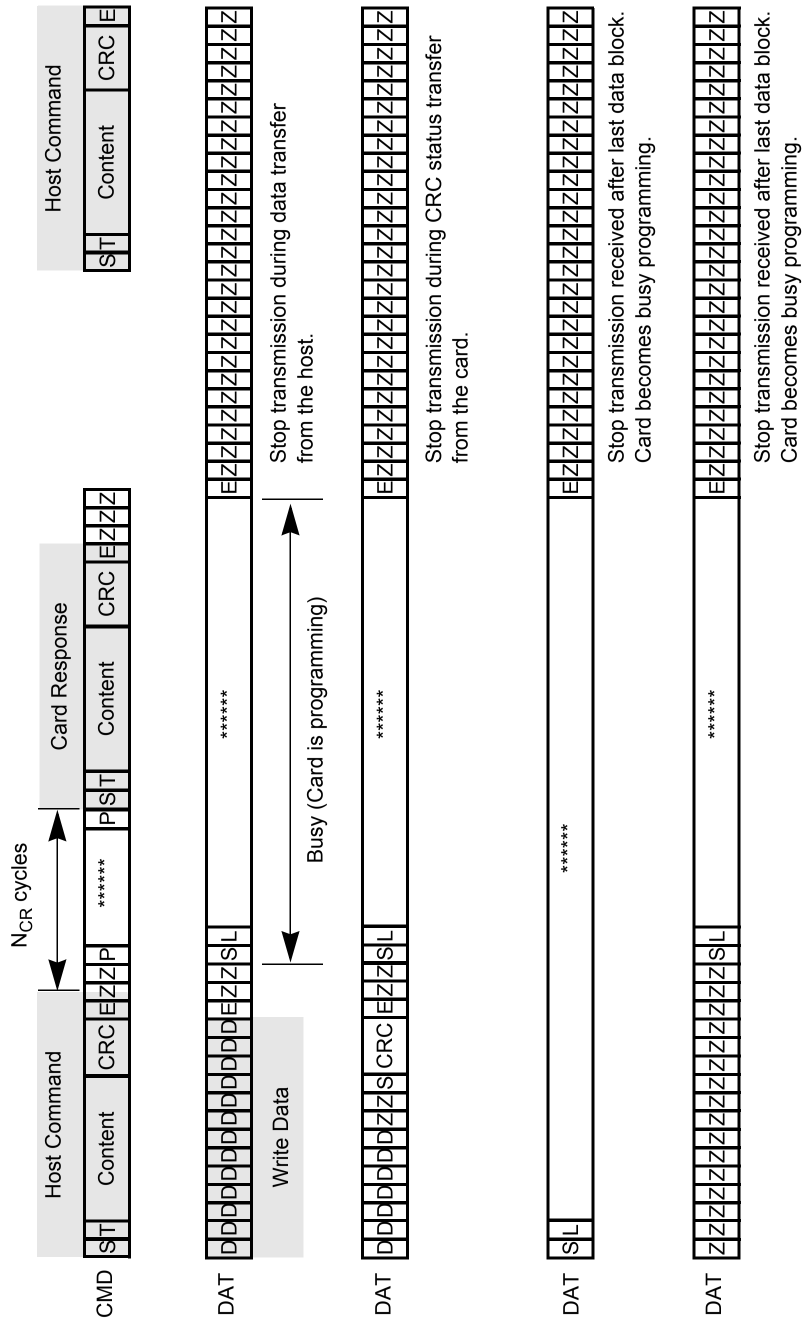


Figure 50. Stop Transmission During Different Scenarios

Table 24. Timing Values for Figure 46 through Figure 50

Parameter	Symbol	Minimum	Maximum	Unit	Remark
MMC/SD bus clock, CLK (All values are referred to minimum (VIH) and maximum (VIL)					
Command response cycle	NCR	2	64	clock cycles	—
Identification response cycle	NID	5	5	clock cycles	—
Access time delay cycle	NAC	2	TAAC + NSAC	clock cycles	—
Command read cycle	NRC	8	—	clock cycles	—
Command-command cycle	NCC	8	—	clock cycles	—
Command write cycle	NWR	2	—	clock cycles	—
Stop transmission cycle	NST	2	2	clock cycles	—
TAAC: Data read access time -1 defined in CSD register bit[119:112] NSAC: Data read access time -2 in CLK cycles (NSAC·100) defined in CSD register bit[111:104]					

3.15.1.1 SDIO-IRQ and ReadWait Service Handling

In SDIO, there will be a 1-bit or 4-bit interrupt response from the SDIO peripheral card. In 1-bit mode, the interrupt response is simply that the SD_DAT[1] line is held low. The SD_DAT[1] line is not used as data in this mode. The memory controller generates an interrupt according to this low and the system interrupt will continue until the source is removed (SD_DAT[1] returns to its high level).

In 4-bit mode, the interrupt is less simple. The interrupt triggers at a particular period called the "Interrupt Period" during the data access, and the controller must sample SD_DAT[1] during this short period to determine the IRQ status of the attached card. The interrupt period only happens at the boundary of each block (512 bytes).

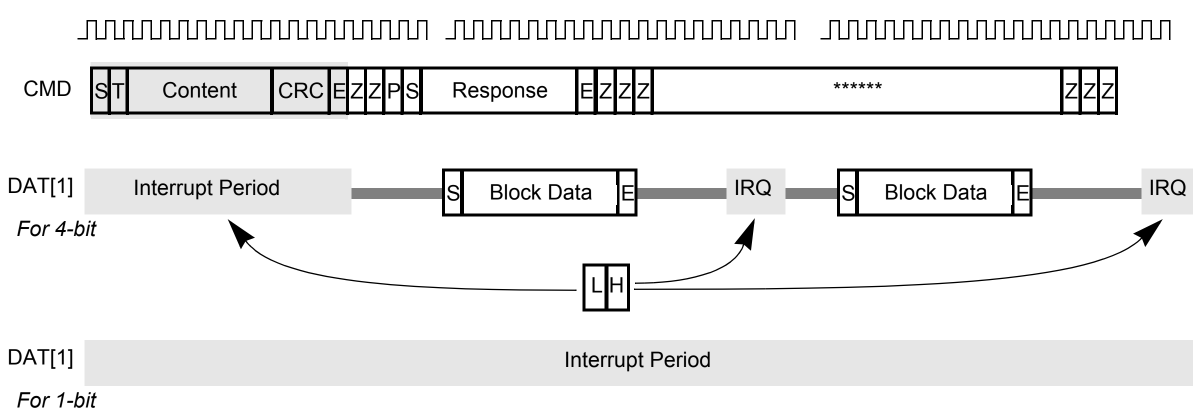


Figure 51. SDIO IRQ Timing Diagram

ReadWait is another feature in SDIO. It allows the user to submit command(s) during the data transfer. In this mode, the block will temporarily pause the data transfer operation counter and related status, but keep the clock running, and allow the user to submit commands as normal. After all commands have been submitted, the user can switch back to the data transfer operation and all counter and status values will be resumed as access continues.

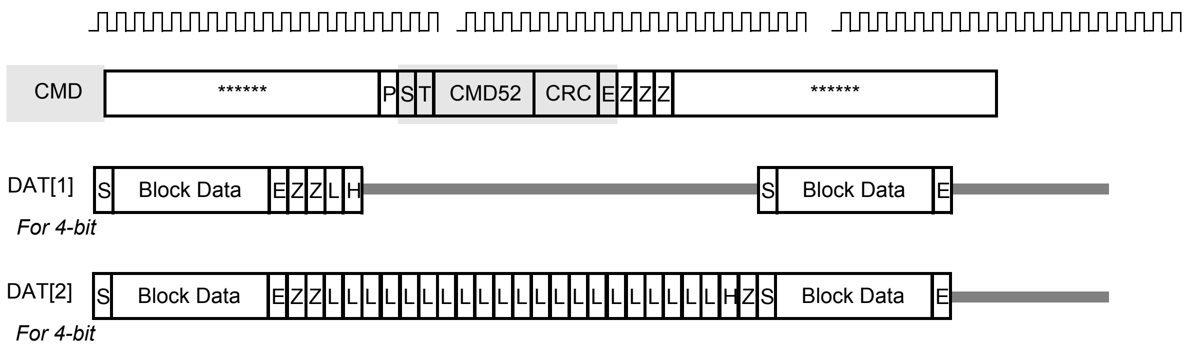


Figure 52. SDIO ReadWait Timing Diagram

3.16 Memory Stick Host Controller

The Memory Stick protocol requires three interface signal line connections for data transfers: MS_BS, MS_SDIO, and MS_SCLKO (or MS_SCLKI). Communication is always initiated by the MSHC and operates the bus in either four-state or two-state access mode.

The MS_BS signal classifies data on the SDIO into one of four states (BS0, BS1, BS2, or BS3) according to its attribute and transfer direction. BS0 is the INT transfer state, and during this state no packet transmissions occur. During the BS1, BS2, and BS3 states, packet communications are executed. The BS1, BS2, and BS3 states are regarded as one packet length and one communication transfer is always completed within one packet length (in four-state access mode).

The Memory Stick usually operates in four state access mode and in BS1, BS2, and BS3 bus states. When an error occurs during packet communication, the mode is shifted to two-state access mode, and the BS0 and BS1 bus states are automatically repeated to avoid a bus collision on the SDIO.

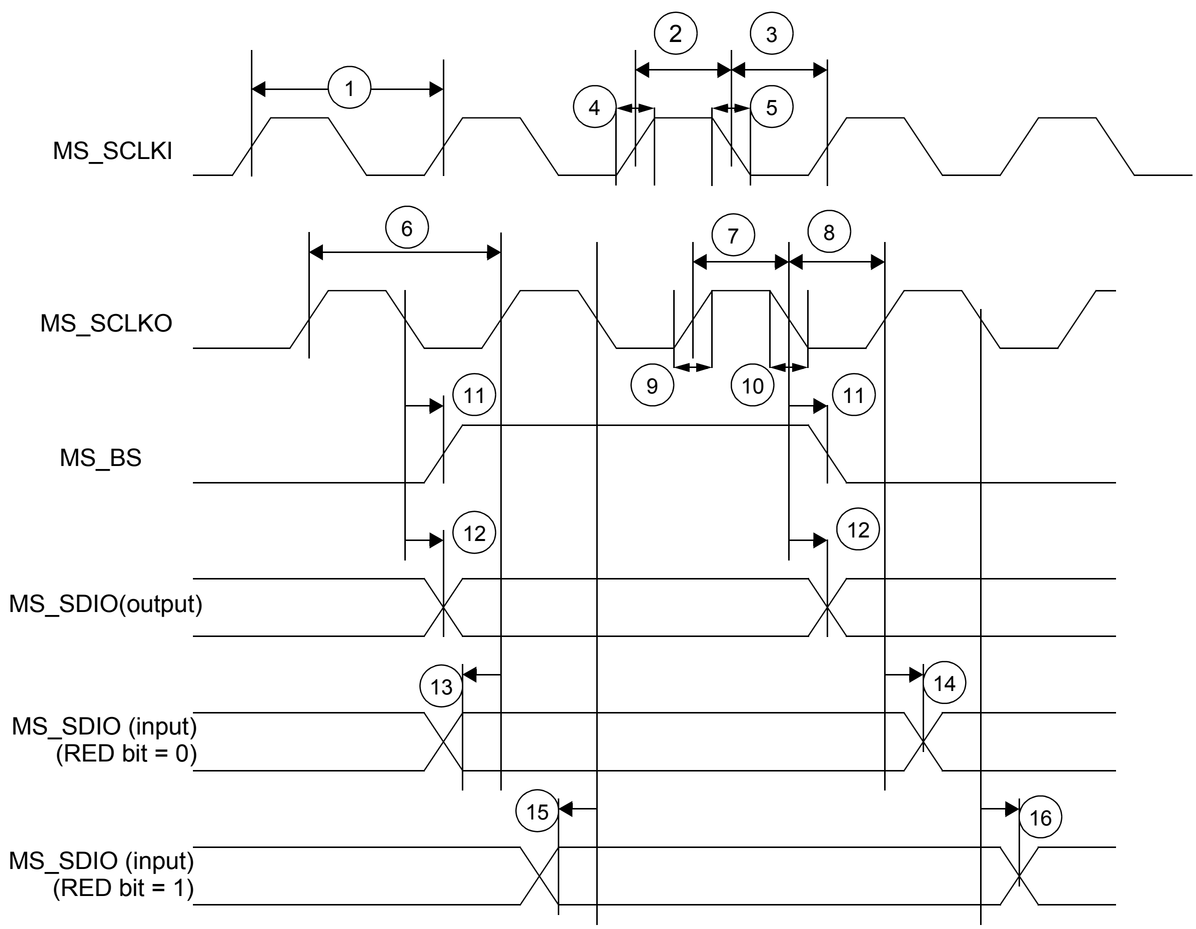


Figure 53. MSHC Signal Timing Diagram

Table 3-25. MSHC Signal Timing Parameter Table

Ref No.	Characteristic	1.8 +/- 0.10V		Unit
		Minimum	Maximum	
1	MS_SCLKI frequency	-	48	MHz
2	MS_SCLKI high pulse width	7	-	ns
3	MS_SCLKI low pulse width	16	-	ns
4	MS_SCLKI rise time	-	6.67	ns
5	MS_SCLKI fall time	-	5	ns
6	MS_SCLKO frequency[1]	-	50	MHz
7	MS_SCLKO high pulse width[1]	6.67	-	ns
8	MS_SCLKO low pulse width[1]	10.5	-	ns
9	MS_SCLKO rise time[1]	-	6.67	ns
10	MS_SCLKO fall time[1]	-	5	ns
11	MS_BS delay time[1]	-	3.42	ns
12	MS_SDIO output delay time[1,2]	-	3.42	ns
13	MS_SDIO input setup time for MS_SCLKO rising edge (RED bit = 0)[3]	17.1	-	ns
14	MS_SDIO input hold time for MS_SCLKO rising edge (RED bit = 0)[3]	0	-	ns
15	MS_SDIO input setup time for MS_SCLKO falling edge (RED bit = 1)[4]	17.1	-	ns
16	MS_SDIO input hold time for MS_SCLKO falling edge (RED bit = 1)[4]	0	-	ns

1. Loading capacitor condition is less than or equal to 30pF
2. An external resistor (100 ~ 200 ohm) should be inserted in series to provide current control on the MS_SDIO pin, because of a possibility of signal conflict between the MS_SDIO pin and Memory Stick SDIO pin when the pin direction changes.
3. If the MSC2[RED] bit = 0, MSHC samples MS_SDIO input data at MS_SCLKO rising edge.
4. If the MSC2[RED] bit = 1, MSHC samples MS_SDIO input data at MS_SCLKO falling edge.

3.17 Pulse Width Modulator

The PWM can be programmed to select one of two clock signals as its source frequency. The selected clock signal is passed through a divider and a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

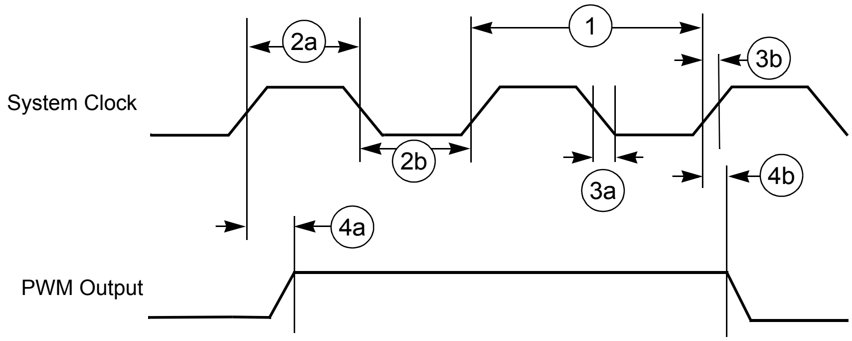


Figure 54. PWM Output Timing Diagram

Table 26. PWM Output Timing Parameter Table

Ref No.	Parameter	1.8 +/- 0.10V		Unit
		Minimum	Maximum	
1	System CLK frequency[1]	0	87	MHz
2a	Clock high time[1]	3.3	—	ns
2b	Clock low time[1]	7.5	—	ns
3a	Clock fall time[1]	—	5	ns
3b	Clock rise time[1]	—	6.67	ns
4a	Output delay time[1]	5.7	—	ns
4b	Output setup time[1]	5.7	—	ns

1. C_L of PWMO = 30 pF

3.18 SDRAM Memory Controller

A write to an address within the memory region initiates the program sequence. The first command issued to the SyncFlash is Load Command Register. A [7:0] determine which operation the command performs. For this write setup operation, an address of 0x40 is hardware generated. The bank and other address lines are driven with the address to be programmed. The next command is Active which registers the row address and confirms the bank address. The third command supplies the column address, re-confirms the bank address, and supplies the data to be written. SyncFlash does not support burst writes, therefore a Burst Terminate command is not required.

A read to the memory region initiates the status read sequence. The first command issued to the SyncFlash is the Load Command Register with A [7:0] set to 0x70 which corresponds to the Read Status Register operation. The bank and other address lines are driven to the selected address. The second command is Active which sets up the status register read. The bank and row addresses are driven during this command. The third command of the triplet is Read. Bank and column addresses are driven on the address bus during this command. Data is returned from memory on the low order 8 data bits following the CAS latency.

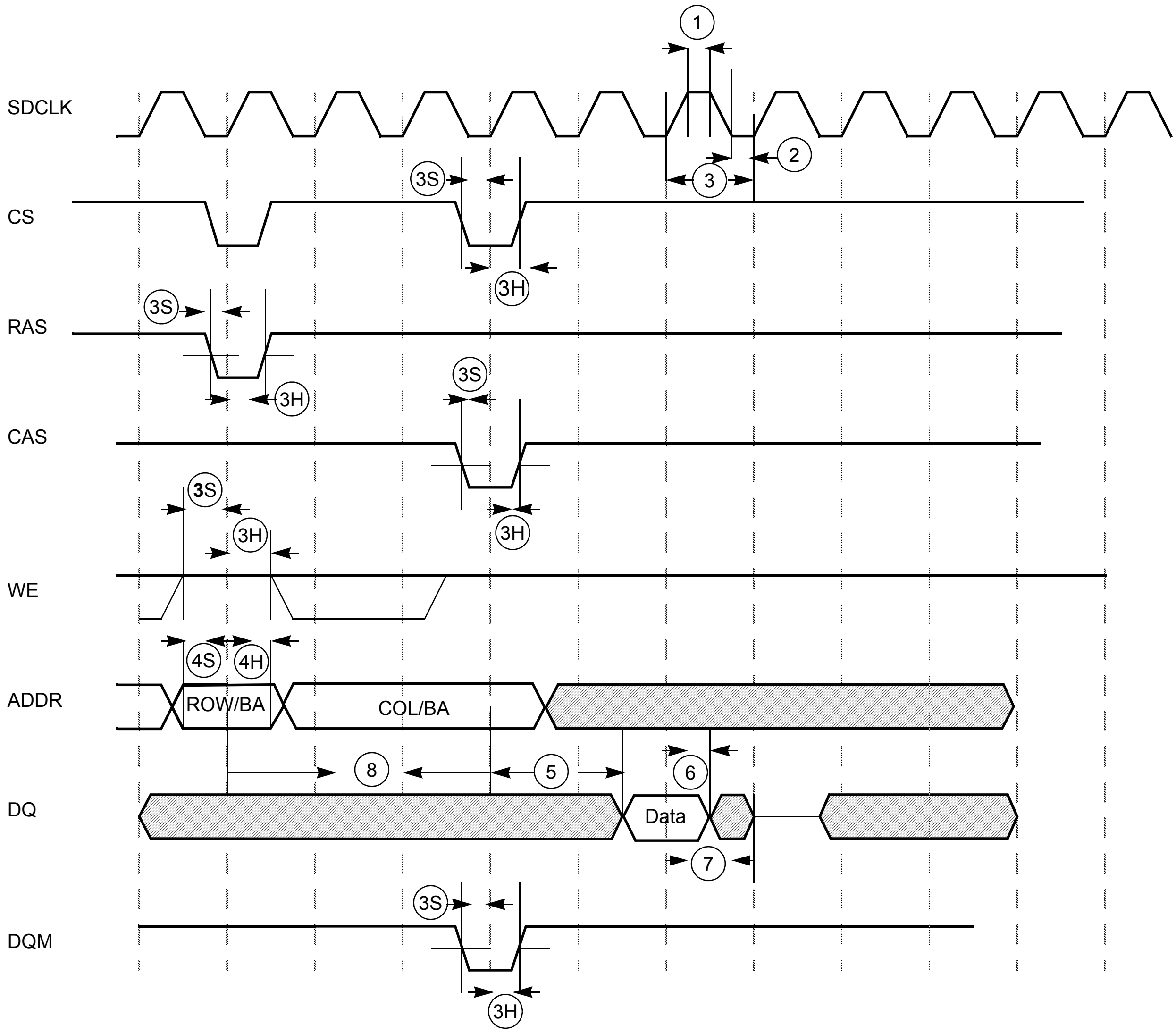


Figure 55. SDRAM/SyncFlash Read Cycle Timing Diagram

Table 27. SDRAMC Timing Parameter Table

Ref No.	Parameter	1.8V		Unit
		Minimum	Maximum	
1	SDRAM clock high-level width	2.6	—	ns
2	SDRAM clock low-level width	6	—	ns
3	SDRAM clock cycle time	11.4	—	ns
3S	CS, RAS, CAS, WE, DQM setup time	3.42	—	ns
3H	CS, RAS, CAS, WE, DQM hold time	2.28	—	ns
4S	Address setup time	3.42	—	ns
4H	Address hold time	2.28	—	ns

Table 27. SDRAMC Timing Parameter Table (Continued)

Ref No.	Parameter	1.8V		Unit
		Minimum	Maximum	
5	SDRAM access time (CL = 3)	—	6.84	ns
5	SDRAM access time (CL = 2)	—	6.84	ns
5	SDRAM access time (CL = 1)	—	—	ns
6	Data out hold time	2.85	—	ns
7	Data out high-impedance time (CL = 3)	—	6.84	ns
7	Data out high-impedance time (CL = 2)	—	6.84	ns
7	Data out high-impedance time (CL = 1)	—	—	ns
8	Active to read/write command period (RC = 1)	t_{RCD}	—	ns

Note: CKE is high during the read/write cycle.

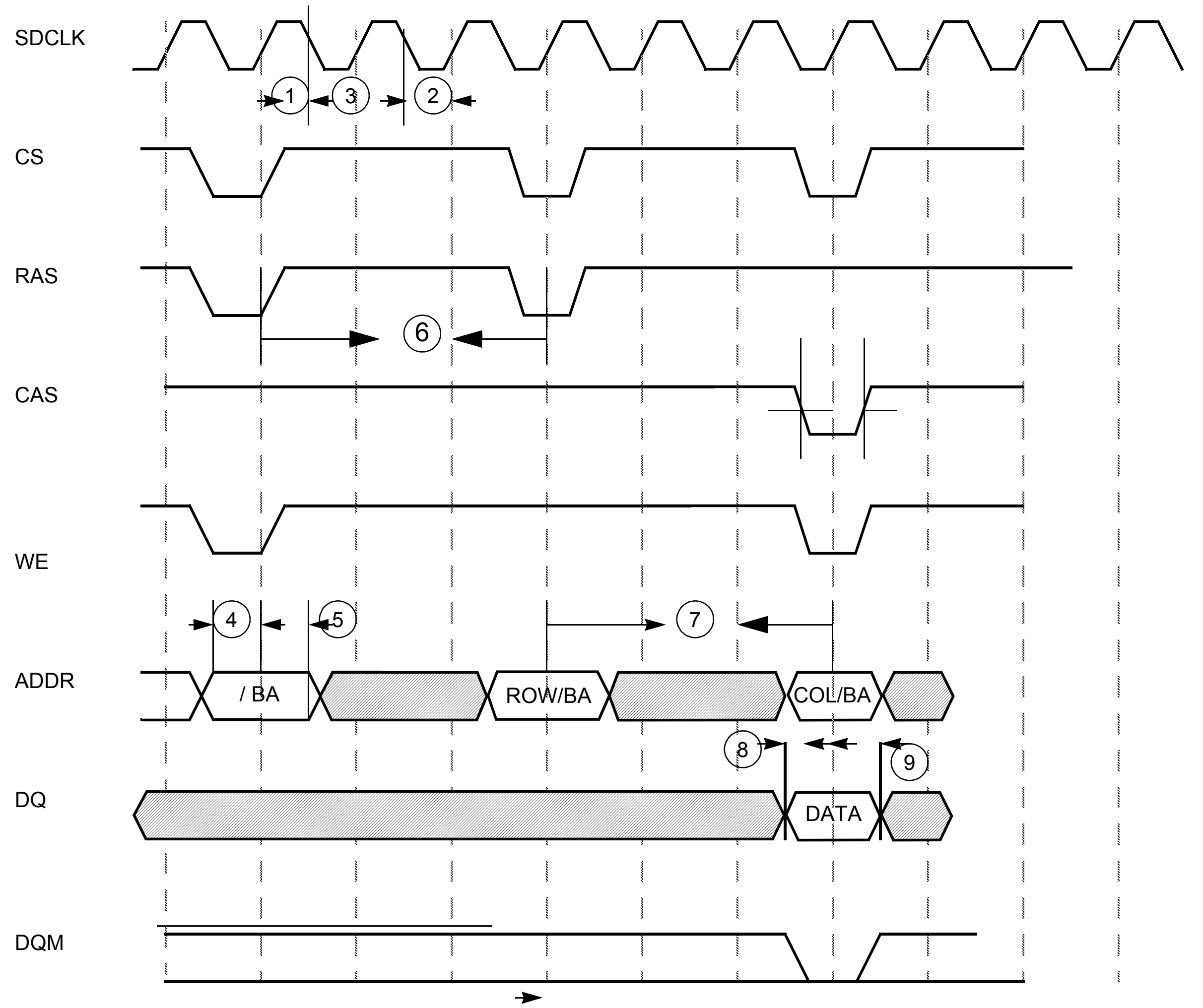


Figure 56. SDRAM/SyncFlash Write Cycle Timing Diagram

Table 28. SDRAM Write Timing Parameter Table

Ref No.	Parameter	1.8V		Unit
		Minimum	Maximum	
1	SDRAM clock high-level width	2.66	—	ns
2	SDRAM clock low-level width	6	—	ns
3	SDRAM clock cycle time	11.4	—	ns
4	Address setup time	3.42	—	ns
5	Address hold time	2.28	—	ns
6	Precharge cycle period	t_{RP}	—	ns
7	Active to read/write command delay	t_{RCD}	—	ns
8	Data setup time	2.28	—	ns

Table 28. SDRAM Write Timing Parameter Table (Continued)

Ref No.	Parameter	1.8V Minimum	1.8V Maximum	Unit
9	Data hold time	2.28	—	ns

Note: Precharge cycle timing is included in the write timing diagram.

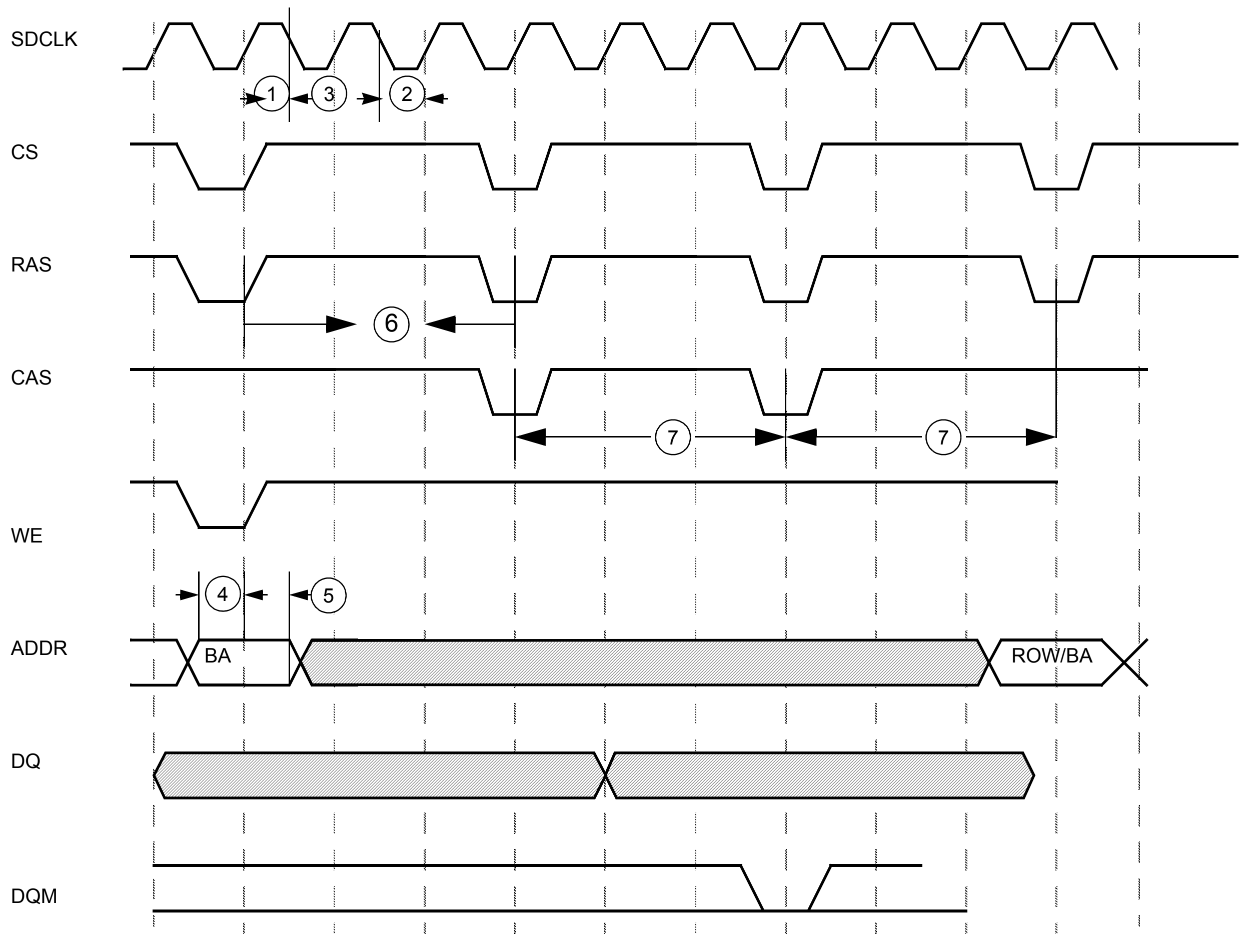


Figure 57. SDRAM Refresh Timing Diagram

Table 29. SDRAM Refresh Timing Parameter Table

Ref No.	Parameter	1.8V Minimum	1.8V Maximum	Unit
1	SDRAM clock high-level width	2.67	—	ns
2	SDRAM clock low-level width	6	—	ns
3	SDRAM clock cycle time	11.4	—	ns
4	Address setup time	3.42	—	ns

Table 29. SDRAM Refresh Timing Parameter Table (Continued)

Ref No.	Parameter	1.8V		Unit
		Minimum	Maximum	
5	Address hold time	2.28	—	ns
6	Precharge cycle period	t_{RP}	—	ns
7	Auto precharge command period	t_{RC}	—	ns

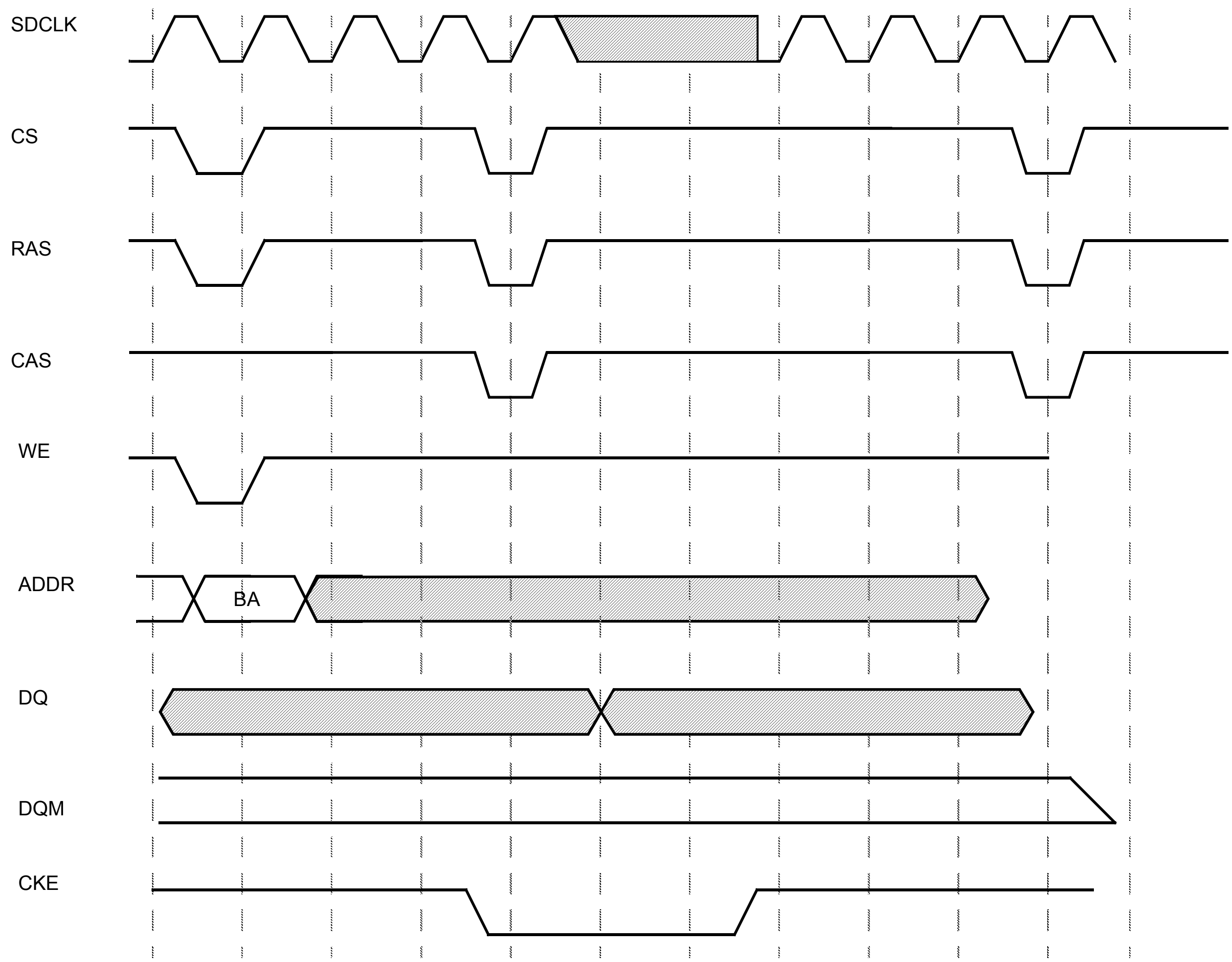


Figure 58. SDRAM Self-Refresh Cycle Timing Diagram

3.19 USB Device Port

Four types of data transfer modes exist for the USB module: control transfers, bulk transfers, isochronous transfers and interrupt transfers. From the perspective of the USB module, the interrupt transfer type is identical to the bulk data transfer mode, and no additional hardware is supplied to support it. This section covers the transfer modes and how they work from the ground up.

Data moves across the USB in packets. Groups of packets are combined to form data transfers. The same packet transfer mechanism applies to bulk, interrupt, and control transfers. Isochronous data is also moved in the form of packets, but because isochronous pipes are given a fixed portion of the USB bandwidth at all times, there is no end-of-transfer.

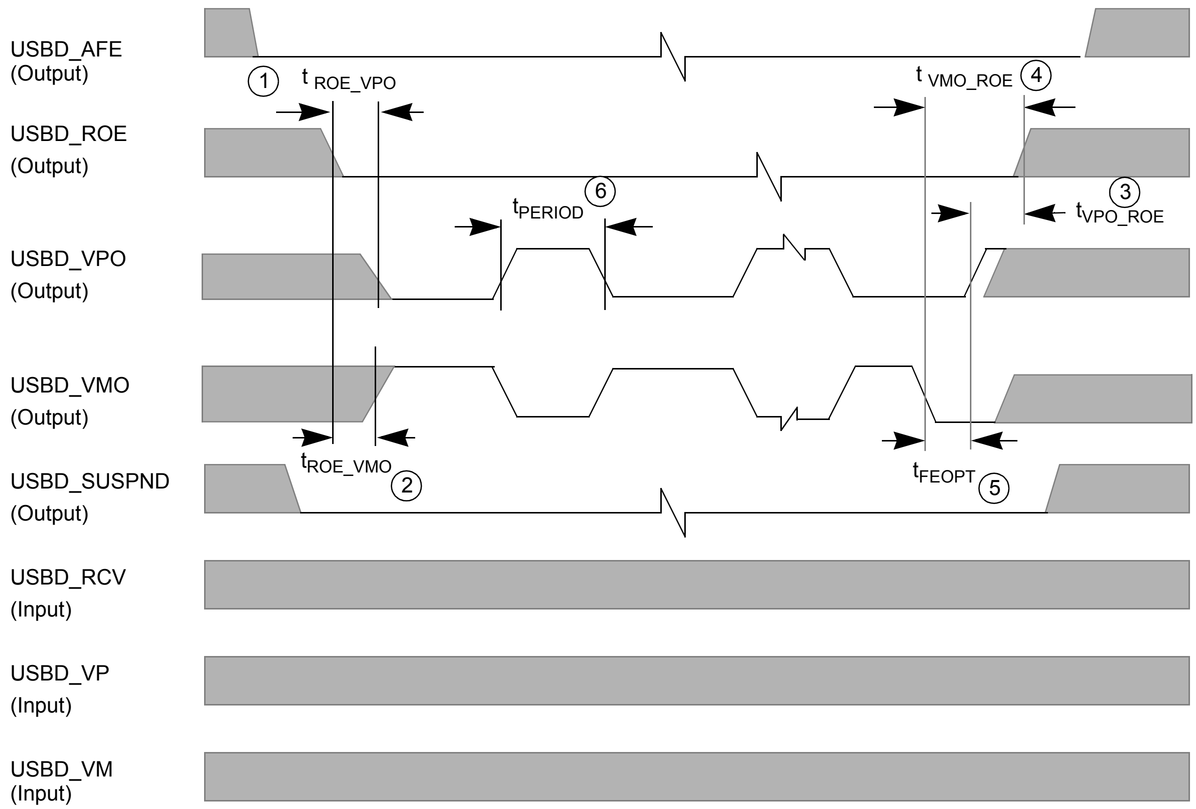


Figure 59. USB Device Timing Diagram for Data Transfer to USB Transceiver (TX)

Table 30. USB Device Timing Parameter Table for Data Transfer to USB Transceiver (TX)

Ref No.	Parameter	1.8 V		Unit
		Minimum	Maximum	
1	t_{ROE_VPO}; USBD_ROE active to USBD_VPO low	83.14	83.47	ns
2	t_{ROE_VMO}; USBD_ROE active to USBD_VMO high	81.55	81.98	ns
3	t_{VPO_ROE}; USBD_VPO high to USBD_ROE deactivated	83.54	83.8	ns
4	t_{VMO_ROE}; USBD_VMO low to USBD_ROE deactivated (includes SE0)	248.9	249.13	ns
5	t_{FEOPT}; SE0 interval of EOP	160	175	ns
6	t_{PERIOD}; Data transfer rate	11.97	12.03	Mb/s

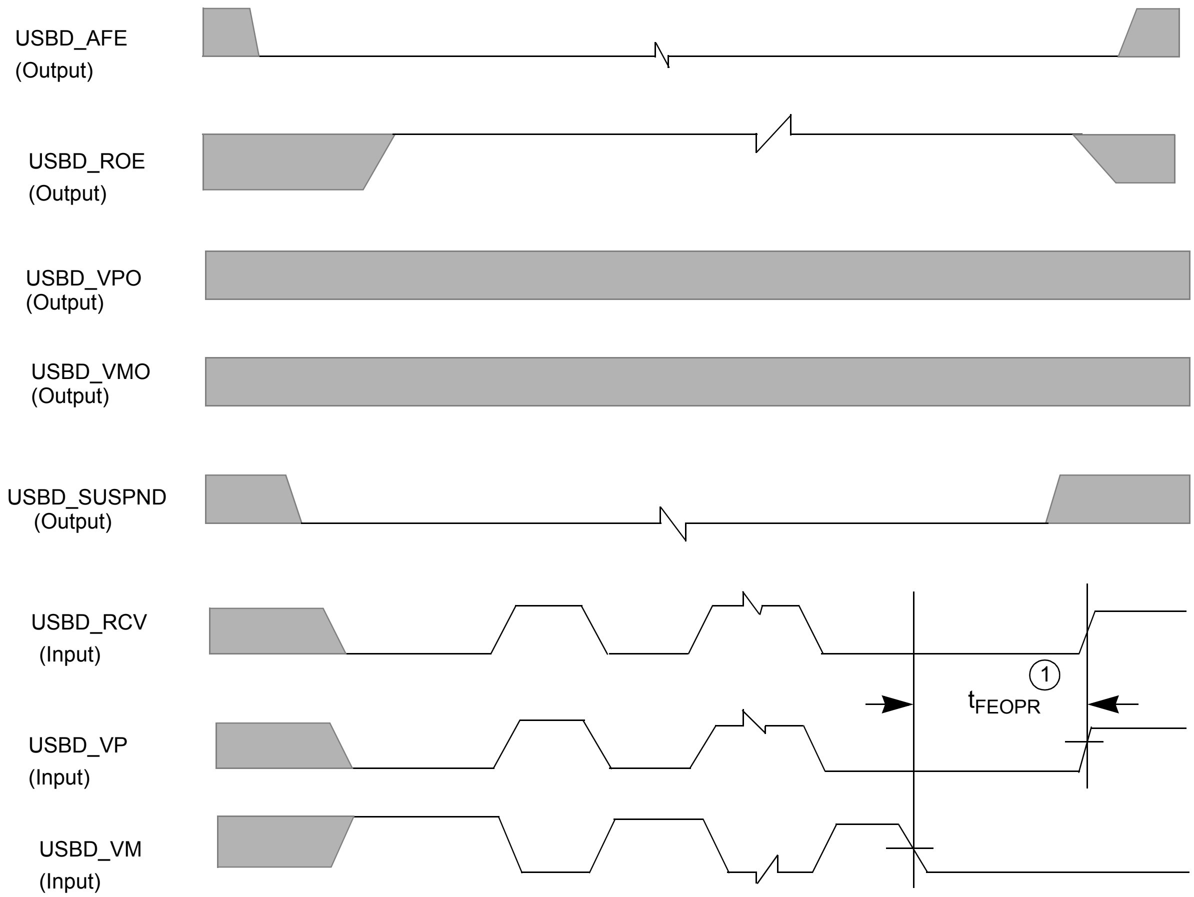


Figure 60. USB Device Timing Diagram for Data Transfer from USB Transceiver (RX)

Table 31. USB Device Timing Parameter Table for Data Transfer from USB Transceiver (RX)

Ref No.	Parameter	1.8 V		Unit
		Minimum	Maximum	
1	t_{FEOPR}; Receiver SE0 interval of EOP	82	—	ns

3.20 I²C Module

The I²C communication protocol consists of six components: START, Data Source/Recipient, Data Direction, Slave Acknowledge, Data, Data Acknowledge, and STOP.

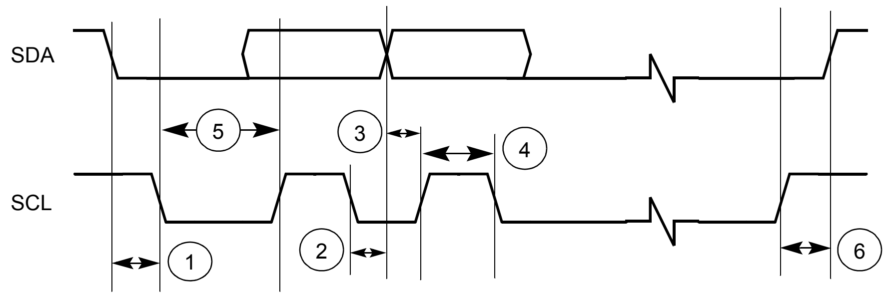


Figure 61. Definition of Bus Timing for I²C

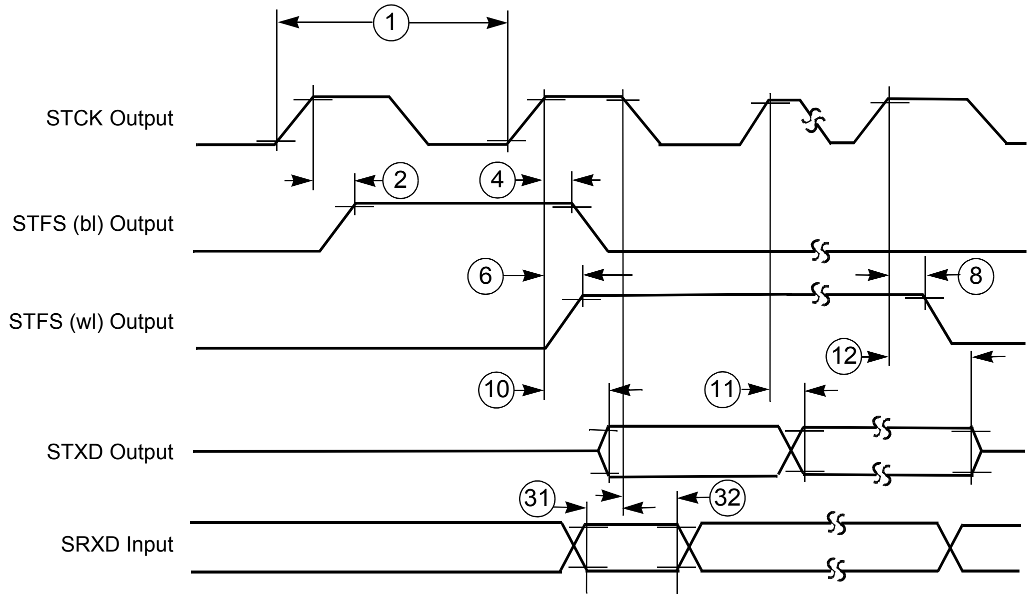
Table 32. I²C Bus Timing Parameter Table

Ref No.	Parameter	1.8 +/- 0.10V		Unit
		Minimum	Maximum	
1	Hold time (repeated) START condition	182	—	ns
2	Data hold time	0	171	ns
3	Data setup time	11.4	—	ns
4	HIGH period of the SCL clock	80	—	ns
5	LOW period of the SCL clock	480	—	ns
6	Setup time for STOP condition	182.4	—	ns

3.21 Synchronous Serial Interface (SSI)

The transmit and receive sections of the SSI can be synchronous or asynchronous. In synchronous mode, the transmitter and the receiver use a common clock and frame synchronization signal. In asynchronous mode, the transmitter and receiver each have their own clock and frame synchronization signals. Continuous or Gated clock mode can be selected. In continuous mode, the clock runs continuously. In gated clock mode, the clock functions only during transmission. The internal and external clock timing diagrams are shown in Figure 63 through Figure 65 on page 77.

Normal or network mode also can be selected. In normal mode, the SSI functions with one data word of I/O per frame. In network mode, a frame can contain between 2 and 32 data words. Network mode is typically used in star or ring-time division multiplex networks with other processors or codecs, allowing interface to time division multiplexed networks without additional logic. Use of the gated clock is not allowed in network mode. These distinctions result in the basic operating modes that allow the SSI to communicate with a wide variety of devices.



Note: SRXD input in synchronous mode only.

Figure 62. SSI Transmitter Internal Clock Timing Diagram

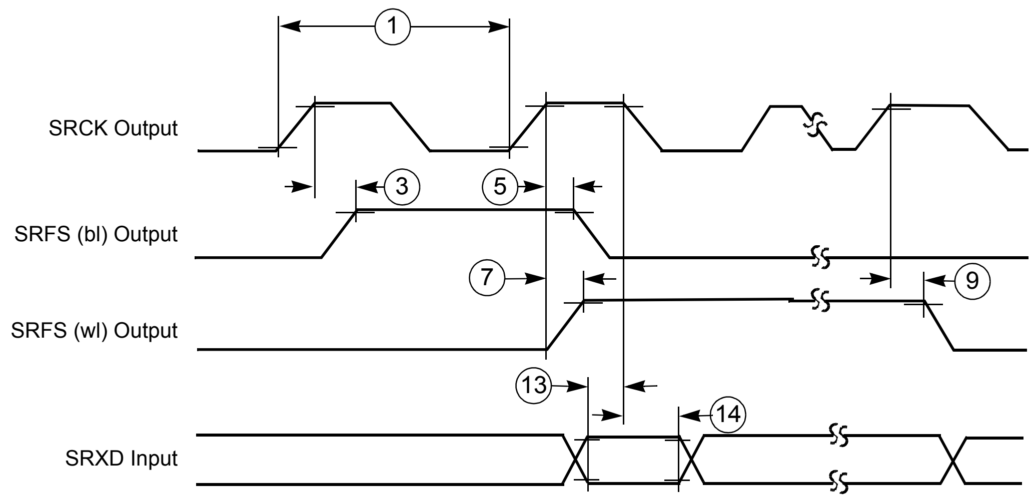
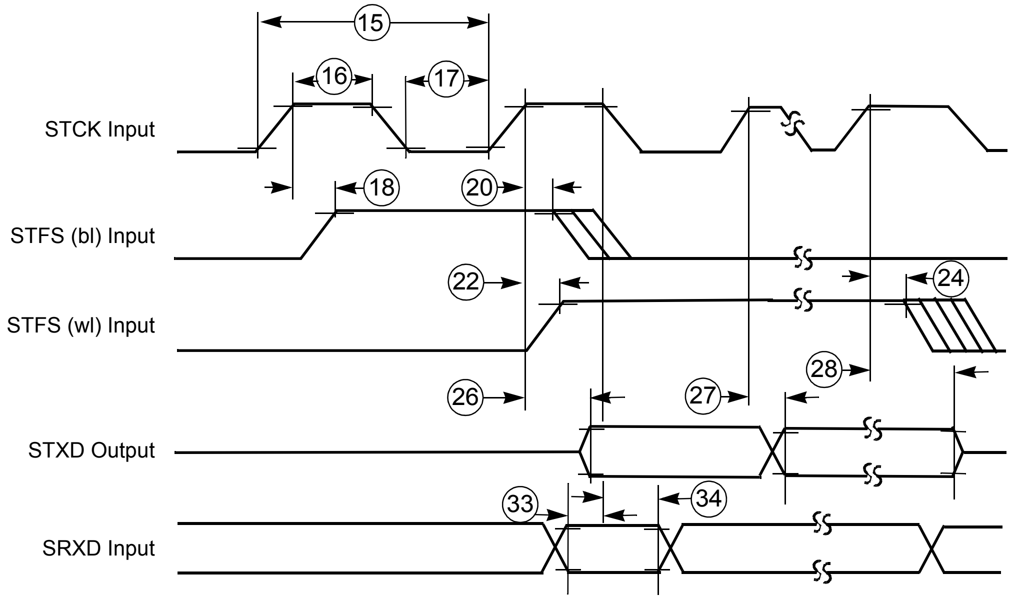


Figure 63. SSI Receiver Internal Clock Timing Diagram



Note: SRXD Input in Synchronous mode only

Figure 64. SSI Transmitter External Clock Timing Diagram

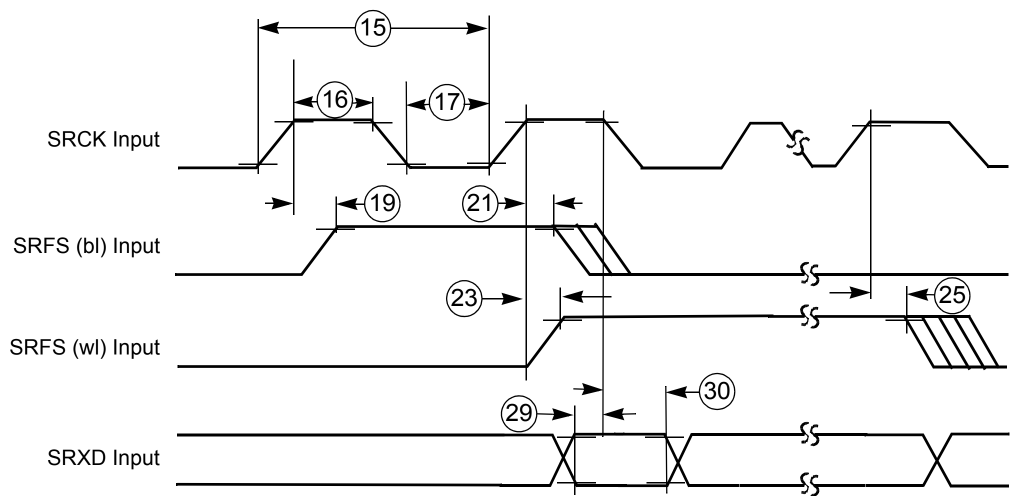


Figure 65. SSI Receiver External Clock Timing Diagram

Table 33. SSI (Port C Primary Function) Timing Parameter Table

Ref No.	Parameter	1.8 +/- 0.10V		Unit
		Minimum	Maximum	
Internal Clock Operation[1] (Port C Primary Function)[2]				
1	STCK/SRCK clock period[1]	95	—	ns
2	STCK high to STFS (bl) high[3]	1.5	4.5	ns
3	SRCK high to SRFS (bl) high[3]	-1.2	-1.7	ns

Table 33. SSI (Port C Primary Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 +/- 0.10V		Unit
		Minimum	Maximum	
4	STCK high to STFS (bl) low[3]	2.5	4.3	ns
5	SRCK high to SRFS (bl) low[3]	0.1	-0.8	ns
6	STCK high to STFS (wl) high[3]	1.48	4.45	ns
7	SRCK high to SRFS (wl) high[3]	-1.1	-1.5	ns
8	STCK high to STFS (wl) low[3]	2.51	4.33	ns
9	SRCK high to SRFS (wl) low[3]	0.1	-0.8	ns
10	STCK high to STXD valid from high impedance	14.25	15.73	ns
11a	STCK high to STXD high	0.91	3.08	ns
11b	STCK high to STXD low	0.57	3.19	ns
12	STCK high to STXD high impedance	12.88	13.57	ns
13	SRXD setup time before SRCK low	21.1	—	ns
14	SRXD hold time after SRCK low	0	—	ns
External Clock Operation (Port C Primary Function)[2]				
15	STCK/SRCK clock period[1]	92.8	—	ns
16	STCK/SRCK clock high period	27.1	—	ns
17	STCK/SRCK clock low period	61.1	—	ns
18	STCK high to STFS (bl) high[3]	—	92.8	ns
19	SRCK high to SRFS (bl) high[3]	—	92.8	ns
20	STCK high to STFS (bl) low[3]	—	92.8	ns
21	SRCK high to SRFS (bl) low[3]	—	92.8	ns
22	STCK high to STFS (wl) high[3]	—	92.8	ns
23	SRCK high to SRFS (wl) high[3]	—	92.8	ns
24	STCK high to STFS (wl) low[3]	—	92.8	ns
25	SRCK high to SRFS (wl) low[3]	—	92.8	ns
26	STCK high to STXD valid from high impedance	18.01	28.16	ns
27a	STCK high to STXD high	8.98	18.13	ns
27b	STCK high to STXD low	9.12	18.24	ns
28	STCK high to STXD high impedance	18.47	28.5	ns

Table 33. SSI (Port C Primary Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 +/- 0.10V		Unit
		Minimum	Maximum	
29	SRXD setup time before SRCK low	1.14	—	ns
30	SRXD hole time after SRCK low	0	—	ns
Synchronous Internal Clock Operation (Port C Primary Function)[2]				
31	SRXD setup before STCK falling	15.4	—	ns
32	SRXD hold after STCK falling	0	—	ns
Synchronous External Clock Operation (Port C Primary Function)[2]				
33	SRXD setup before STCK falling	1.14	—	ns
34	SRXD hold after STCK falling	0	—	ns

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
2. There are 2 sets of I/O signals for the SSI module. They are from Port C primary function (pad 257 to pad 261) and Port B alternate function (pad 283 to pad 288). When SSI signals are configured as outputs, they can be viewed both at Port C primary function and Port B alternate function. When SSI signals are configured as input, the SSI module selects the input based on status of the FMCR register bits in the Clock Controller module (CRM). By default, the input are selected from Port C primary function.
3. bl = bit length; wl = word length.

Table 34. SSI (Port B Alternate Function) Timing Parameter Table

Ref No.	Parameter	1.8 +/- 0.10V		Unit
		Minimum	Maximum	
Internal Clock Operation[1] (Port B Alternate Function)[2]				
1	STCK/SRCK clock period[1]	95	—	ns
2	STCK high to STFS (bl) high[3]	1.7	4.8	ns
3	SRCK high to SRFS (bl) high[3]	-0.1	1.0	ns
4	STCK high to STFS (bl) low[3]	3.08	5.24	ns
5	SRCK high to SRFS (bl) low[3]	1.25	2.28	ns
6	STCK high to STFS (wl) high[3]	1.71	4.79	ns
7	SRCK high to SRFS (wl) high[3]	-0.1	1.0	ns
8	STCK high to STFS (wl) low[3]	3.08	5.24	ns
9	SRCK high to SRFS (wl) low[3]	1.25	2.28	ns

Table 34. SSI (Port B Alternate Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 +/- 0.10V		Unit
		Minimum	Maximum	
10	STCK high to STXD valid from high impedance	14.93	16.19	ns
11a	STCK high to STXD high	1.25	3.42	ns
11b	STCK high to STXD low	2.51	3.99	ns
12	STCK high to STXD high impedance	12.43	14.59	ns
13	SRXD setup time before SRCK low	20	—	ns
14	SRXD hold time after SRCK low	0	—	ns
External Clock Operation (Port B Alternate Function)[2]				
15	STCK/SRCK clock period[1]	92.8	—	ns
16	STCK/SRCK clock high period	27.1	—	ns
17	STCK/SRCK clock low period	61.1	—	ns
18	STCK high to STFS (bl) high[3]	—	92.8	ns
19	SRCK high to SRFS (bl) high[3]	—	92.8	ns
20	STCK high to STFS (bl) low[3]	—	92.8	ns
21	SRCK high to SRFS (bl) low[3]	—	92.8	ns
22	STCK high to STFS (wl) high[3]	—	92.8	ns
23	SRCK high to SRFS (wl) high[3]	—	92.8	ns
24	STCK high to STFS (wl) low[3]	—	92.8	ns
25	SRCK high to SRFS (wl) low[3]	—	92.8	ns
26	STCK high to STXD valid from high impedance	18.9	29.07	ns
27a	STCK high to STXD high	9.23	20.75	ns
27b	STCK high to STXD low	10.60	21.32	ns
28	STCK high to STXD high impedance	17.90	29.75	ns
29	SRXD setup time before SRCK low	1.14	—	ns
30	SRXD hole time after SRCK low	0	—	ns
Synchronous Internal Clock Operation (Port B Alternate Function)[2]				
31	SRXD setup before STCK falling	18.81	—	ns
32	SRXD hold after STCK falling	0	—	ns

Table 34. SSI (Port B Alternate Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 +/- 0.10V		Unit
		Minimum	Maximum	
Synchronous External Clock Operation (Port B Alternate Function)[2]				
33	SRXD setup before STCK falling	1.14	—	ns
34	SRXD hold after STCK falling	0	—	ns

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
2. There are 2 set of I/O signals for the SSI module. They are from Port C primary function (pad 257 to pad 261) and Port B alternate function (pad 283 to pad 288). When SSI signals are configured as outputs, they can be viewed both at Port C primary function and Port B alternate function. When SSI signals are configured as inputs, the SSI module selects the input based on FMCR register bits in the Clock Controller module (CRM). By default, the input are selected from Port C primary function.
3. bl = bit length; wl = word length

3.22 CMOS Sensor Interface

The CSI module consists of a control register to configure the interface timing, a control register for statistic data generation, a status register, interface logic, a 32×32 image data receive FIFO, and a 16×32 statistic data FIFO. Figure 66 shows the timing diagram when the CMOS Sensor output data in negative edge and CSI are programmed to received data in positive edge. Figure 31-6 shows the timing diagram when the CMOS Sensor output data in positive edge and CSI is programmed to received data in negative edge.

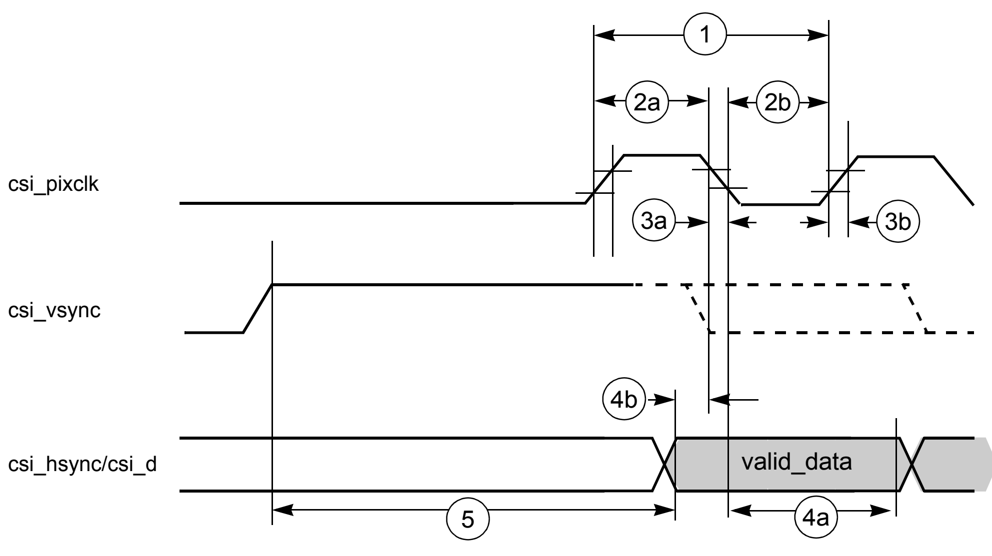


Figure 66. CSI Signal Timing Diagram

Table 35. CSI Signal Timing Parameter Table

Ref No.	Parameter	1.8 V		Unit
		Minimum	Maximum	
1	csi_pixclk frequency	0	48	MHz
2a	csi_pixclk high time[1]	10.42	—	ns
2b	csi_pixclk low time[1]	10.42	—	ns
3a	csi_pixclk fall time[1]	—	5	ns
3b	csi_pixclk rise time[1]	—	6.67	ns
4a	csi_hsync/csi_d hold time[1]	1	—	ns
4b	csi_hsync/csi_d setup time[1]	1	—	ns
5	csi_vsync to data valid time[1]	200	—	ns

1. $C_L \leq 30$ pF

4 Pin-Out and Package Information

Table 36. MC9328MX1 BGA Pin Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	VSS	SD_DAT3	SD_CLK	VSS	USBD_AFE	NVDD4	VSS	UART1_RTS	UART1_RXD	NVDD3	BT5	BT3	QVDD4	RVP	UIP	RM
B	A24	SD_DAT1	SD_CMD	SIM_TX	USBD_OE	USBD_VP	SSI_RXCLK	SSI_TXCLK	SPI1_SCLK	BT11	BT7	BT1	VSS	RVM	UIN	RP
C	A23	D31	SD_DAT0	SIM_PD	USBD_RCV	UART2_CTS	UART2_RXD	SSI_RXFS	UART1_TXD	BTRFGND	BT8	BTRFVDD	RVM1	AVDD2	VSS	R1B
D	A22	D30	D29	SIM_SVEN	USBD_SUSPND	USBD_VPO	USBD_VMO	SSI_RXDAT	SPI1_SPI_RDY	BT13	BT6	DAC_OM	RVP1	MIM	R1A	R2B
E	A20	A21	D28	D26	SD_DAT2	USBD_VM	UART2_RTS	SSI_TXDAT	SPI1_SS	BT12	BT4	DAC_OP	MIP	PY2	PX2	R2A
F	A18	D27	D25	A19	A16	SIM_RST	UART2_TXD	SSI_TXFS	SPI1_MISO	BT10	BT2	REV	PY1	PX1	LSCLK	SPL_SPR
G	A15	A17	D24	D23	D21	SIM_RX	SIM_CLK	UART1_CTS	SPI1_MOSI	BT9	CLS	CONTRAST	ACD/OE	LP/HSYNC	FLM/VSYNC	LD1
H	A13	D22	A14	D20	NVDD1	NVDD1	VSS	VSS	QVDD1	PS	LD0	LD2	LD4	LD5	LD9	LD3
J	A12	A11	D18	D19	NVDD1	NVDD1	VSS	NVDD1	VSS	VSS	LD6	LD7	LD8	LD11	QVDD3	VSS
K	A10	D16	A9	D17	NVDD1	VSS	VSS	NVDD1	NVDD2	NVDD2	LD10	LD12	LD13	LD14	TMR2OUT	LD15
L	A8	A7	D13	D15	D14	NVDD1	VSS	CAS	TCK	TIN	PWMO	CSI_MCLK	CSI_D0	CSI_D1	CSI_D2	CSI_D3
M	A5	D12	D11	A6	SDCLK	VSS	RW	MA10	RAS	RESET_IN	BIG_ENDIAN	CSI_D4	CSI_HSYNC	CSI_VSYNC	CSI_D6	CSI_D5
N	A4	EB1	D10	D7	A0	D4	PA17	D1	DQM1	RESET_SF	RESET_OUT	BOOT2	CSI_PIXCLK	CSI_D7	TMS	TDI
P	A3	D9	EB0	CS3	D6	ECB	D2	D3	DQM3	SDCKE1	BOOT3	BOOT0	TRST	I2C_SCL	I2C_SDA	XTAL32K
R	EB2	EB3	A1	CS4	D8	D5	LBA	BCLK	D0	DQM0	SDCKE0	POR	BOOT1	TDO	QVDD2	EXTAL32K
T	VSS	A2	OE	CS5	CS2	CS1	CS0	MA11	DQM2	SDWE	CLKO	AVDD1	TRISTATE	EXTAL16M	XTAL16M	VSS

4.1 MAPBGA Package Dimensions

Figure 68 illustrates the MAPBGA 14 mm × 14 mm × 1.30 mm package, which has 0.8 mm spacing between the pads. The device designator for the MAPBGA package is VF.

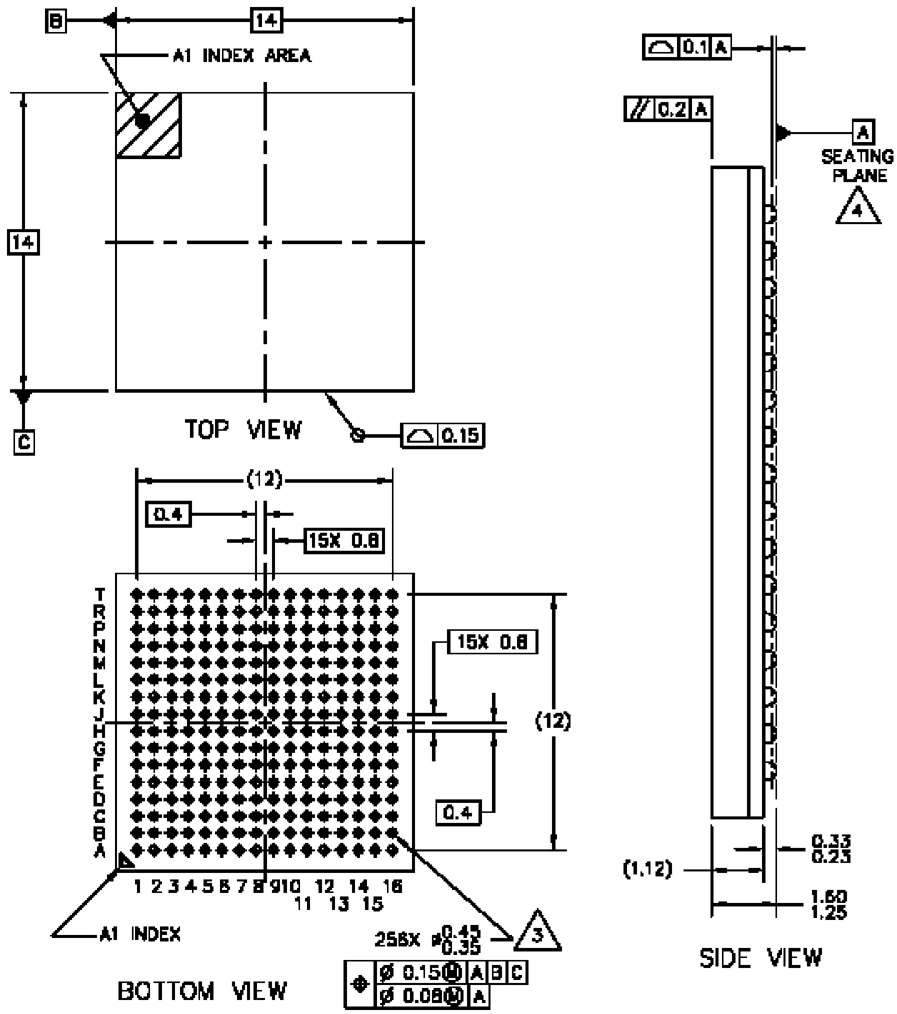


Figure 67. MC9328MX1 MAPBGA Mechanical Drawing (Part 1 of 2)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE IS DEFINED BY SPHERICAL CROWNS OF THE SOLDER BALLS.

Figure 68. MC9328MX1 MAPBGA Mechanical Drawing (Part 2 of 2)

4.2 PCB Finish Requirement

For a more reliable BGA assembly process, use HASL finish on the PCB. The EMNI AU finish is not recommended. When the EMNI AU finish is used on a PCB, brittle inter-metallic fractures occasionally occur at the BGA pad-to-PCB pad solder joint.

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