REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 03 and 04. Add case outline M. Add vendor CAGE 01295 as source of supply for device types 03 and 04. Update boilerplate. Editorial changes throughout.	94-11-01	M. A. Frye

REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51			
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
92-12-16

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS 256K X 4 VIDEO RAM, MONOLITHIC SILICON

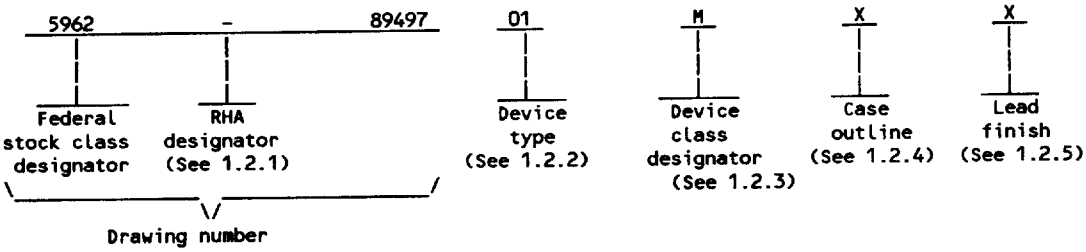
SIZE	CAGE CODE	5962-89497
A	67268	

SHEET 1 OF 51

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	DRAM Access time	SAM Access time
01		256K x 4, multiport video RAM	120 ns	35 ns
02		256K x 4, multiport video RAM	100 ns	30 ns
03		256K x 4, multiport video RAM	120 ns	35 ns
04		256K x 4, multiport video RAM	100 ns	30 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level (see 6.7 herein) as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
T	See figure 1	32	"J" lead chip carrier
U	CDFP4-F28	28	Flat pack
X	See figure 1	28	Dual-in-line
Y	See figure 1	28	"J" lead chip carrier
Z	See figure 1	28	Rectangular leadless chip carrier
M	See figure 1	28	Zig-zag in-line

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-BUL-103.

1.3 Absolute maximum ratings. 2/

Voltage range on any pin except DQ and SDQ	-1 V dc to 7 V dc
Voltage range on DQ and SDQ	-1 V dc to V_{CC}
Voltage range on V_{CC}	0 V dc to 7 V dc
Short circuit output current (per output)	50 mA
Power dissipation (P_D)	1 W
Storage temperature range	-65°C to 150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case U	See MIL-STD-1835
Cases X, Y, Z, and T	10°C/W 3/
Case M	5°C/W 3/
Junction temperature (T_J) 4/	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) 5/	+4.5 V dc to +5.5 V dc
Supply voltage (V_{SS})	0.0 V dc
High level input voltage range (V_{IH})	2.9 V dc to V_{CC}
Low level input voltage range (V_{IL}) 6/	-1.0 V dc to 0.6 V dc
System transition times, rise and fall (t_t)	3 ns to 50 ns
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	7/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ When the thermal resistance for this case is specified in MIL-STD-1835, that value shall supersede the value indicated herein.
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
5/ All voltage values in this drawing are with respect to V_{SS}.
6/ The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this drawing for voltage levels only.
7/ When a Qualified Manufacturer's List (QML) source exists, a value shall be provided.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the characterization of latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit will be provided when RHA product becomes available.

3.2.5 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the preparing or acquiring activity upon request.

3.2.6 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-I-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-I-38535 for classes Q and V. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

TABLE I. Electrical performance characteristics.

Test	Symbol/ alten. symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	$I_{OH} = -5$ mA	1,2,3	All	2.4		V
Low level output voltage 1/	V_{OL}	$I_{OL} = 4.2$ mA	1,2,3	All		0.4	V
Input leakage current	I_L	$V_I = 0$ to 5.8 V, $V_{CC} = 5$ V All other pins open	1,2,3	01,02		±1.0	µA
				03,04		±10	
Output leakage current 2/	I_O	$V_O = 0$ to V_{CC}, $V_{CC} = 5.5$ V	1,2,3	All		±10	µA
Operation current (standby) 3/	I_{CC1}	$t_{c(RW)}$ = minimum $t_{c(SC)}$ = minimum	1,2,3	01,03		90	mA
				02,04		100	
Operation current (active) 3/	I_{CC1A}		1,2,3	01,03		110	mA
				02,04		120	
Standby current (standby) 3/	I_{CC2}	All clocks = V_{CC} $t_{c(SC)}$ = minimum	1,2,3	All		15	mA
Standby current (active) 3/	I_{CC2A}		1,2,3	01,03		50	mA
				02,04		55	
RAS-only refresh current (standby) 3/	I_{CC3}	$t_{c(RW)}$ = minimum $t_{c(SC)}$ = minimum	1,2,3	01,03		90	mA
				02,04		100	
RAS-only refresh current (active) 3/	I_{CC3A}		1,2,3	01,03		120	mA
				02,04		125	
Page mode current (standby) 3/	I_{CC4}	$t_{c(P)}$ = minimum $t_{c(SC)}$ = minimum	1,2,3	01,03		60	mA
				02,04		65	
Page mode current (active) 3/	I_{CC4A}	$t_{c(P)}$ = minimum $t_{c(SC)}$ = minimum	1,2,3	01,03		90	mA
				02,04		100	
CAS-before-RAS current (standby) 3/	I_{CC5}	$t_{c(RW)}$ = minimum $t_{c(SC)}$ = minimum	1,2,3	01,03		80	mA
				02,04		90	
CAS-before-RAS current (active) 3/	I_{CC5A}		1,2,3	01,03		110	mA
				02,04		115	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol/ alten. symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Data transfer current (standby) 3/	I_{CC6}	$t_{c(RW)}$ = minimum $t_{c(SC)}$ = minimum	1,2,3	01,03		90	mA
				02,04		100	
Data transfer current (active) 3/	I_{CC6A}		1,2,3	01,03		125	mA
				02,04		130	
Input capacitance, address inputs	$C_{I(A)}$	See 4.4.1e f = 1 MHz, V_{IN} = 0 V	4	All		9	pF
Input capacitance, strobe inputs	$C_{I(RC)}$		4	All		10	pF
Input capacitance, write enable input	$C_{I(W)}$		4	All		10	pF
Input capacitance, serial clock input	$C_{I(SC)}$		4	All		10	pF
Input capacitance, special function	$C_{I(DSF)}$		4	All		10	pF
Input capacitance, serial enable	$C_{I(SE)}$		4	All		10	pF
Input capacitance, transfer register input	$C_{I(TRG)}$		4	All		10	pF
Output capacitance, SDQ and DQ	$C_{O(O)}$	See 4.4.1e f = 1 MHz, V_{IN} = 0 V	4	All		11	pF
Output capacitance, QSF	$C_{O(QSF)}$		4	All		17	pF
Functional tests		See 4.4.1c	7,8A,8B	All	L	H	V
Access time from CAS	$t_{a(C)}$ t_{CAL}	(See figures 4 and 5) $t_{d(RLCL)}$ = max, C_L = 80 pF	9,10,11	01,03		30	ns
				02,04		25	
Access time from column address	$t_{a(CA)}$ t_{AA}	(See figures 4 and 5) $t_{d(RLCL)}$ = max, C_L = 80 pF	9,10,11	01,03		60	ns
				02,04		50	
Access time from CAS high	$t_{a(CP)}$ t_{CPA}	(See figures 4 and 5) $t_{d(RLCL)}$ = min, C_L = 80 pF	9,10,11	01,03		65	ns
				02,04		55	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol/ alten. symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Access time from RAS high	$t_{a(R)}$ t_{RAC}	(See figures 4 and 5) $t_{d(RLCL)}$ = min, C_L = 80 pF	9,10,11	01,03		120	ns
				02,04		100	
Access time of Q from TRG low	$t_{a(G)}$ t_{OE}	(See figures 4 and 5) C_L = 80 pF	9,10,11	01,03		30	ns
				02,04		25	
Access time of SQ from SC high 4/	$t_{a(SQ)}$ t_{SAC}	(See figures 4 and 5) C_L = 30 pF	9,10,11	01,03		35	ns
				02,04		30	
Access time of SQ from SE low 4/	$t_{a(SE)}$ t_{SEA}	(See figures 4 and 5) C_L = 30 pF	9,10,11	01		30	ns
				03		25	
				02,04		20	
Access time of QSF from SC low	$t_{a(QSF)}$	(See figures 4 and 5) C_L = 30 pF	9,10,11	01,02		60	ns
Disable time, random output from CAS high	$t_{dis(CH)}$ t_{OFF}	(See figures 4 and 5) C_L = 80 pF	9,10,11	01	0	30	ns
				02-04	0	20	
Disable time, random output from TRG high 5/	$t_{dis(G)}$ t_{OD}	(See figures 4 and 5) C_L = 80 pF	9,10,11	01	0	30	ns
				02-04	0	20	
Disable time, serial output from SE high 5/	$t_{dis(SE)}$ t_{SEZ}	(See figures 4 and 5) C_L = 30 pF	9,10,11	All	0	20	ns
Cycle time, read 6/	$t_{c(rd)}$ t_{RC}	(See figures 4 and 5) C_L = 80 pF	9,10,11	01,03	220		ns
				02,04	190		
Cycle time, write	$t_{c(W)}$ t_{RC}		9,10,11	01,03	220		ns
				02,04	190		
Cycle time, read-modify write	$t_{c(rdW)}$ t_{RWC}		9,10,11	01	295		ns
				03	290		
				02,04	250		
Cycle time, page-mode read, write	$t_{c(P)}$ t_{PC}		9,10,11	01	70		ns
				02	60		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol/ alten. symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Cycle time, page-mode read-modify-write	$t_{c(RDWP)}$ t_{PRWC}	(See figures 4 and 5) C_L = 80 pF	9,10,11	01	130		ns
				02	110		
				03	125		
				04	105		
Cycle time, transfer read	$t_{c(TRD)}$ t_{RC}		9,10,11	01,03	220		ns
				02,04	190		
Cycle time, transfer write	$t_{c(TW)}$ t_{RC}		9,10,11	01,03	220		ns
				02,04	190		
Cycle time, serial clock 7/	$t_{c(SC)}$		9,10,11	01,03	35		ns
				02,04	30		
Pulse duration, CAS high	$t_{w(CH)}$ t_{CP}		9,10,11	01,03	30		ns
				02,04	20		
Pulse duration, CAS low 8/ 9/	$t_{w(CL)}$ t_{CAS}		9,10,11	01,03	30	75,000	ns
				02,04	25	75,000	
Pulse duration, RAS high	$t_{w(RH)}$ t_{RP}		9,10,11	01,03	90		ns
				02,04	80		
Pulse duration, RAS low 9/ 10/	$t_{w(RL)}$ t_{RAS}		9,10,11	01,03	120	75,000	ns
				02,04	100	75,000	
Pulse duration, W low	$t_{w(WL)}$ t_{WP}		9,10,11	All	25		ns
Pulse duration, TRG low	$t_{w(TRG)}$		9,10,11	01,03	30		ns
				02,04	25		
Pulse duration, SC high	$t_{w(SCH)}$ t_{SAS}		9,10,11	01,03	12		ns
				02,04	10		
Pulse duration, SC low	$t_{w(SCL)}$ t_{SP}		9,10,11	01,03	12		ns
				02,04	10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol/ alten. symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Setup time, column address	$t_{su(CA)}$ t_{ASC}	(See figures 4 and 5) C_L = 80 pF	9,10,11	All	0		ns
Setup time, DSF before $\overline{CAS}$ low	$t_{su(SFC)}$		9,10,11	All	0		ns
Setup time, row address	$t_{su(RA)}$ t_{ASR}		9,10,11	All	0		ns
Setup time, W before RAS low	$t_{su(WMR)}$ t_{WSR}		9,10,11	All	0		ns
Setup time, DQ before RAS low	$t_{su(DQR)}$ t_{TMS}		9,10,11	All	0		ns
Setup time, TRG before RAS low	$t_{su(TRG)}$ t_{TLS}		9,10,11	All	0		ns
Setup time, SE before $\overline{RAS}$ low 9/ 11/	$t_{su(SE)}$ t_{ESR}		9,10,11	All	0		ns
Setup time, DSF before $\overline{RAS}$ low	$t_{su(SFR)}$		9,10,11	All	0		ns
Setup time, data before CAS low 12/	$t_{su(DCL)}$ t_{DS}		9,10,11	All	0		ns
Setup time, data before W low 12/	$t_{su(DWL)}$ t_{DS}		9,10,11	All	0		ns
Setup time, read command	$t_{su(rd)}$ t_{RCS}		9,10,11	All	5		ns
Setup time, early write command before CAS low	$t_{su(WCL)}$ t_{WCS}		9,10,11	All	0		ns
Setup time, write before CAS high	$t_{su(WCH)}$ t_{CWL}		9,10,11	01,03	30		ns
				02,04	25		
Setup time, write before RAS high	$t_{su(WRH)}$ t_{RWL}		9,10,11	01,03	30		ns
				02,04	25		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol/ alten. symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Setup time, SD before SC high	$t_{su(SDS)}$ t_{SDS}	(See figures 4 and 5) C_L = 80 pF	9,10,11	01,02	3		ns
				03,04	0		
Hold time, column address after CAS low	$t_{h(CLCA)}$ t_{CAH}		9,10,11	01	25		ns
				02-04	20		
Hold time, DSF after $\overline{CAS}$ low	$t_{h(SFC)}$		9,10,11	All	20		ns
Hold time, row address address after RAS low	$t_{h(RA)}$ t_{RAH}		9,10,11	All	15		ns
Hold time, TRG after RAS low	$t_{h(TRG)}$ t_{TLH}		9,10,11	All	15		ns
Hold time, SE after RAS low 9/ 11/	$t_{h(SE)}$ t_{REH}		9,10,11	All	15		ns
Hold time, write mask transfer enable after RAS low	$t_{h(RWM)}$ t_{RWH}		9,10,11	All	15		ns
Hold time, DQ after $\overline{RAS}$ low (write mask operation)	$t_{h(RDQ)}$ t_{MH}		9,10,11	All	15		ns
Hold time, DSF after $\overline{RAS}$ low	$t_{h(SFR)}$		9,10,11	All	15		ns
Hold time, column address after RAS low 13/	$t_{h(RLCA)}$ t_{AR}		9,10,11	01-03	50		ns
				04	45		
Hold time, data after CAS low	$t_{h(CLD)}$ t_{DH}		9,10,11	01,03	25		ns
				02,04	20		
Hold time, data after $\overline{RAS}$ low 13/	$t_{h(RLD)}$ t_{DHR}		9,10,11	01-03	50		ns
				04	45		
Hold time, data after W low	$t_{h(WLD)}$ t_{DH}		9,10,11	01,03	25		ns
				02,04	20		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol/ alten. symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Hold time, TRG after W low (output enable controlled write) 9/	$t_{h(WLG)}$ t_{OEH}	(See figures 4 and 5) C_L = 80 pF	9,10,11	01,03	30		ns
				02,04	25		
Hold time, read after CAS 14/	$t_{h(CHrd)}$ t_{RCH}		9,10,11	All	0		ns
Hold time, read after RAS 14/	$t_{h(RHrd)}$ t_{RRH}		9,10,11	All	10		ns
Hold time, write after CAS low	$t_{h(CLW)}$ t_{WCH}		9,10,11	01,03	35		ns
				02,04	30		
Hold time, write after RAS low 13/	$t_{h(RLW)}$ t_{WCR}		9,10,11	01,03	55		ns
				02,04	50		
Hold time, SD after SC high	$t_{h(SDS)}$ t_{SDH}		9,10,11	01,02	20		ns
				03,04	5		
Hold time, SQ after SC high 9/	$t_{h(SHSQ)}$ t_{SOH}		9,10,11	All	5		ns
Delay time, RAS low to CAS high	$t_{d(RLCH)}$ t_{CSH}		9,10,11	01,03	120		ns
				02,04	100		
Delay time, CAS high to RAS low	$t_{d(CHRL)}$ t_{CRP}		9,10,11	01	10		ns
				02	5		
				03,04	0		
Delay time, CAS low to RAS high	$t_{d(CLRH)}$ t_{RSH}		9,10,11	01	35		ns
				02,03	30		
				04	25		
Delay time, CAS low to W low 15/ 16/	$t_{d(CLWL)}$ t_{CWD}		9,10,11	01	75		ns
				02	60		
				03	65		
				04	55		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol/ alten. symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low 17/	$t_{d(RLCL)}$ t_{RCD}	(See figures 4 and 5) C_L = 80 pF	9,10,11	01,03	25	90	ns
				02,04	25	75	
Delay time, column address to RAS high	$t_{d(CARH)}$ t_{RAL}		9,10,11	01,03	60		ns
				02,04	50		
Delay time, $\overline{RAS}$ low to $\overline{W}$ low 15/	$t_{d(RLWL)}$ t_{RWD}		9,10,11	01	160		ns
				03	155		
				02,04	130		
Delay time, column address to $\overline{W}$ low 9/ 15/	$t_{d(CAWL)}$ t_{AWD}		9,10,11	01,03	100		ns
				02,04	85		
Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high 9/ 18/	$t_{d(RLCH)R}$ t_{CHR}		9,10,11	01,02	30		ns
				03,04	25		
Delay time, $\overline{CAS}$ low to RAS low 18/	$t_{d(CLRL)R}$ t_{CSR}		9,10,11	All	10		ns
Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low 9/ 18/	$t_{d(RHCL)R}$ t_{RPC}		9,10,11	All	10		ns
Delay time, $\overline{CAS}$ low to TRG high	$t_{d(CLGH)}$ t_{CTH}		9,10,11	01,03	30		ns
				02,04	25		
Delay time, $\overline{TRG}$ high before data applied at DQ 15/	$t_{d(GHD)}$ t_{OD}		9,10,11	01,03	30		ns
				02,04	25		
Delay time, $\overline{RAS}$ low to TRG high 9/	$t_{d(RLTH)}$ t_{RTH}		9,10,11	01,03	95		ns
				02,04	90		
Delay time, RAS low to first SC high after TRG high 9/ 19/	$t_{d(RLSH)}$ t_{RSD}		9,10,11	01,03	140		ns
				02,04	130		
Delay time, CAS low to first SC high after TRG high 9/ 19/	$t_{d(CLSH)}$ t_{CSD}		9,10,11	01,03	45		ns
				02,04	40		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol/ alten. symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Delay time, SC high to $\overline{TRG}$ high 9/ 19/ 20/	$t_{d(SCTR)}$ t_{TTSC}	(See figures 4 and 5) C_L = 80 pF	9,10,11	01,03	20		ns
				02,04	15		
Delay time, $\overline{TRG}$ high to RAS high 19/	$t_{d(THRH)}$ t_{TRL}		9,10,11	All	-10		ns
Delay time, SC high to $\overline{RAS}$ low 9/ 11/ 21/	$t_{d(SCRL)}$ t_{SRS}		9,10,11	01,03	20		ns
				02	15		
				04	10		
Delay time, SC high to $\overline{SE}$ high in serial input mode 9/ 22/	$t_{d(SCSE)}$ t_{SWH}		9,10,11	All	20		ns
Delay time, $\overline{RAS}$ high to SC high 9/ 11/	$t_{d(RHSC)}$ t_{SRD}		9,10,11	01,03	30		ns
				02,04	25		
Delay time, $\overline{TRG}$ high to RAS low 23/	$t_{d(THRL)}$		9,10,11	All	$t_{w(RH)}$		ns
Delay time, $\overline{TRG}$ high to SC high 23/	$t_{d(THSC)}$ t_{TSO}		9,10,11	01,03	40		ns
				02,04	35		
Delay time, $\overline{SE}$ low to SC high 9/ 22/	$t_{d(SESC)}$ t_{SWS}		9,10,11	01,03	15		ns
				02,04	10		
Delay time, $\overline{RAS}$ high to last (most significant) rising edge of SC before boundary switch (split read transfer cycles)	$t_{d(RHMS)}$		9,10,11	01	30		ns
				02	25		
				03	20		
				04	15		
Delay time, first (TAP) rising edge of SC after boundary switch to $\overline{RAS}$ low (split read transfer cycles)	$t_{d(TPRL)}$		9,10,11	01	25		ns
				02	20		
Refresh time interval, memory	$t_{rf(MA)}$ t_{REF}		9,10,11	All		8	ms

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

1/ These devices exhibit simultaneous switching noise. This phenomenon exhibits itself upon the DQ pins when the SDQ pins are switched and upon the SDQ pins when DQ pins are switched. This may cause the V_{OL} and V_{OH} to exceed the limit for a short period of time, depending upon output loading and temperature. Care should be taken to provide proper termination, decoupling, and layout of the device to minimize simultaneous switching effects.
2/ SE is disabled for SDQ output leakage tests.
3/ I_{CC} (standby) versus I_{CCA} (active) denotes the following:
I_{CC} (standby): SAM port is inactive (standby) and the DRAM port is active (except for I_{CC2}).
I_{CCA} (active): SAM port is active and the DRAM port is active (except for I_{CC2A}).
I_{CC} is measured with no load on DQ or SDQ pins.
4/ SAM output timing may be measured with a load equivalent to 2 TTL gates plus 30 pF. Output reference levels: V_{OH} = 2.0 V, V_{OL} = 0.8 V.
5/ Disable times are specified when the output is no longer driven.
6/ All cycle times assume t_t = 5 ns.
7/ When the odd tap is used (tap address can be 0-511, and odd taps are 1,3,5, etc.), the cycle time for SC in serial data out cycle needs to be 70 ns minimum.
8/ In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional CAS low time, $t_{w(CL)}$.
9/ If not tested, shall be guaranteed to the limits in table IA.
10/ In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional RAS low time, $t_{w(RL)}$.
11/ Register to memory (write) transfer cycles only.
12/ These parameters are referenced to CAS leading edge in early-write cycles and $\overline{ME}/\overline{NE}$ leading edge in late write or read-write cycles.
13/ The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ minimum as a reference.
14/ Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
15/ Read-modify-write operation only.
16/ TRG must disable the output buffers prior to applying data to the DQ pins.
17/ Maximum value specified only to guarantee RAS access time.
18/ CAS-before-RAS refresh operation only.
19/ Memory to register (read) transfer cycles only.
20/ In a transfer read cycle, the state of SC when $\overline{TRG}$ rises is a don't care condition. However, to guarantee proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{TRG}$ goes high.
21/ In a transfer write cycle, the state of SC when $\overline{RAS}$ falls is a don't care condition. However, to guarantee proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{RAS}$ goes low.
22/ Serial data-in cycles only.
23/ Memory to register (read) and register to memory (write) transfer cycles only.

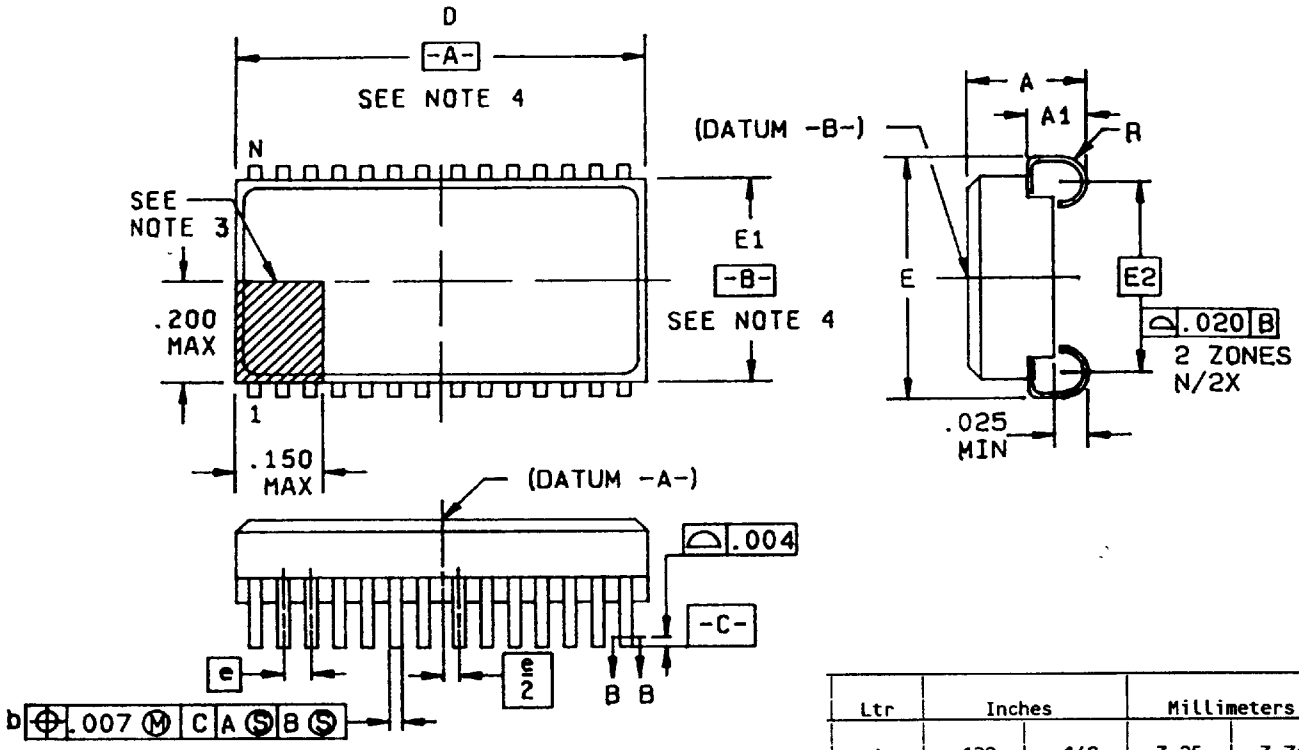
TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

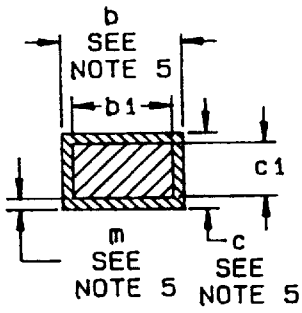
Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B Δ	1,2,3,7, 8A,8B,9, 10,11 Δ
9	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

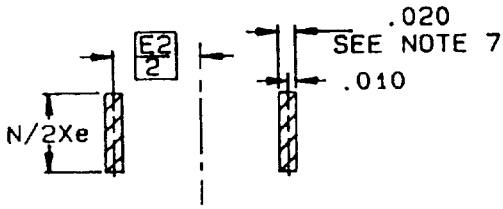
1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1d.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

Case T

"J" lead chip carrier





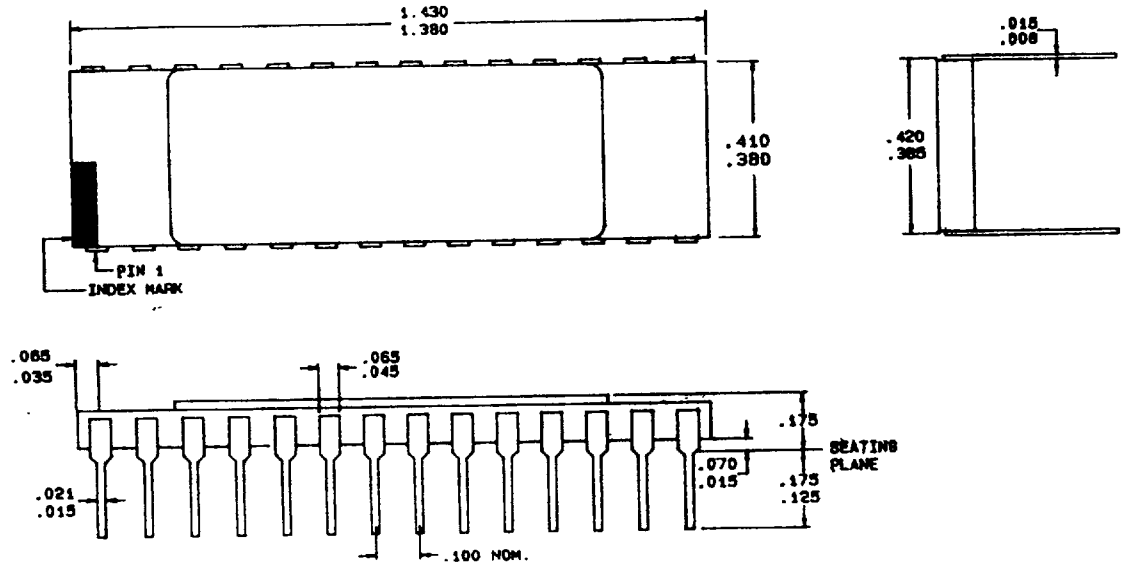


Inches	mm
.004	0.10
.007	0.18
.010	0.25
.020	0 51
025	0.64
.150	3.81
.200	5 08

Ltr	Inches		Millimeters	
A	.128	.148	3.25	3.76
A1	.055	.075	1.40	1.91
b	.015	.022	0.38	0.56
b1	.015	.019	0.38	0.48
c	.004	.009	0.10	0.23
c1	.004	.006	0.10	0.15
D	.710	.730	18.03	18.54
e	.050 BSC		1.27	1.27
E	.435	.445	11.05	11.30
E1	.405	.415	10.29	10.54
E2	.370 BSC		9.40	9.40
m	.0002	.0015	0.005	0.038
N	28			
R	.030	.040	0.76	1.01

FIGURE 1. Case outlines.

Case X



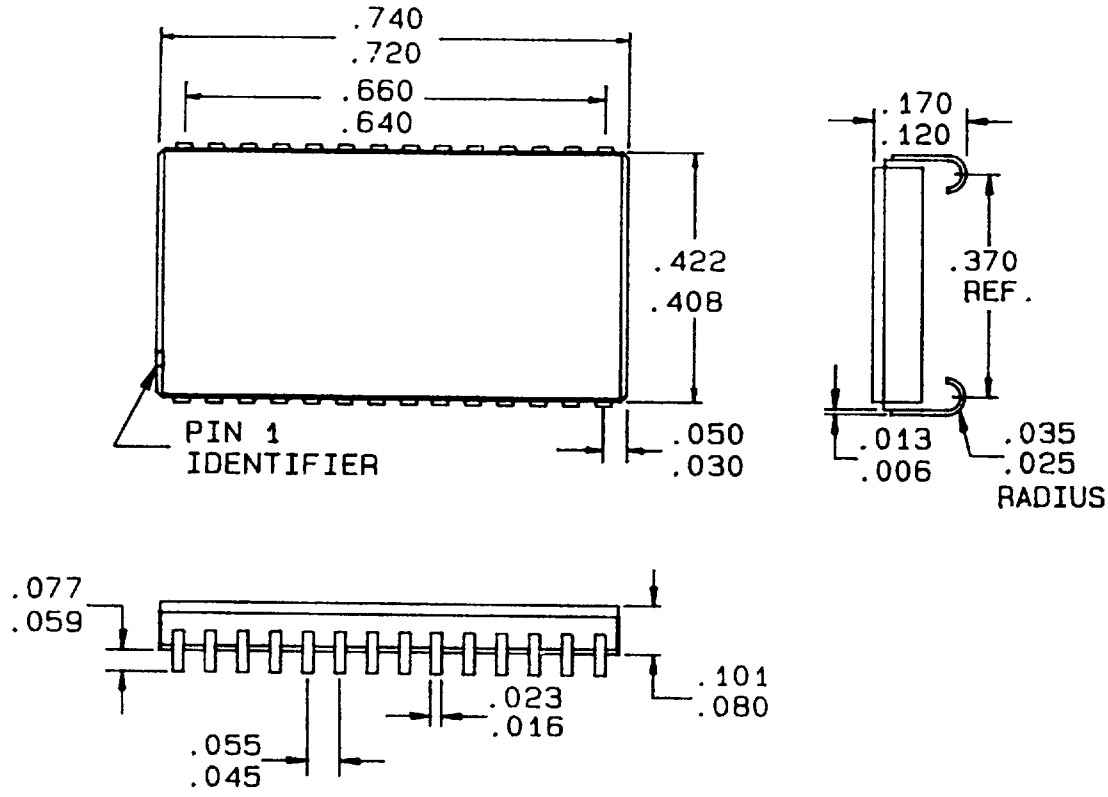
Inches	mm	Inches	mm
.008	0.20	.125	3.18
.015	0.38	.175	4.45
.021	0.53	.380	9.65
.035	0.89	.385	9.79
.045	1.14	.410	10.41
.065	1.65	.420	10.67
.070	1.78	1.380	35.05
.100	2.54	1.430	36.32

NOTE: Configurations A and C as specified in MIL-STD-1835 may be used.

FIGURE 1. Case outlines - continued.

Case Y

28-pin "J" lead chip carrier

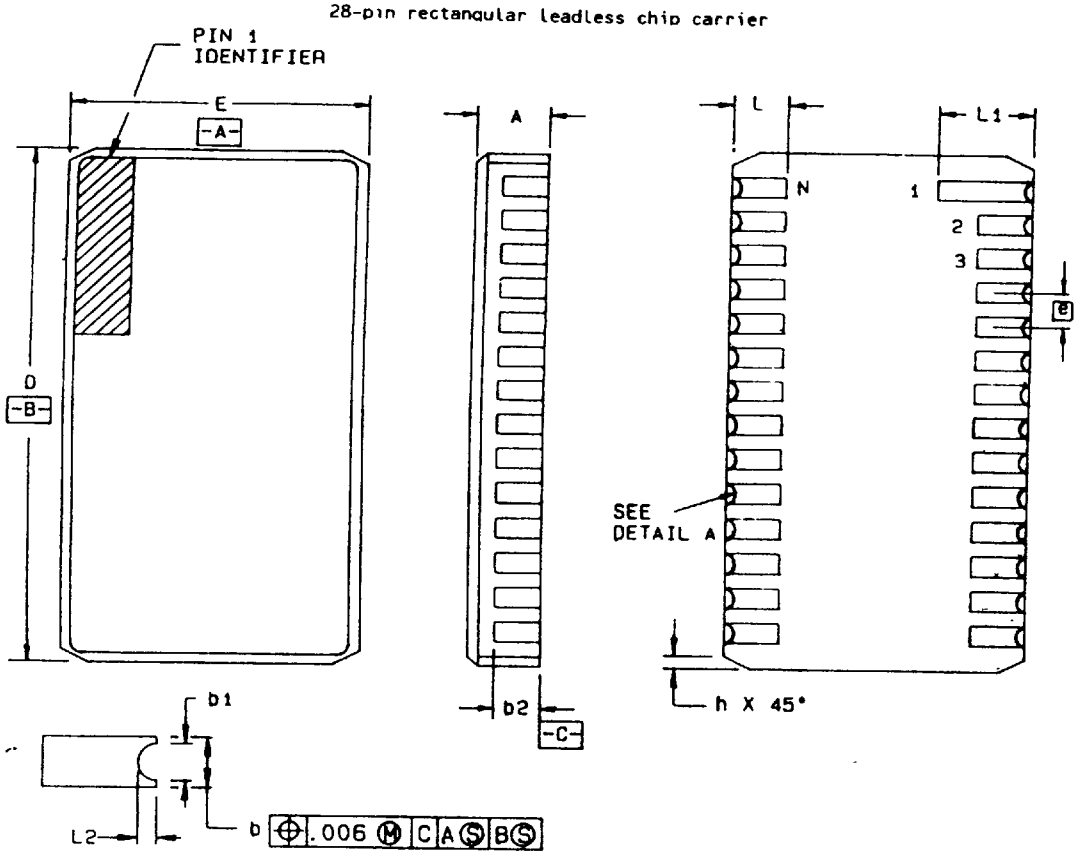


Inches	mm	Inches	mm
.006	0.152	.077	1.778
.013	0.330	.080	2.032
.016	0.406	.101	2.565
.023	0.584	.139	3.513
.025	0.635	.170	4.318
.030	0.762	.370	9.398
.035	0.889	.408	10.636
.045	1.143	.422	10.719
.050	1.270	.640	16.256
.055	1.397	.660	16.764
.059	1.498	.720	18.288
		.740	18.796

FIGURE 1. Case outlines - continued.

Case Z

28-pin rectangular leadless chip carrier

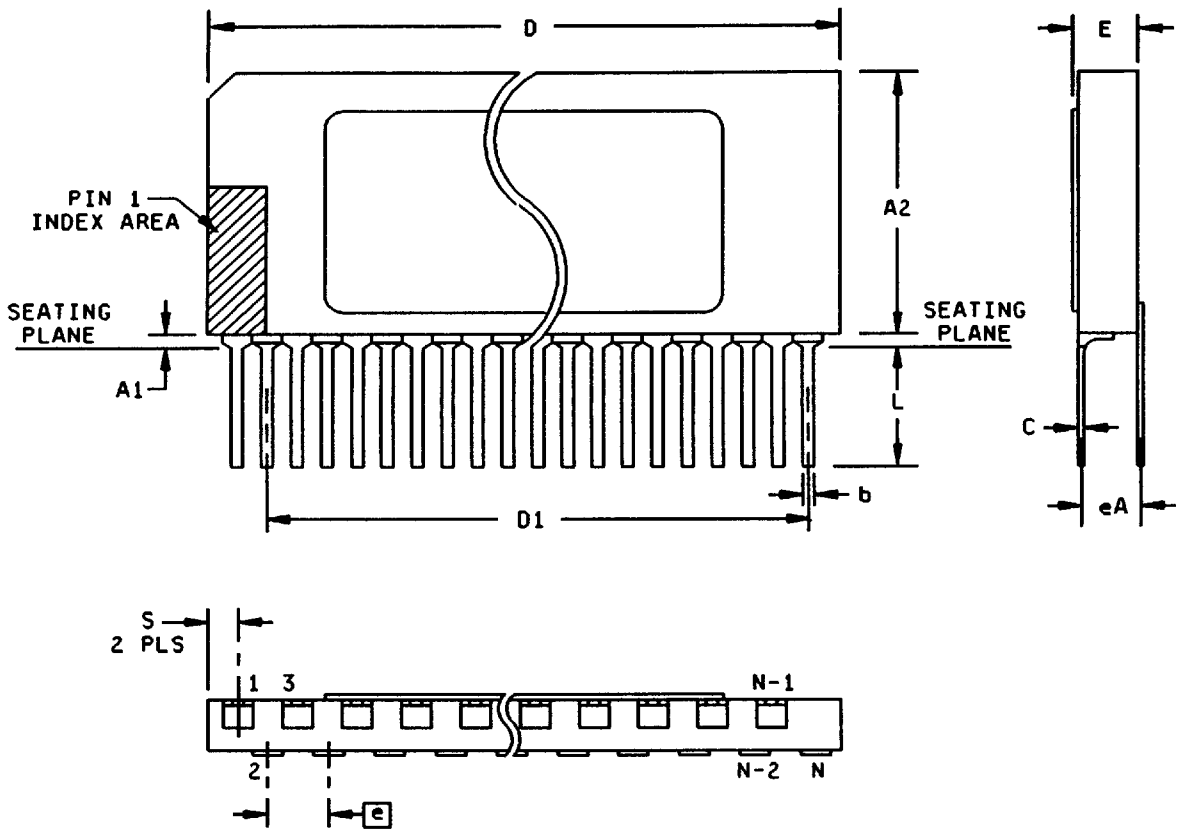


Ltr	Dimensions				Ltr	Dimensions			
	Inches		Millimeters			Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	.080	.100	2.03	2.54	e	.050 BSC		1.27	
b	.022	.028	0.56	0.71	h	.012 REF		0.30	
b1	.006	.022	0.15	0.56	L	.070	.080	1.78	2.03
b2	.040		1.02		L1	.090	.110	2.29	2.79
D	.700	.740	17.78	18.80	L2	.003	.015	0.08	0.38
E	.392	.408	9.96	10.36	N	28 terminals			

NOTES:
1. All dimensions are in inches. All dimensioning and tolerancing conform to ANSI Y14.5M-1982.
2. Unless otherwise specified, a minimum clearance of .015 inch (0.38 mm) shall be maintained between all metallized features.
3. Index area: Details of pin 1 identifier are optional, but must be located within the zone indicated.
4. The cover shall not extend beyond the edges of the body.
5. Dimensions b1 and c1 apply to the base metal only. Dimension m applies to the plating/coating thickness.
6. N indicates the number of terminals.
7. A gauge makers tolerance is applied.

FIGURE 1. Case outlines - continued.

Case M



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A1	0.38	1.27	.015	.050
A2	11.18	11.81	.440	.465
b	0.41	0.58	.016	.023
c	0.20	0.39	.008	.015
D	36.45	37.21	1.435	1.465
D1	32.77	33.27	1.290	1.310
e	2.54 BSC		.100 BSC	
eA	2.16	2.92	.085	.115
E	2.54	3.30	.100	.130
L	3.18	5.08	.125	.200
S	0.88	1.65	.035	.065

Note: The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outlines - continued.

Device types	01, 02, 03, 04	
Case outlines	T, U, X, Y, Z	M
Terminal number	Terminal symbol	
1	SC	DSF
2	SDQ_0	DQ_2
3	SDQ_1	DQ_3
4	$\overline{TRG}$	$\overline{SE}$
5	DQ_0	SDQ_2
6	DQ_1	SDQ_3
7	W	V_{SS}
8	GND	SC
9	$\overline{RAS}$	SDQ_0
10	A_8	SDQ_1
11	A_6	TRG
12	A_5	DQ_0
13	A_4	DQ_1
14	V_{CC}	W
15	A_7	NC/GND
16	A_3	RAS
17	A_2	A_8
18	A_1	A_6
19	A_0	A_5
20	QSF	A_4
21	CAS	V_{CC}
22	DSF	A_7
23	DQ_2	A_3
24	DQ_3	A_2
25	SE	A_1
26	SDQ_2	A_0
27	SDQ_3	QSF
28	V_{SS}	CAS

FIGURE 2. Terminal connections.

Type	RAS fall					CAS fall	Address		DQ0 - DQ3		Function
	CAS	TRG	* W	DSF	SE	DSF	RAS	CAS	RAS	** CAS W	
R	L	X	X	X	X	X	X	X	X	X	CAS-before-RAS refresh
T	H	L	L	X	L	X	Row Addr	Tap Point	X	X	Register to memory transfer (Transfer write)
T	H	L	L	H	X	X	Row Addr	Tap Point	X	X	Alternate transfer write (Independent of SE)
T	H	L	L	L	H	X	Refresh Addr	Tap Point	X	X	Serial write-mode enable (Pseudo-transfer write)
T	H	L	H	L	X	X	Row Addr	Tap Point	X	X	Memory to register transfer (Transfer read)
T	H	L	H	H	X	X	Row Addr	Tap Point	X	X	Split register transfer Read (must reload tap)
R	H	H	L	L	X	L	Row Addr	Col Addr	Write Mask	Valid Data	Load and use write mask Write data to dram
R	H	H	L	L	X	H	Row Addr	Col A2-A8	Write Mask	Addr Mask	Load and use write mask Block write to dram
R	H	H	L	H	X	L	Row Addr	Col Addr	X	Valid Data	Persistent write-per-bit Write data to dram
R	H	H	L	H	X	H	Row Addr	Col A2-A8	X	Addr Mask	Persistent write-per-bit Block write to dram
R	H	H	H	L	X	L	Row Addr	Col Addr	X	Valid Data	Normal dram read/write (Nonmasked)
R	H	H	H	L	X	H	Row Addr	Col A2-A8	X	Addr Mask	Block write to dram (Nonmasked)
R	H	H	H	H	X	L	Refresh Addr	X	X	Write Mask	Load write mask
R	H	H	H	H	X	H	Refresh Addr	X	X	Color Mask	Load color register

R = Random access operation
T = Transfer operation
X = Don't care

NOTES:
* Addr mask = 1 write to address location enabled.
Write mask = 1 write to I/O enabled.
In persistent write-per-bit function, $\overline{W}$ must be high during the refresh cycles.
** DQ0-3 are latched on the later of W or CAS falling edge.

FIGURE 3. Truth tables.

Transfer operation logic ***

$\overline{TRG}$	$\overline{W}$	$\overline{SE}$	DSF	Mode
L	L	L	X	Register to memory (write) transfer (serial write mode enable)
L	L	X	H	Alternate register to memory transfer
L	L	H	L	Serial write mode enable (pseudo write transfer)
L	H	X	L	Memory to register (read) transfer
L	H	X	H	Split register read transfer

H = High voltage level
L = Low voltage level
X = Don't care
R = Random access operation
T = Transfer operation

Serial operation logic

Last transfer cycle	$\overline{SE}$	SDQ
Alternate register to memory	H	Input disabled
Serial write mode enable ****	L	Input enable
Serial write mode enable ****	H	Input disable
Memory to register	L	Output enabled
Memory to register	H	HI-Z

H = High voltage level
L = Low voltage level
X = Don't care
R = Random access operation
T = Transfer operation

NOTES:
*** Above logic states are assumed valid on the falling edge of $\overline{RAS}$.
**** Pseudo transfer write.

FIGURE 3. Truth tables - continued.

Read cycle timing

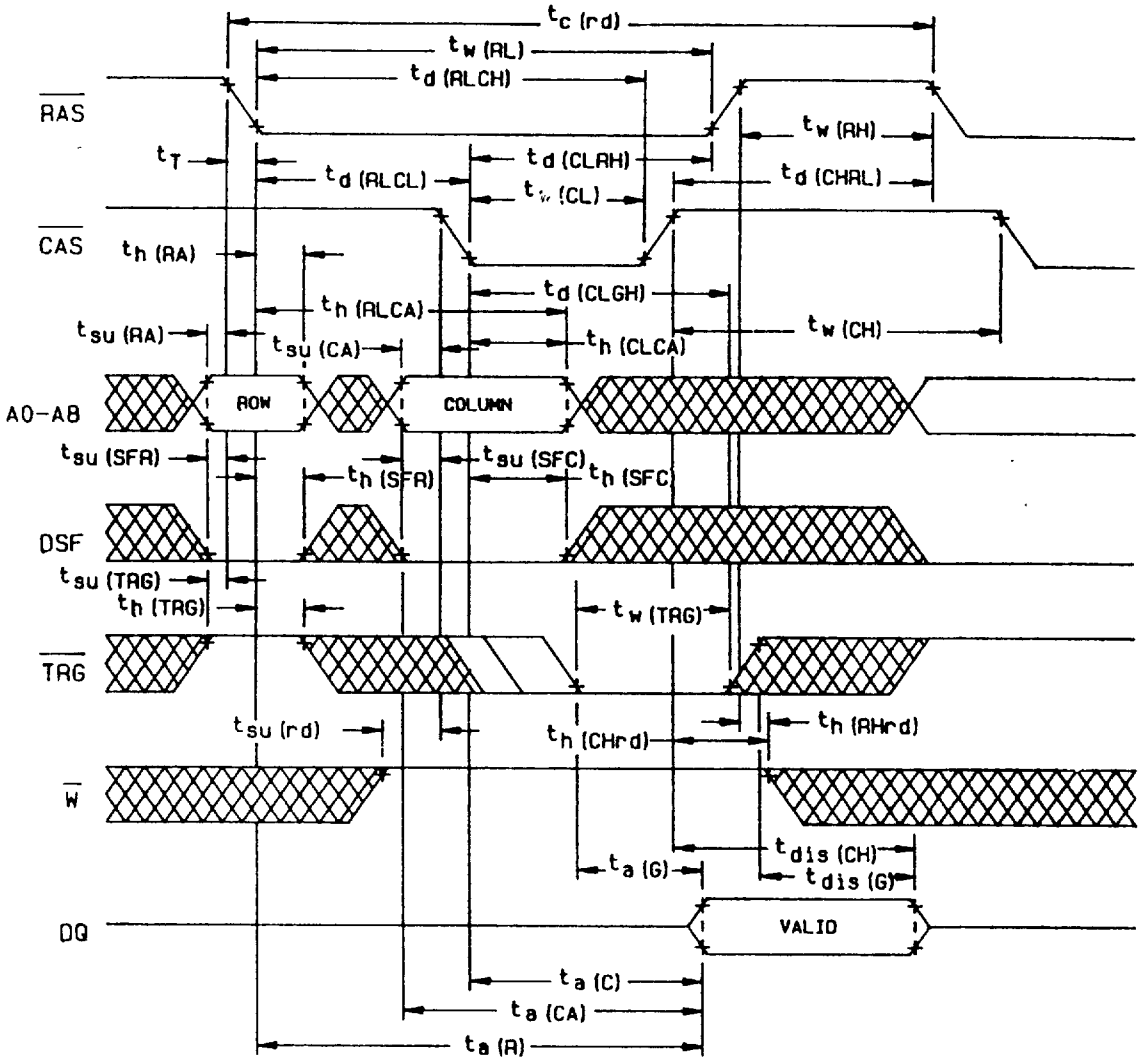
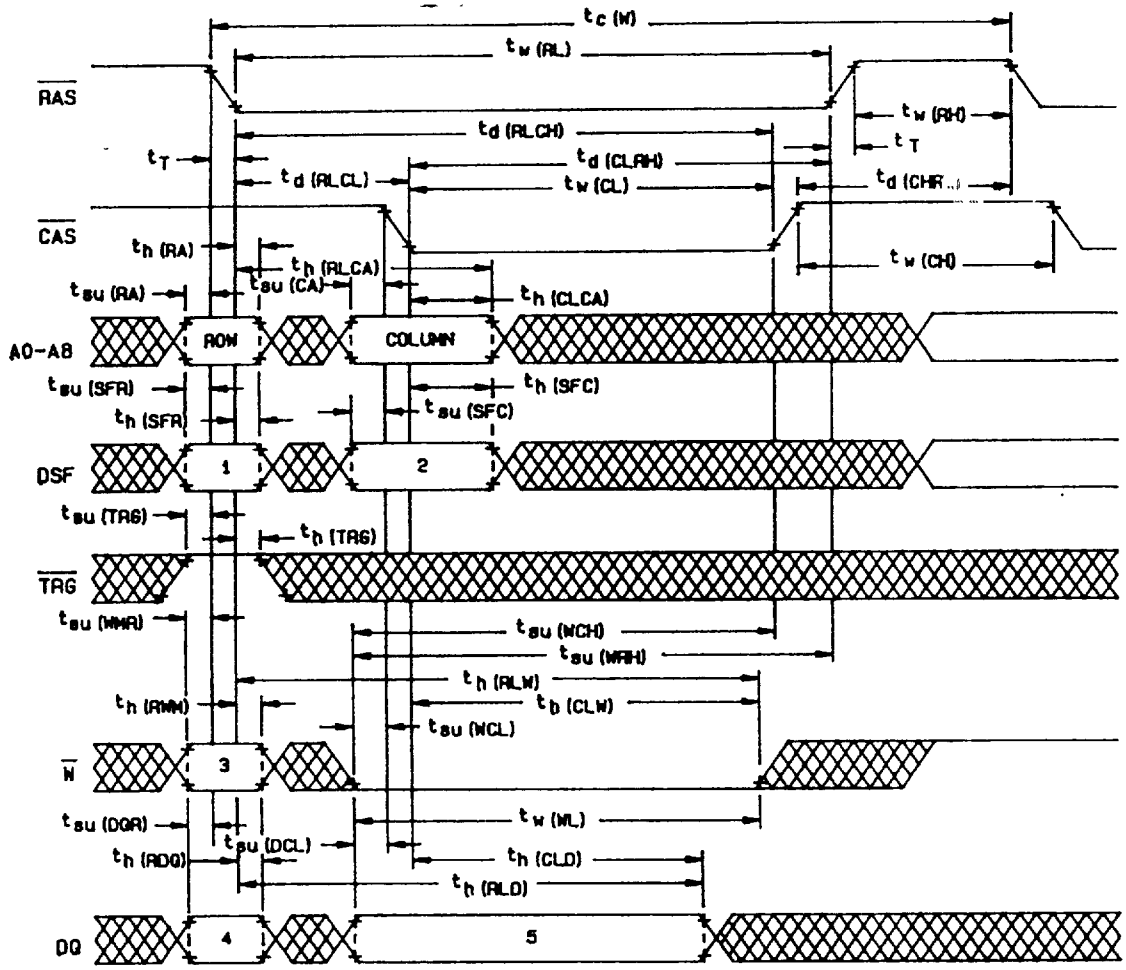


FIGURE 4. Timing waveform diagrams.

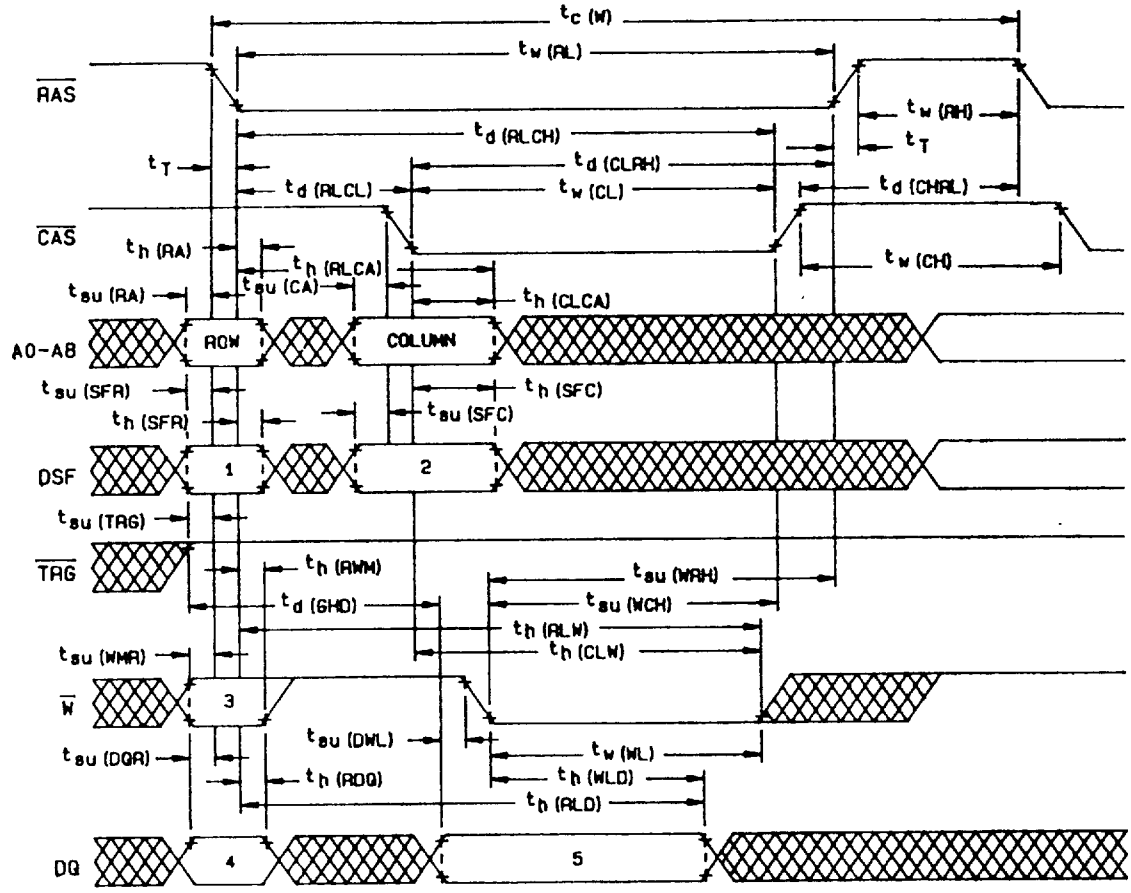
Early write cycle timing



NOTE: See "write cycle state" table (of figure 4) for the logic state of "1", "2", "3", "4", and "5".

FIGURE 4. Timing waveform diagrams - Continued.

Delayed write cycle timing



NOTE: See "write cycle state" table (of figure 4) for the logic state of "1", "2", "3", "4", and "5".

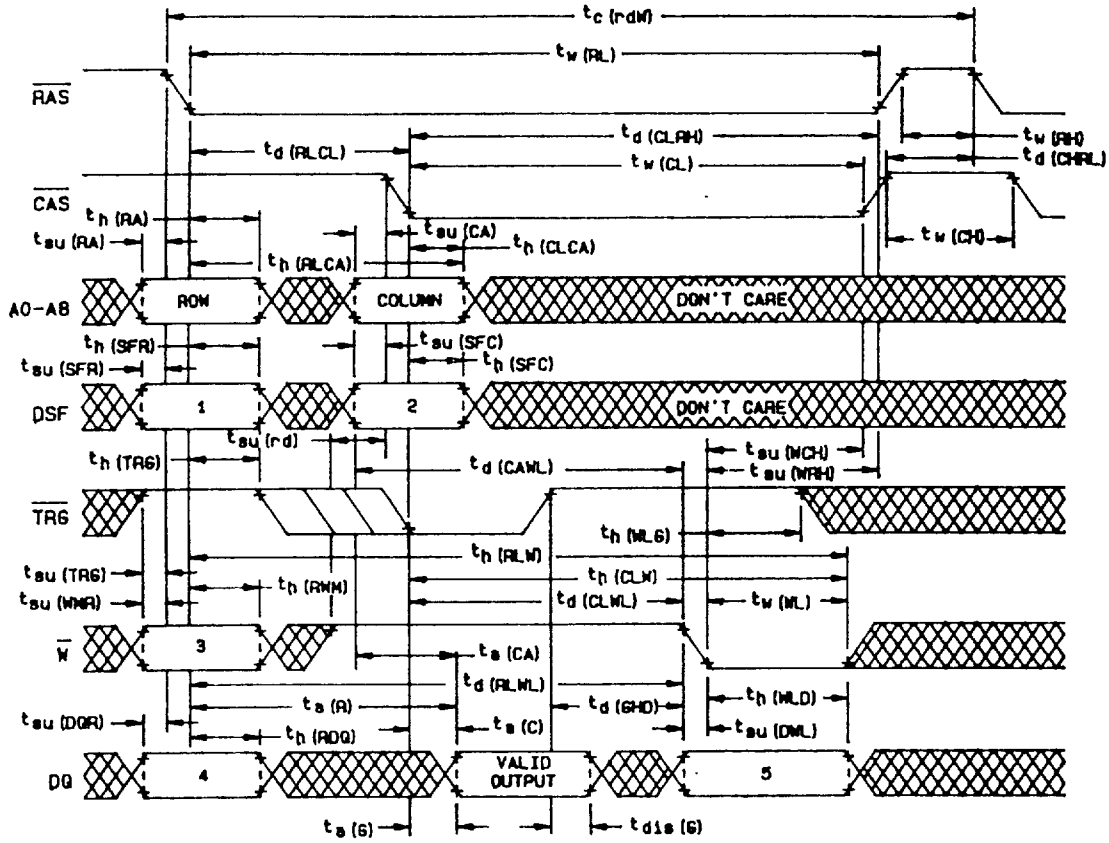
FIGURE 4. Timing waveform diagrams - Continued.

Write cycle state table

Cycle	State				
	1	2	3	4	5
Write mask load/use write DQs to I/Os	L	L	L	Write mask	Valid date
Write mask load/use block write	L	H	L	Write mask	ADDR mask
Use previous write mask, write DQs to I/Os	H	L	L	Don't care	Valid data
Use previous write mask, block write	H	H	L	Don't care	ADDR mask
Load write mask on later of $\overline{W}$ fall and $\overline{CAS}$ fall	H	L	H	Don't care	Write mask
Load color register on later of $\overline{W}$ fall and $\overline{CAS}$ fall	H	H	H	Don't care	Color data
Write mask disabled, block write to all I/Os	L	H	H	Don't care	ADDR mask
Normal early or late write operation	L	L	H	Don't care	Valid data

FIGURE 4. Timing waveform diagrams - Continued.

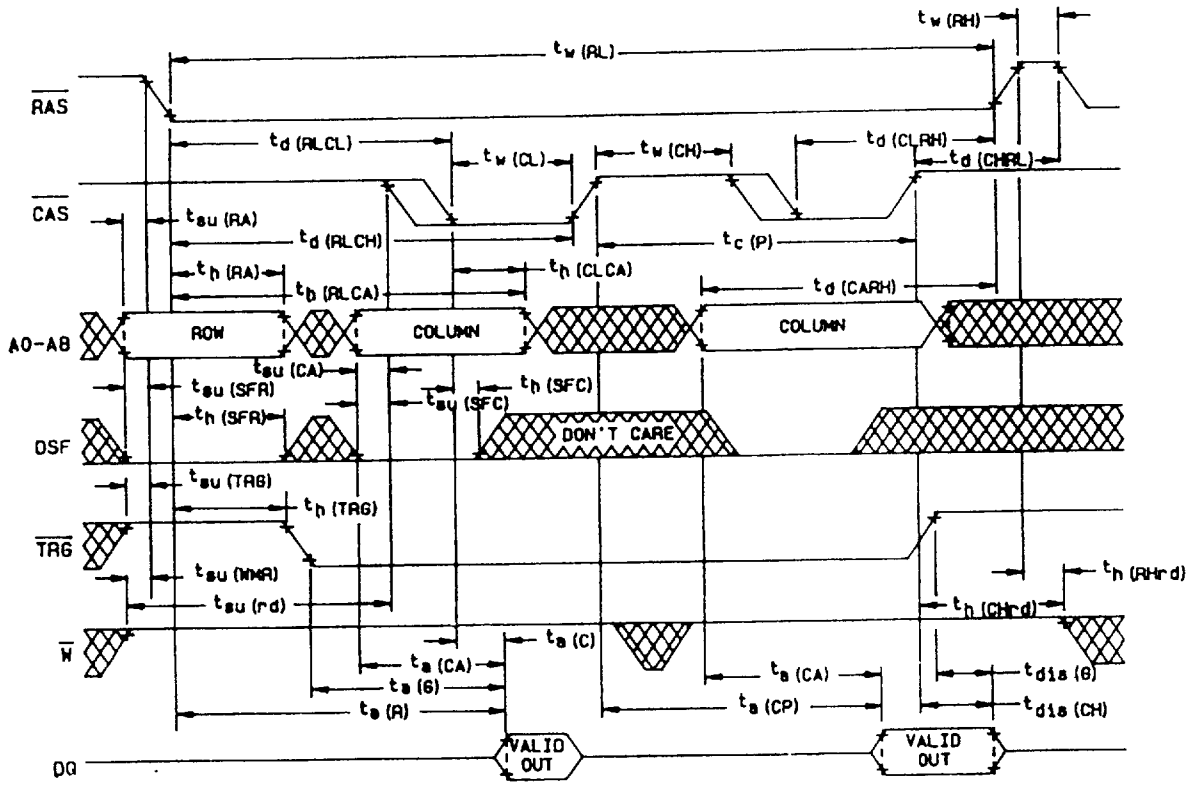
Read-write/read-modify-write cycle timing



NOTES:
1. See "write cycle state" table (of figure 4) for the logic state of "1", "2", "3", "4", and "5".
2. Same logic as delayed write cycle.

FIGURE 4. Timing waveform diagrams - Continued.

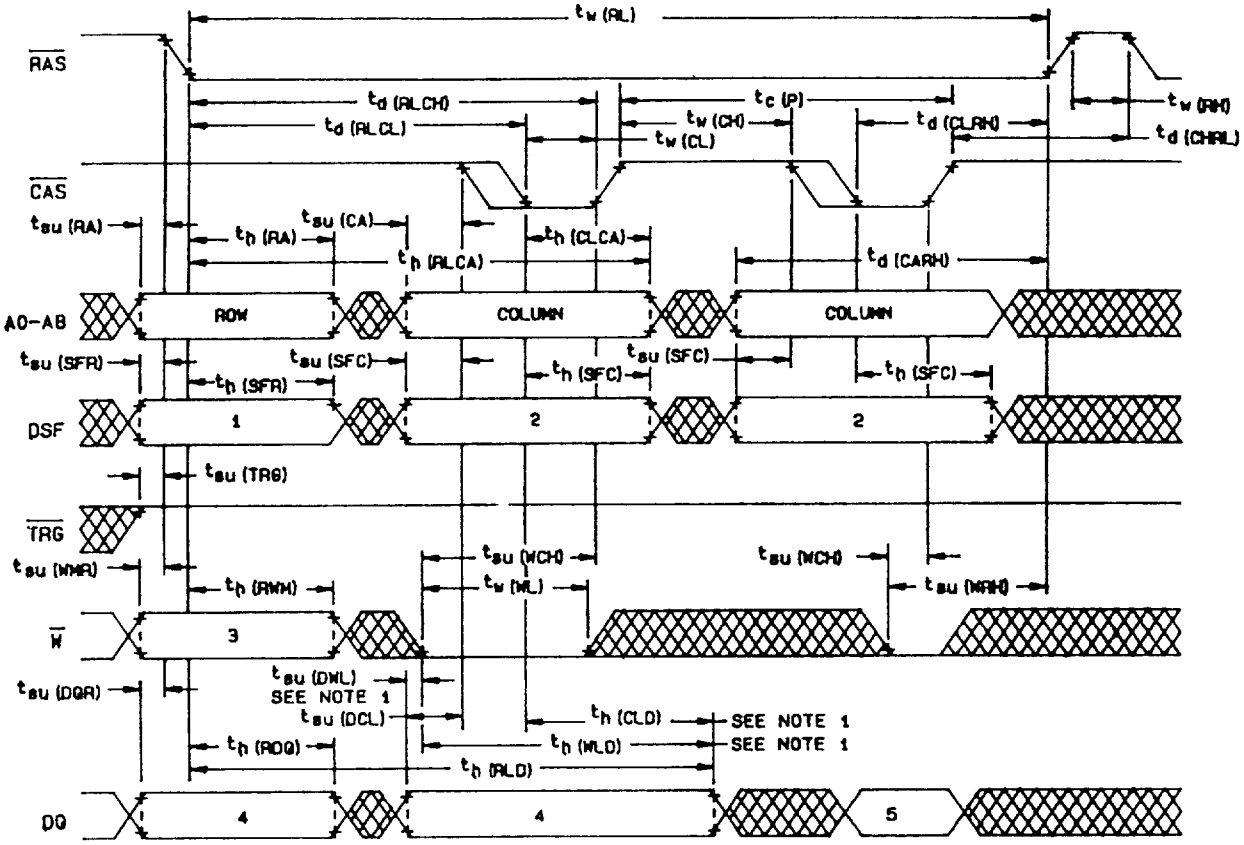
Enhanced page-mode read cycle timing



NOTES:
1. Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
2. Output may go from high impedance state to an invalid state prior to the specified access time.
3. A write cycle or a read-modify-write cycle can be mixed with read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edges of RAS and CAS to select the desired write mode (normal, block write, etc.).

FIGURE 4. Timing waveform diagrams - Continued.

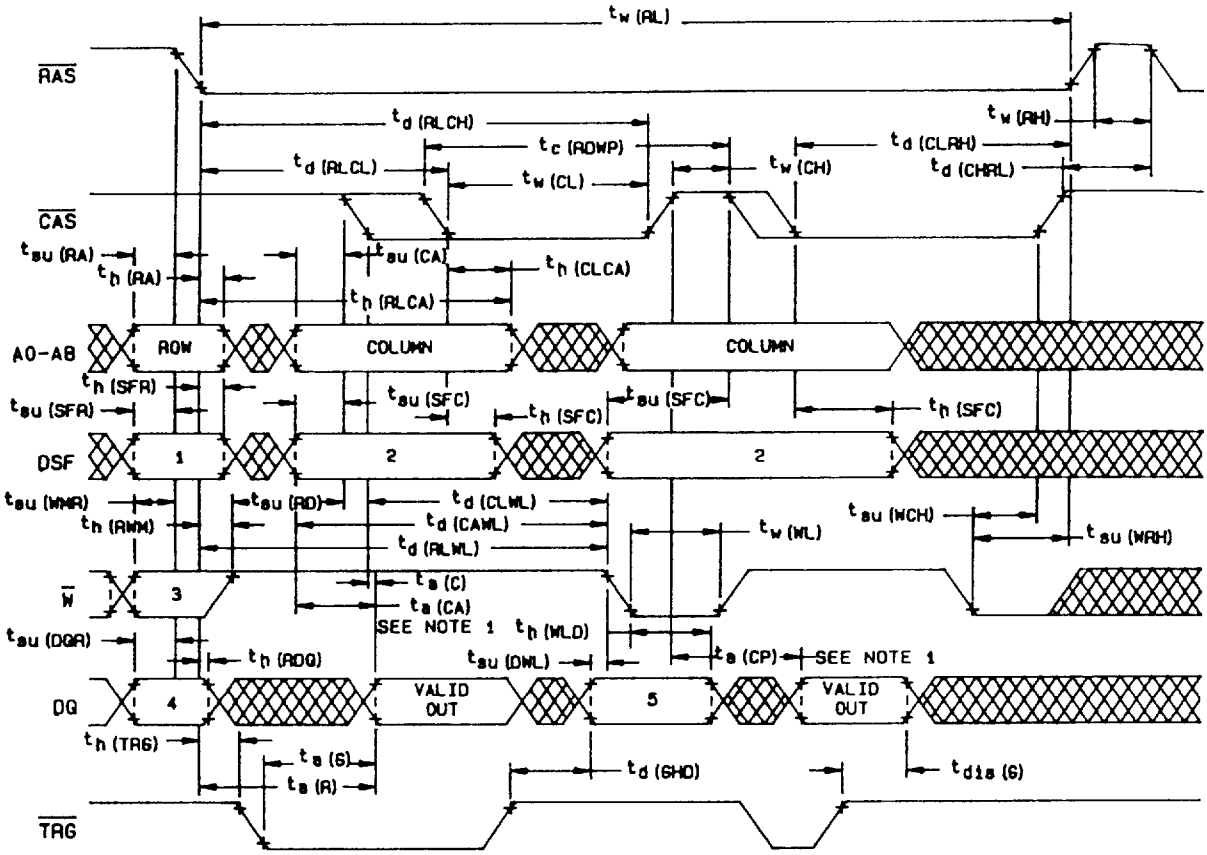
Enhanced page-mode write cycle timing



NOTES:
1. Referenced to CAS or W, whichever occurs last.
2. See "write cycle state" table (of figure 4) for the logic state of "1", "2", "3", "4", and "5".
3. A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. TRG must remain high throughout the entire page-mode operation if the late write feature is used, to guarantee page-mode cycle time. If the early write cycle timing is used, the state of TRG is don't care after the minimum period $t_{h(TRG)}$ from the falling edge of RAS.

FIGURE 4. Timing waveform diagrams - Continued.

Enhanced page-mode read-modify-write cycle timing



NOTES:
1. Output may go from the high impedance state to an invalid data state prior to the specified access time.
2. See "write cycle state" table (of figure 4) for the logic state of "1", "2", "3", "4", and "5".
3. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

FIGURE 4. Timing waveform diagrams - Continued.

$\overline{RAS}$-only refresh timing

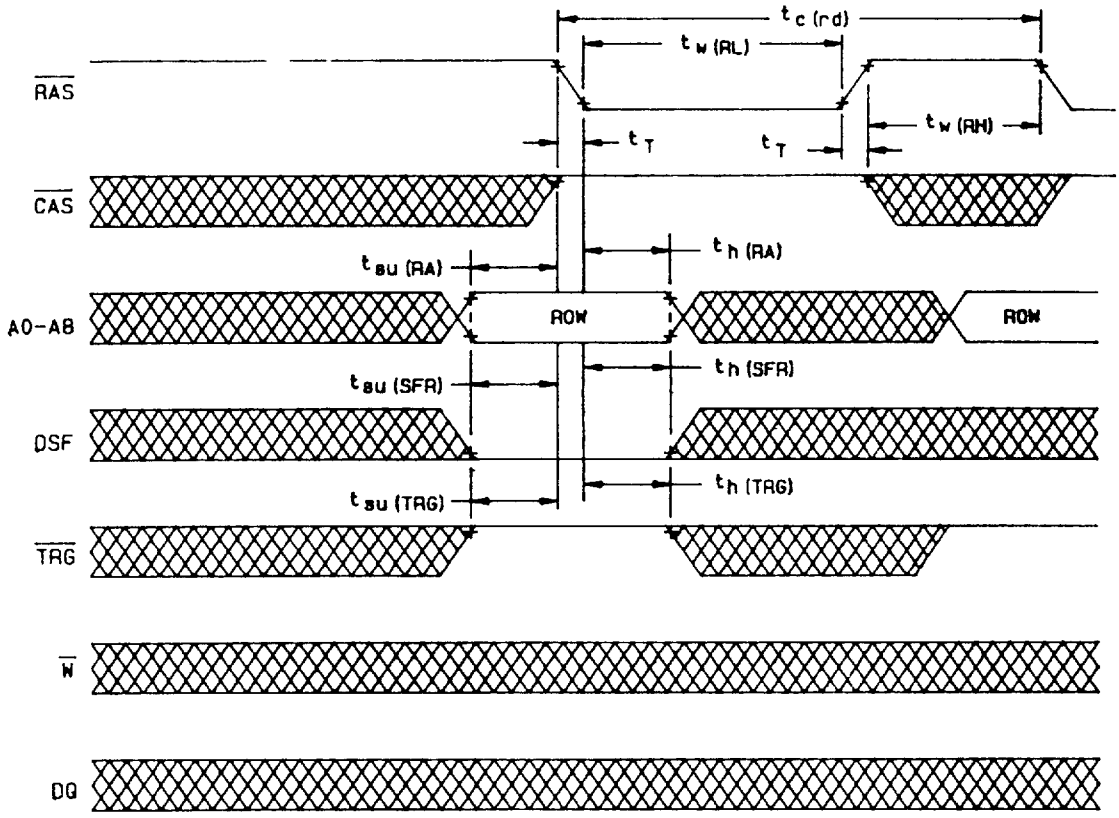


FIGURE 4. Timing waveform diagrams - Continued.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

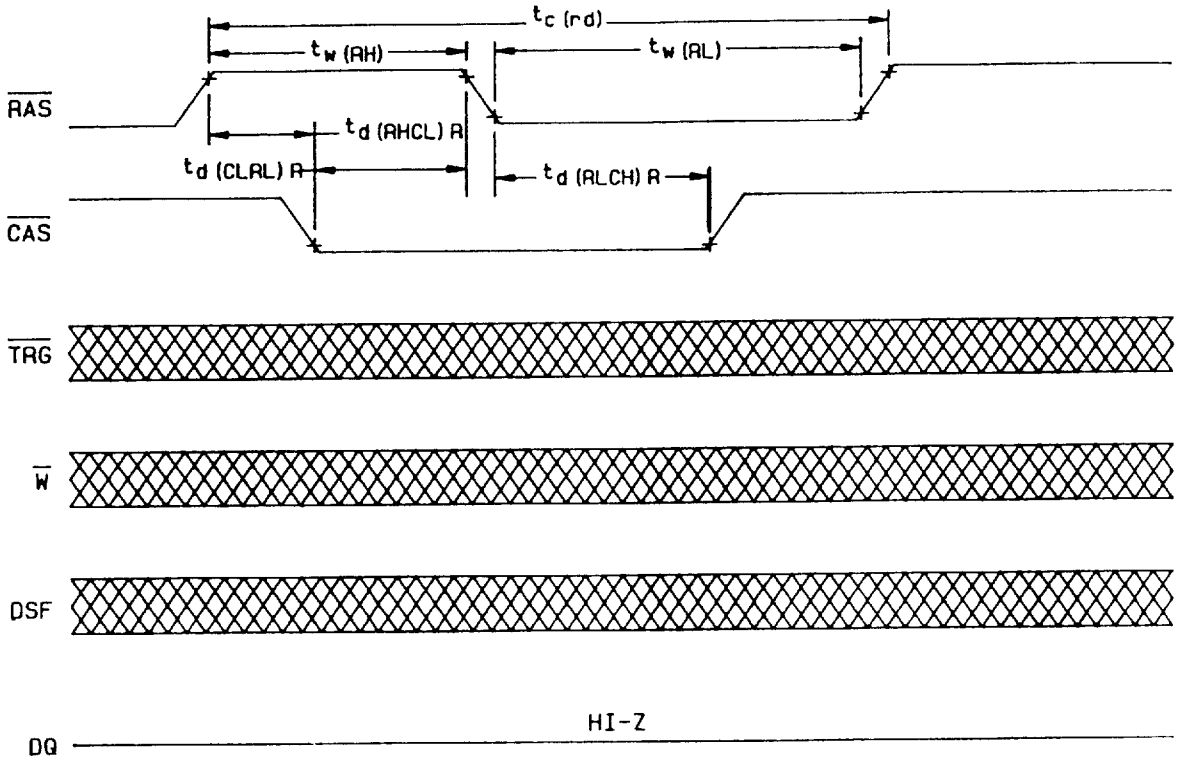


FIGURE 4. Timing waveform diagrams - Continued.

$\overline{CAS}$-before-$\overline{RAS}$ refresh counter test timing

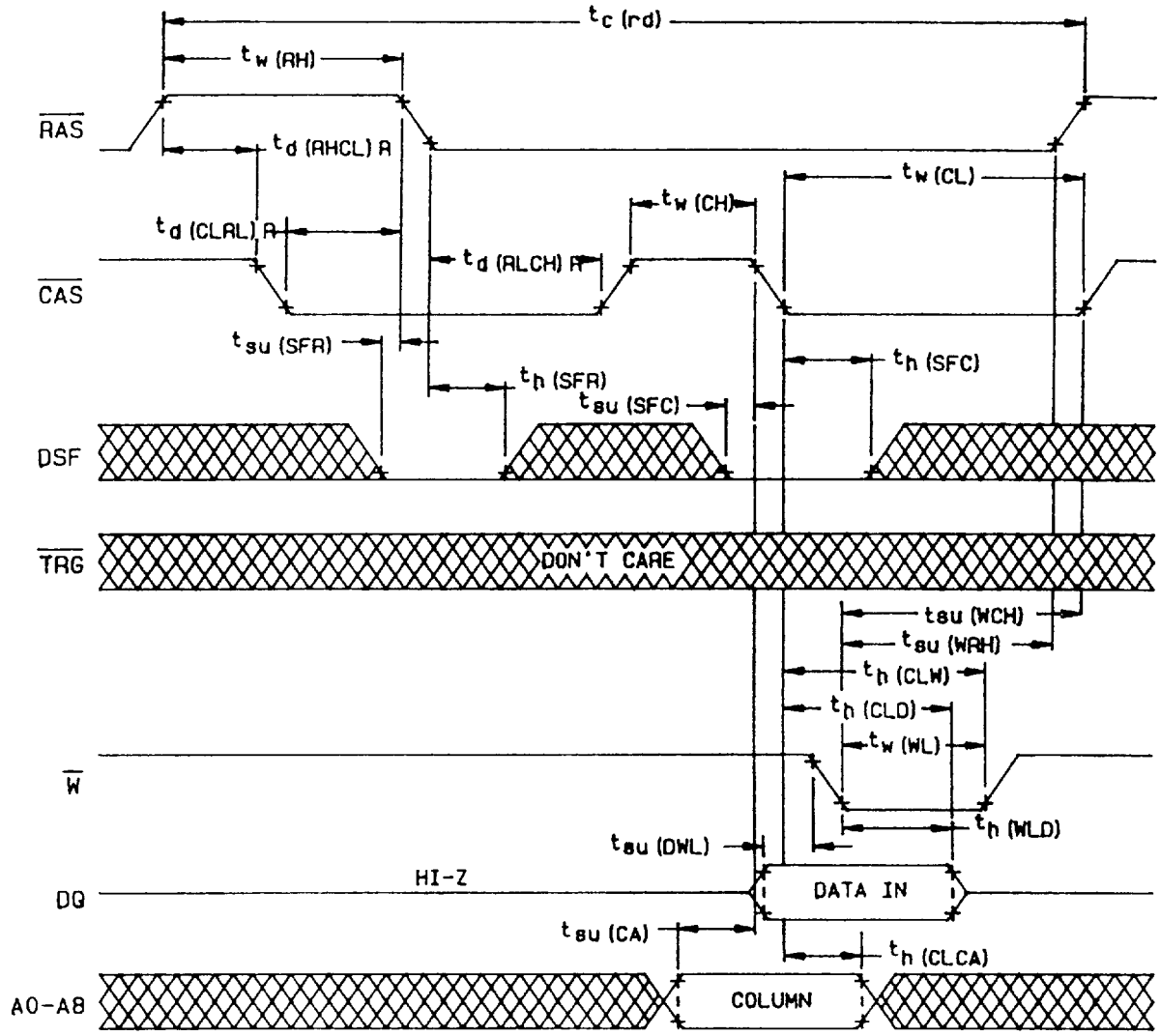


FIGURE 4. Timing waveform diagrams - Continued.

Hidden refresh cycle timing

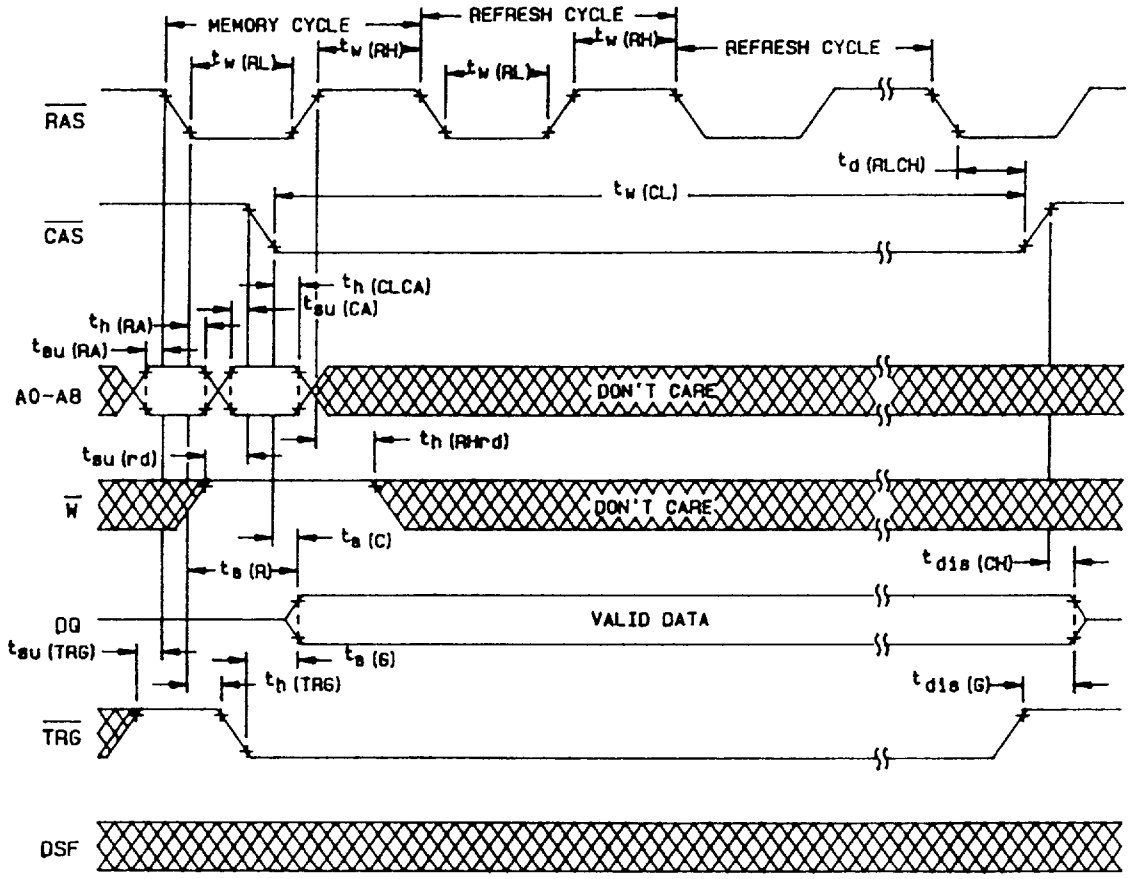
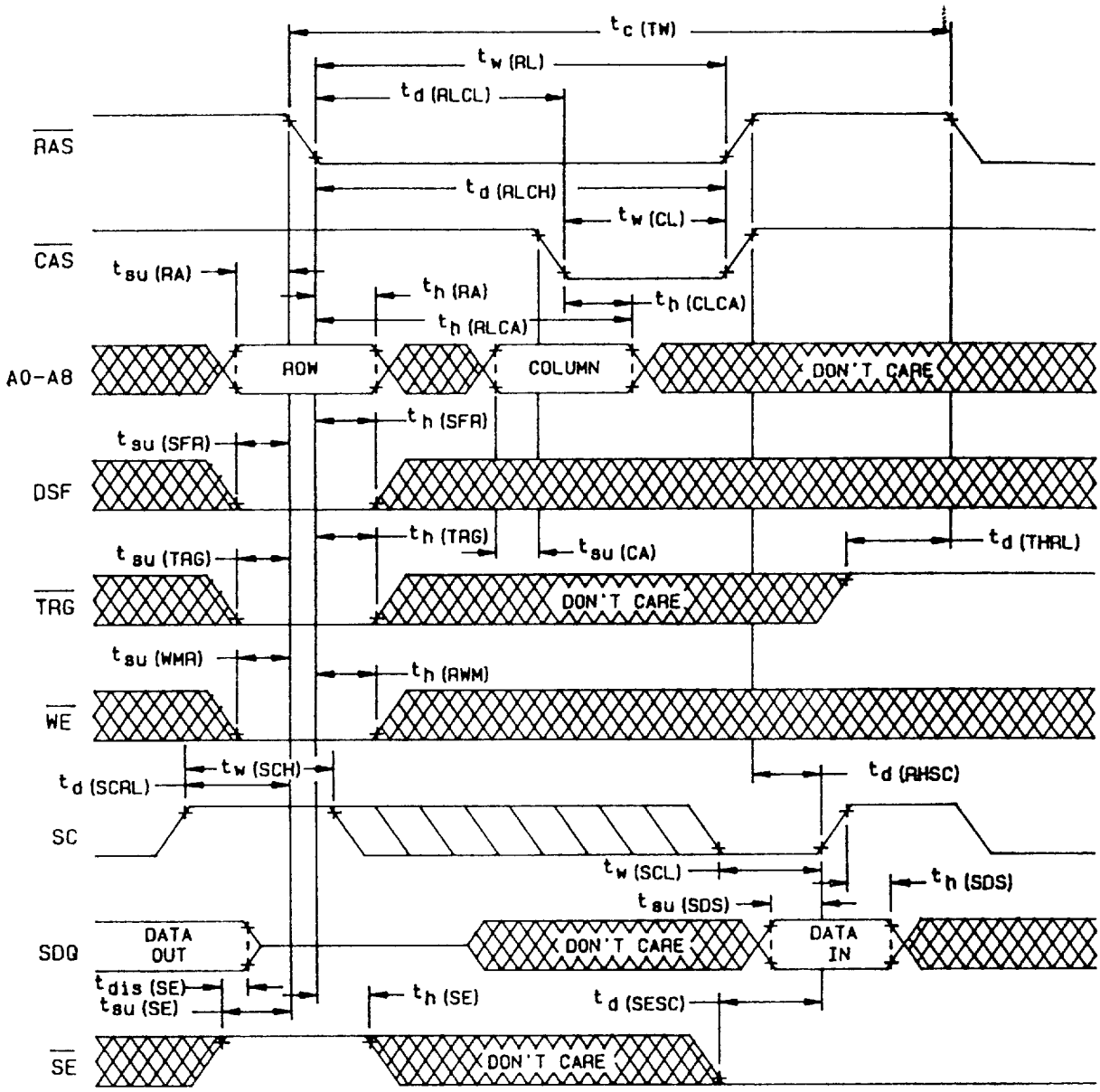


FIGURE 4. Timing waveform diagrams - Continued.

Write-mode control pseudo write transfer timing



NOTES:
1. Random-mode Q outputs remain in the high-impedance state for the entire write-mode control.
2. $\overline{SE}$ must be high as $\overline{RAS}$ falls in order to perform a write-mode control cycle.

FIGURE 4. Timing waveform diagrams - Continued.

Data register to memory timing, serial input enabled

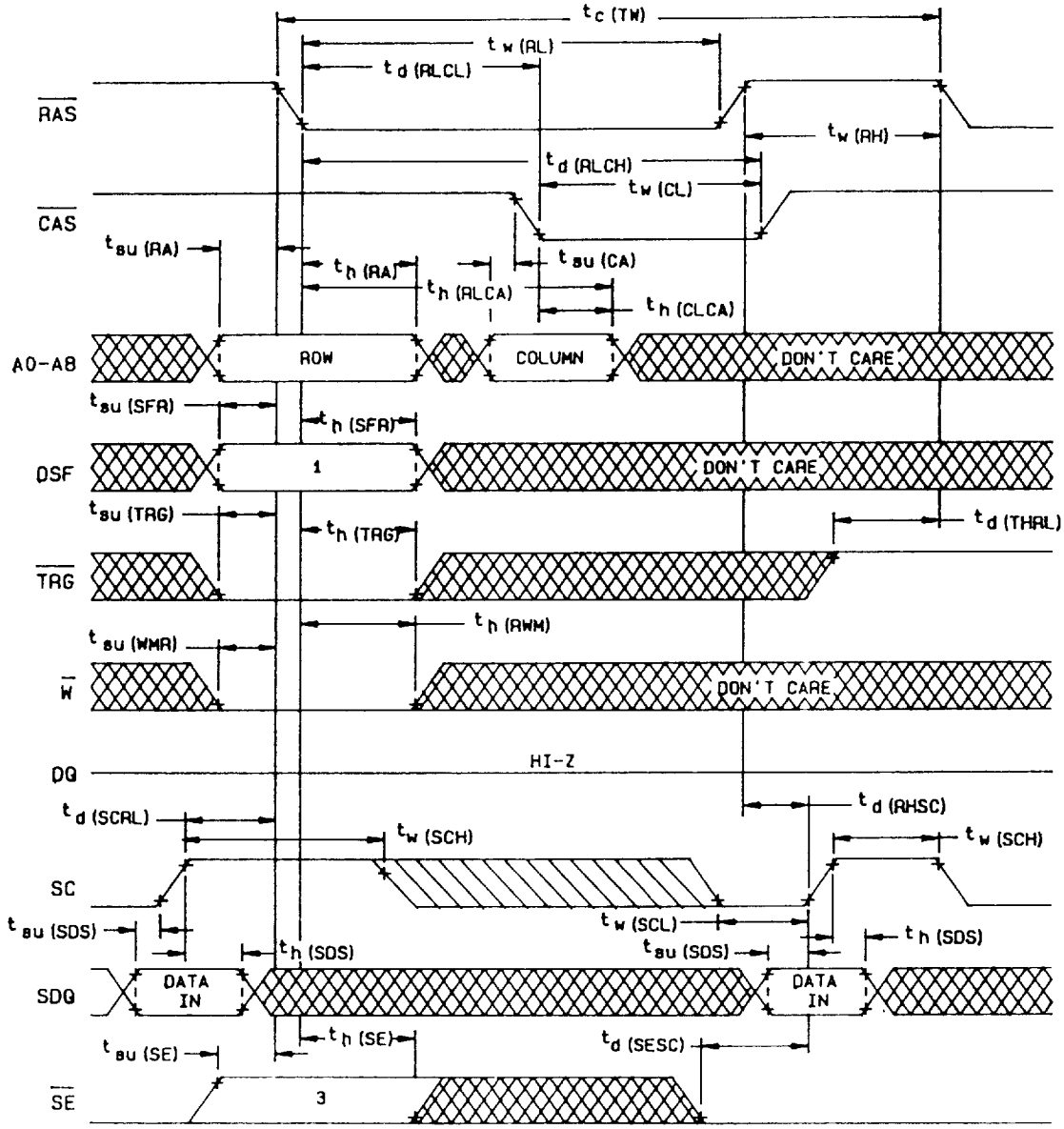


FIGURE 4. Timing waveform diagrams - Continued.

Data register to memory timing, serial input enable - Continued

NOTES:
1. Random mode Q outputs remain in the high impedance state for the entire data register to memory transfer cycle. This cycle is used to transfer data from the data register to the memory array. Every one of the 512 locations in each data register is written into the corresponding 512 columns of the selected row. Data in the data register may proceed from a serial shift-in or from a parallel load from one of the memory array rows. The above diagram assumes that the device is in the serial write mode (i.e., SD is enabled by a previous write mode control cycle, thus allowing data to be shifted-in).
2. Successive transfer writes can be performed without serial clocks for applications requiring fast memory array clears.

FIGURE 4. Timing waveform diagrams - Continued.

Register transfer function table

Function	$\overline{RAS}$ fall			
	$\overline{TRG}$	$\overline{W}$	DSF (1)	$\overline{SE}$ (3)
Register to memory transfer	L	L	H	L
Register to memory transfer, alternate transfer write	L	L	H	X
Pseudo-transfer SDQ control, serial input enabled	L	L	L	H
Memory to register transfer	L	H	L	X
Split register transfer	L	H	H	X

FIGURE 4. Timing waveform diagrams - Continued.

Alternate data register to memory timing

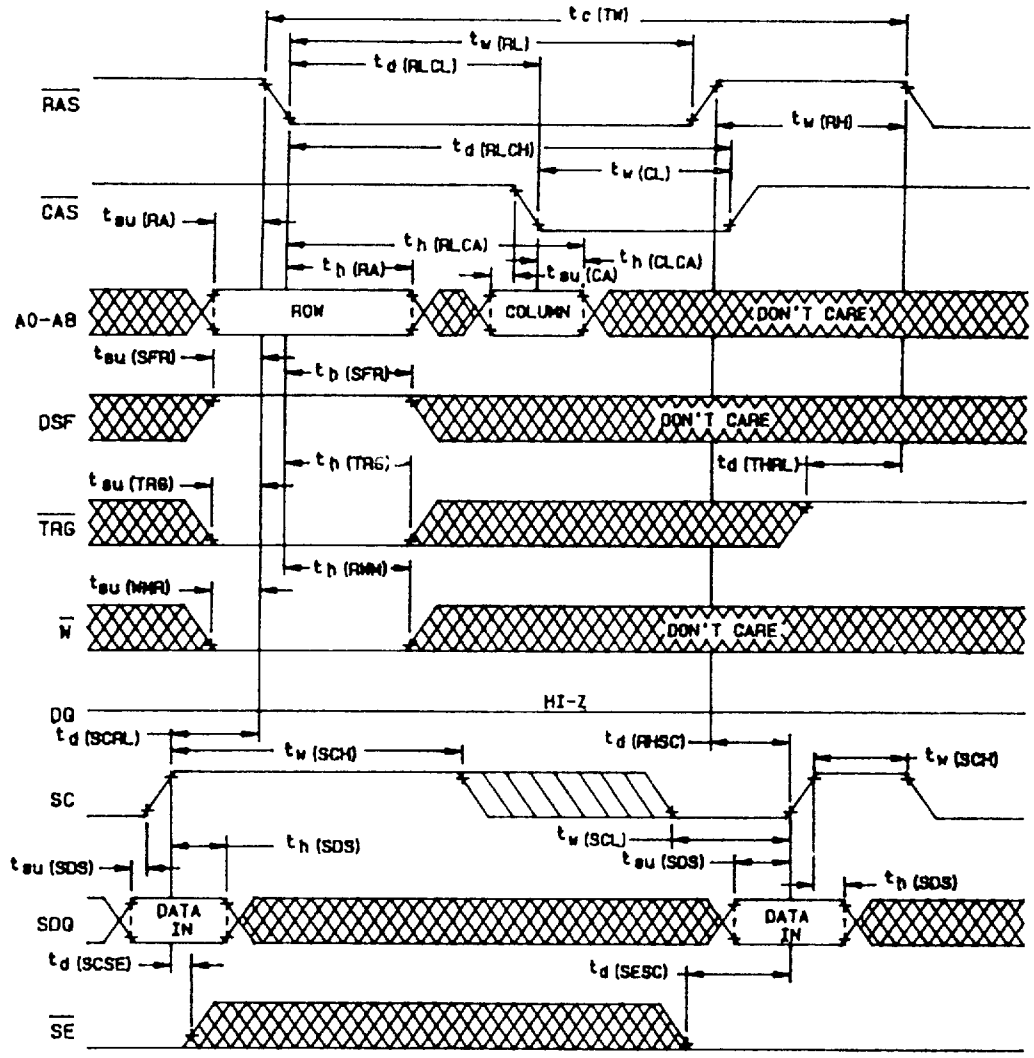
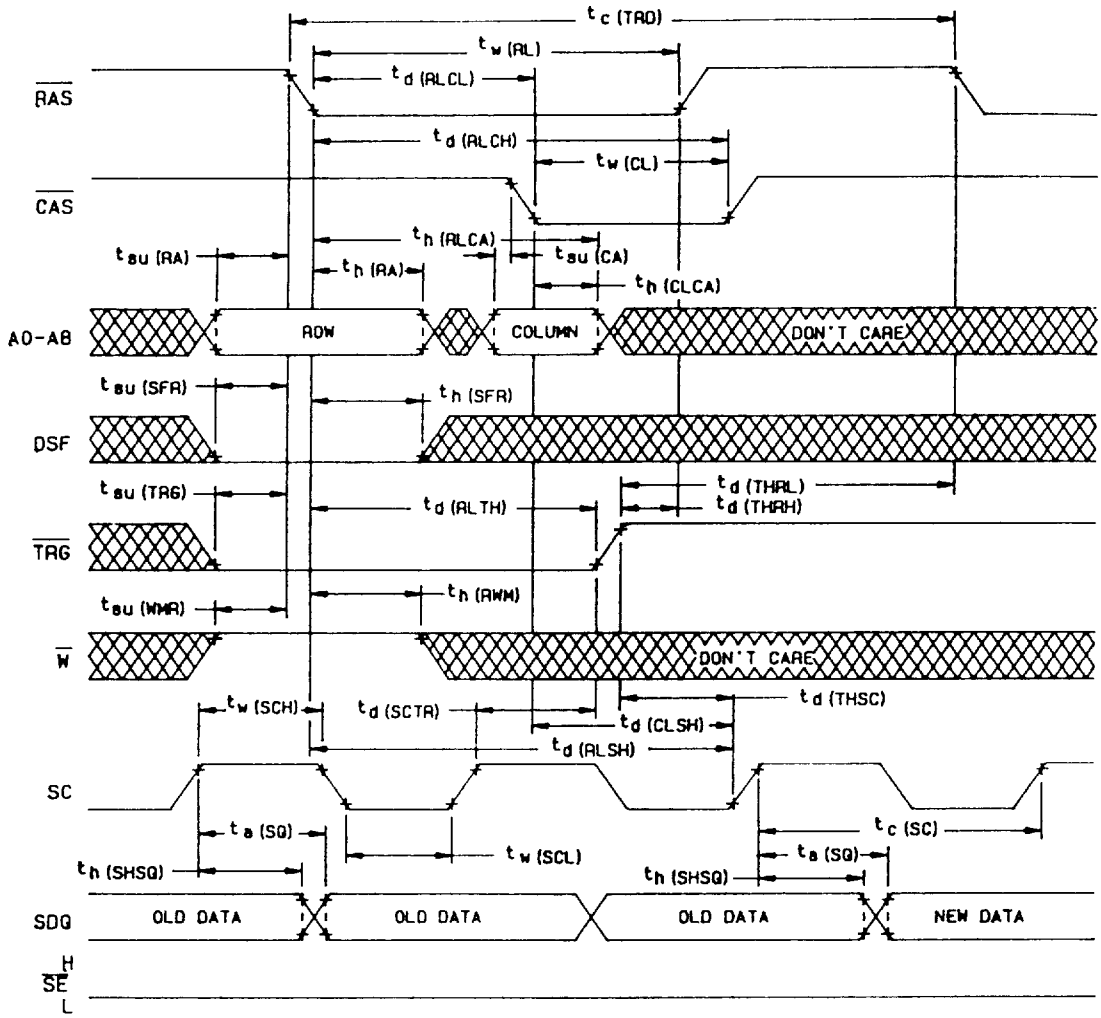


FIGURE 4. Timing waveform diagrams - Continued.

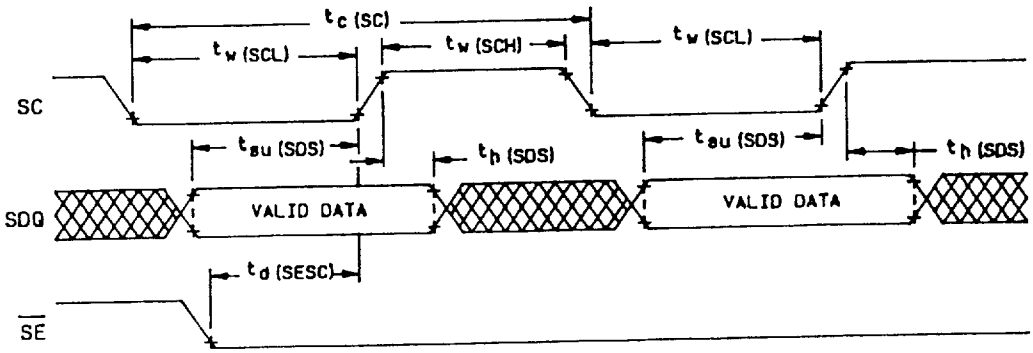
Memory to data register transfer timing



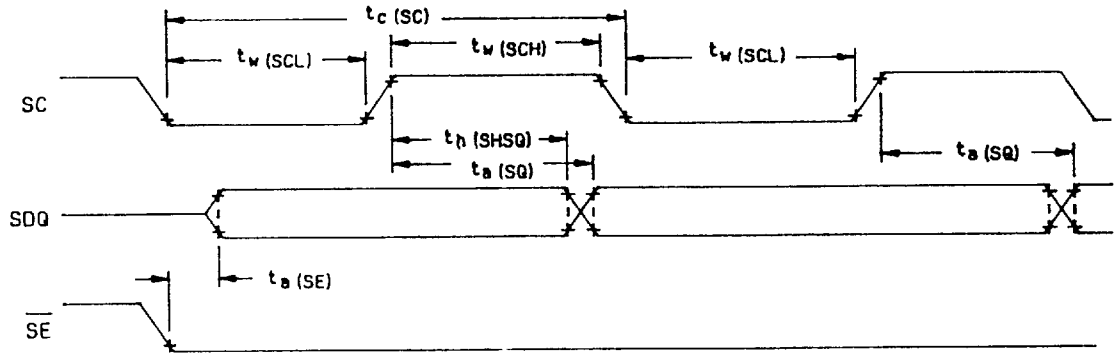
NOTE: Random mode (Q outputs) remain in the high-impedance state for the entire memory to data register transfer cycle. The memory to data register transfer cycle is used to load the data registers in parallel from the memory array. The 512 locations in each data register are written into from the 512 corresponding columns of the selected row. The data that is transferred into the data registers may be either shifted out or transferred back into another row. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), thus allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after TRG has gone high must be activated by a positive transition of SC.

FIGURE 4. Timing waveform diagrams - Continued.

Serial data-in timing

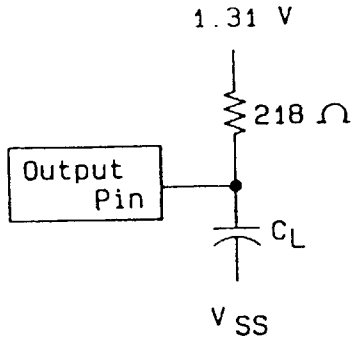


Serial data-out timing



NOTE: When the odd tap is used (tap addresses can be 0-511, and odd taps are 1, 3, 5... etc.), the cycle time for SC in the first serial data out cycle needs to be 70 ns minimum.

FIGURE 4. Timing waveform diagrams - Continued.



NOTE: For part numbers 01 and 02, QSF pin is open collector which requires 5 v with an 820 Ω pull-up resistor

FIGURE 5. Load circuit.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{CC2} standby	±1.5 mA of specified value in table IA
I_{IL}	±1.5 µA of specified value in table IA
I_O	±1.5 µA of specified value in table IA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device classes Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

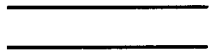
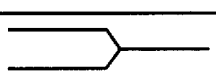
6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38535, MIL-STD-1331, and as follows:

C_I C_O	Input and bidirectional output, terminal-to-GND capacitance.
GND	Ground zero voltage potential.
I_{CC}	Supply current.
I_{IL}	Input current low
I_{IH}	Input current high
T_C	Case temperature.
T_A	Ambient temperature
V_{CC}	Positive supply voltage.
V_{IC}	Positive input clamp voltage
O/V	Latch-up over-voltage
O/I	Latch-up over-current

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a Random Access Memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Output high impedance (t_{off}). This pattern verifies the output buffer switches to high impedance (three-state) within the specified t_{OFF} after the rise of CAS. It is performed in the following manner.

Step 1: Perform 8 pump cycles.
Step 2: Load address location with data.
Step 3: Raise CAS and read address location and guarantee $V_{OL} < V_{OUT} < V_{OH}$ after T_{OFF} delay.

30.2 Algorithm B (pattern 2).

30.2.1 V_{CC} slew. This pattern indicates sense amplifier margin by slewing the supply voltage between memory writing and reading. It is performed in the following manner:

Step 1: Perform 8 pump cycles, 1 memory to register transfer and 2 SC cycles.
Step 2: Load memory with background data with V_{CC} at 5.0 V.
Step 3: Change V_{CC} to 5.5 V.
Step 4: Read memory with background data.
Step 5: Load memory with background data complement.
Step 6: Change V_{CC} to 4.5 V.
Step 7: Read memory with background data complement.

30.3 Algorithm C (pattern 3).

30.3.1 March data. This pattern tests for address uniqueness and multiple selection. It is performed in the following manner:

Step 1: Perform 8 pump cycles, 1 memory to register transfer and 2 SC cycles.
Step 2: Load memory with background data.
Step 3: Read location 0.
Step 4: Write data complement in location 0.
Step 5: Repeat steps 3 and 4 for all other locations in the memory (sequentially).
Step 6: Read data complement in maximum address location.
Step 7: Write data in maximum address location.
Step 8: Repeat steps 6 and 7 for all other locations in the memory from maximum to minimum address.
Step 9: Read data in maximum address location.
Step 10: Write data complement in maximum address location.
Step 11: Repeat steps 6 and 7 for all other locations in the memory from maximum to minimum address.
Step 12: Read memory with data complement.

30.4 Algorithm D (pattern 4).

30.4.1 Refresh test (cell retention) +125°C only. This test is used to check the retention time of the memory cells. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Pause T_{REF} (stop all clocks).
Step 4: Read memory with background data.
Step 5: Repeat steps 2, 3, and 4 with data complement.

30.5 Algorithm E (pattern 5).

30.5.1 Read-modify-write (RMW). This pattern verifies the read-modify-write mode for the memory. It is performed in the following manner:

Step 1: Perform 8 pump cycles, 1 memory to register transfer and 2 SC cycles.
Step 2: Load memory with background data.
Step 3: Read minimum address location with data and load with data complement using RMW cycle.
Step 4: Repeat step 3 for all address locations (sequentially).
Step 5: Read maximum address location with data complement and load with data using RMW cycle.
Step 6: Repeat step 5 for all address locations from maximum to minimum.

30.6 Algorithm F (pattern 6).

30.6.1 Page mode. This pattern verifies the Page mode for the memory. It is performed in the following manner:

Step 1: Perform 8 pump cycles, 1 memory to register transfer and 2 SC cycles.
Step 2: Load first page of memory with background data using page mode cycle.
Step 3: Repeat step 2 for remaining rows.
Step 4: Read first page of memory with data and load with data complement using page mode cycle.
Step 5: Repeat step 4 for remaining rows.
Step 6: Read first page of memory with data complement and write data starting at maximum Y address and decrementing Y address.
Step 7: Repeat step 6 for remaining rows.

30.7 Algorithm G (pattern 7).

30.7.1 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ counter test. This test is used to verify the functionality of the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ internal address counter.

Step 1: Perform 8 pump cycles, 1 memory to register transfer and 2 SC cycles.
Step 2: Write data to one column of memory.
Step 3: Perform 512 CBR cycles presenting data complement, but not changing the address presented.
Step 4: Read data complement from the column written to in step 2.
Step 5: Perform 512 CBR cycles presenting data, but not changing the address presented.
Step 6: Read data from the column written to in step 2.

30.8 Algorithm H (pattern 8).

30.8.1 Memory to register test. This test is used to verify the functionality of the memory to register transfer circuitry.

Step 1: Perform 8 pump cycles, 1 memory to register transfer and 2 SC cycles.
Step 2: Write one row of data to the memory.
Step 3: Transfer this row to the serial register.
Step 4: Read data out of the serial register.
Step 5: Repeat steps 2 through 4 with data complement.
Step 6: Repeat steps 2 through 5 for the remaining rows.

30.9 Algorithm I (pattern 9).

30.9.1 Register to memory transfer test. This test is used to verify the functionality of the register to memory transfer circuitry.

Step 1: Perform 8 pump cycles, 1 memory to register transfer and 2 SC cycles.
Step 2: Write one row of data complement to memory.
Step 3: Transfer this row to the serial register.
Step 4: Write entire memory array with data.
Step 5: Transfer serial register to first row of memory.
Step 6: Repeat step 5 for remaining rows of memory.
Step 7: Read data complement for entire memory array.

30.10 Algorithm J (pattern 10).

30.10.1 Serial input test. This test is used to verify the functionality of the serial input circuitry.

Step 1: Perform 8 pump cycles, 1 memory to register transfer and 2 SC cycles.
Step 2: Write entire memory array with data.
Step 3: Transfer the first row of memory to the serial register.
Step 4: Perform a pseudo transfer write cycle.
Step 5: Shift one row of data complement into serial register.
Step 6: Transfer serial register to first memory row.
Step 7: Repeat steps 5 through 6 until entire memory array is written to.
Step 8: Read data complement from entire array.

30.11 Algorithm K (pattern 11).

30.11.1 Serial output test. This test is used to verify the functionality of the serial output and tap circuitry.

Step 1: Perform 8 pump cycles, 1 memory to register transfer and 2 SC cycles.
Step 2: Write one row of data into memory array.
Step 3: Write data complement into tap point.
Step 4: Perform memory to register transfer on row written to.
Step 5: Read data complement from tap point.
Step 6: Read data for all bits beyond tap point.
Step 7: Increment tap point.
Step 8: Repeat steps 2 through 7 511 times.