REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26							

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
92-11-04

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, CHMOS SINGLE-CHIP, 8-BIT MICROCONTROLLER WITH 256 BYTES OF ON CHIP DATA RAM, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-90976
A	67268	

SHEET 1 OF 26

DESC FORM 193
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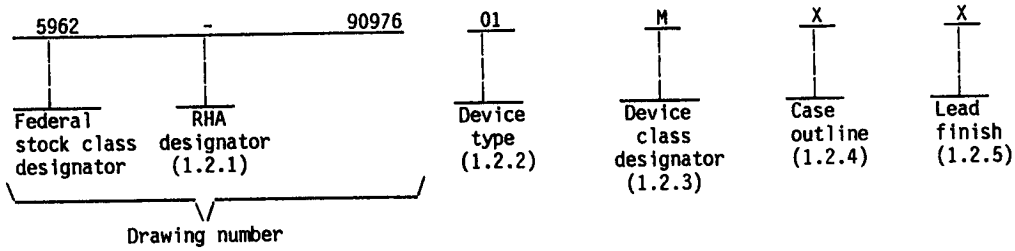
5962-E042

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V devices shall meet or exceed the electrical performance characteristics specified in table I herein after exposure to the specified irradiation levels specified in the absolute maximum ratings herein and the RHA marked device shall be marked in accordance with MIL-I-38535. A dash (-) indicates a non RHA device.

1.2.2 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	80C51FB	CHMOS single chip 8-bit microcontroller
02	80C51FB-16	CHMOS single-chip 8-bit microcontroller

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for NON-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
T	See figure 1	44	J-leaded ceramic chip carrier
U	CQCC1-N44	44	Square leadless chip carrier
X	GDIP1-T40 or CDIP2-T40	40	Dual-in-line
Z	See figure 1	44	Gullwing-lead ceramic chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, or C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Storage temperature range	-65°C to +150°C
Voltage on $\overline{EA}/V_{PP}$ pin to V_{SS}	0.0 V dc to +13.0 V dc
Voltage on any other pin to V_{SS}	-0.5 V dc to +6.5 V dc
Maximum I_{OL} per I/O pin	15 mA
Power dissipation (P_D)	1.5 W 1/
Lead temperature (soldering 10 seconds)	265°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases U and X	See MIL-STD-1835
Cases T and Z	14°C/W
Junction temperature	+150°C

1.4 Recommended operating conditions.

Case Operating Temperature Range	-55°C to +125°C 2/
Supply Voltage, V_{CC}	+4.0 V dc to 6.0 V dc
Oscillator frequency:	
Device 01	3.5 MHz to 12 MHz
Device 02	3.5 MHz to 16 MHz

1.5 Digital testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 3/

1/ Power dissipation based on package heat transfer limitations, not device power consumption.
2/ Case temperatures are instant on.
3/ Values will be added when they become available.

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for
MIL-M-38510 - Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit case outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant NON-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S a full electrical characterization table for each device type shall be included in this SMD when a qualified source exists. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and post irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post irradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein) or for device classes Q and V the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M notification to DESC-ECC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. The following additional criteria shall apply.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. For device class M the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S the test circuit shall be submitted to the qualifying activity.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $4.0\ V \le V_{CC} \le 6.0\ V$ $V_{SS} = 0.0\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}		1,2,3	All	- 0.5 2/	$0.2\ V_{CC}$ -0.25	V
Input high voltage (except XTAL1, RST)	V_{IH}				$0.2\ V_{CC}$ +0.9	V_{CC}+0.5 2/	
Input high voltage (XTAL1 and RST)	V_{IH1}				$0.7\ V_{CC}$	V_{CC}+0.5 2/	
Output low voltage (ports 1,2,3) 3/	V_{OL}	I_{OL} = 100 µA 4/ I_{OL} = 1.6 mA I_{OL} = 3.5 mA				0.3 0.45 1.0	
Output low voltage (Port 0, ALE, PSEN) 3/	V_{OL1}	I_{OL} = 200 µA 4/ I_{OL} = 3.2 mA I_{OL} = 7.0 mA				0.3 0.45 1.0	
Output high voltage (Ports 1, 2, 3,) ALE, PSEN	V_{OH}	I_{OH} = -10 µA I_{OH} = -30 µA I_{OH} = -60 µA			V_{CC}-0.3V V_{CC}-0.7V V_{CC}-1.5V		
Output high voltage (Port 0 in external bus mode,)	V_{OH1}	I_{OH} = -200 µA 5/ I_{OH} = -3.2 mA I_{OH} = -7.0 mA			V_{CC}-0.3V V_{CC}-0.7V V_{CC}-1.5V		
Logical 0 input current (Ports 1, 2 and 3)	I_{IL}	V_{IN} = 0.45 V				-75	µA
Input leakage current (Port 0)	I_{LI}	$.45 \le V_{IN} \le V_{CC}$				±10	
Logical 1 to 0 transition current (Ports 1, 2 and 3)	I_{TL}	V_{IN} = 2.0 V				-750	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $4.0\ V \le V_{CC} \le 6.0\ V$ $V_{SS} = 0.0\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Address to valid instruction in	t_{AVIV}	Load capacitance for Port 0, ALE/PROG and PSEN = 100 pF, load capacitance for all other outputs = 80 pF 8/ See figure 4	9, 10 11	All		$5t_{CLCL}$ -105	ns
PSEN low to ADDRESS float	t_{PLAZ}					10	
RD pulse width	t_{RLRH}				$6t_{CLCL}$ -100		
WR pulse width	t_{WLWH}				$6t_{CLCL}$ -100		
RD low to valid data in	t_{RLDV}					$5t_{CLCL}$ -165	
Data hold after RD	t_{RHDX}				0		
Data float after RD	t_{RHDZ}					$2t_{CLCL}$ -60	
ALE low to valid data in	t_{LLDV}					$8t_{CLCL}$ -150	
Address to valid data in	t_{AVDV}					$9t_{CLCL}$ -165	
Ale low to RD or WR low	t_{LLWL}				$3t_{CLCL}$ -50	$3t_{CLCL}$ +50	
Address valid to WR low	t_{AVWL}				$4t_{CLCL}$ -130		
Data valid before WR	t_{QVWX}				t_{CLCL} -50		
Data hold after WR	t_{WHQX}				t_{CLCL} -50		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ $4.0\ V \le V_{CC} \le 6.0\ V$ $V_{SS} = 0.0\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data valid to WR high	t_{QVWH}	Load capacitance for Port 0, ALE/PROG and PSEN = 100 pF, load capacitance for all other outputs = 80 pF 8/ See figure 4	9, 10 11	All	$7t_{CLCL}$ -150		ns
RD low to Address float	t_{RLAZ}					0	
RD or WR high to ALE high	t_{WHLH}				t_{CLCL} -40	t_{CLCL} +40	
Serial port clock cycle time	T_{XLXL}	Serial port timing - shift register mode load capacitance = 80 pF See figure 4	9, 10 11	All	$12t_{CLCL}$		
Output data setup to clock rising edge	t_{QVXH}				$10t_{CLCL}$ -133		
Output data hold after clock rising edge	t_{XHQX}				$2t_{CLCL}$ -117		
Input data hold after clock rising edge	t_{XHDX}				0		
Clock rising edge to input data valid	t_{XHDV}					$10t_{CLCL}$ -133	
Oscillator frequency 8/	$1/t_{CLCL}$	External clock drive See figure 4		01 02	3.5 3.5	12 16	MHz
High time	t_{CHCX}			All	20		ns
Low time	t_{CLCX}				20		
Rise time 2/	t_{CLCH}					20	
Fall time 2/	t_{CHCL}					20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ The following pins are active low: $\overline{INT0}$, $\overline{INT1}$, $\overline{WR}$, $\overline{RD}$, $\overline{EA}$ of $\overline{EA}/V_{PP}$, $\overline{PROG}$ of ALE/$\overline{PROG}$, and $\overline{PSEN}$. Case temperatures are instant on. Unless otherwise specified, all test conditions shall be worst case condition.

2/ Guaranteed to the limits specified in table I, if not tested.

3/ Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin:	10 mA
Maximum I_{OL} per 8-bit port - port 0:	26 mA
Maximum I_{OL} per ports 1, 2 and 3:	15 mA
Maximum total I_{OL} for all output pins:	71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed conditions.

4/ Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1 to 0 transitions during bus operations. In applications where capacitance loading exceeds 100 pF, the noise pulse on the ALE signal may exceed 0.8 V. In these cases, it may be desirable to qualify ALE with schmitt trigger, or use an address latch with a schmitt trigger strobe input.

5/ Capacitive loading on ports 0 and 2 cause the V_{OH} on ALE and PSEN to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.

6/ Minimum V_{CC} for power down is 2.0V.

7/ I_{CC} is measured with all output pins and XTAL2 disconnected; XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} - 0.5$ V measured with EA and RST connected to V_{CC}. Idle and power down currents measured with EA and RST connected to V_{SS}. Power down currents measured with XTAL1 connected to V_{SS}.

8/ Timings tested at 16 MHz only but guaranteed across the specified operating frequency range.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein.

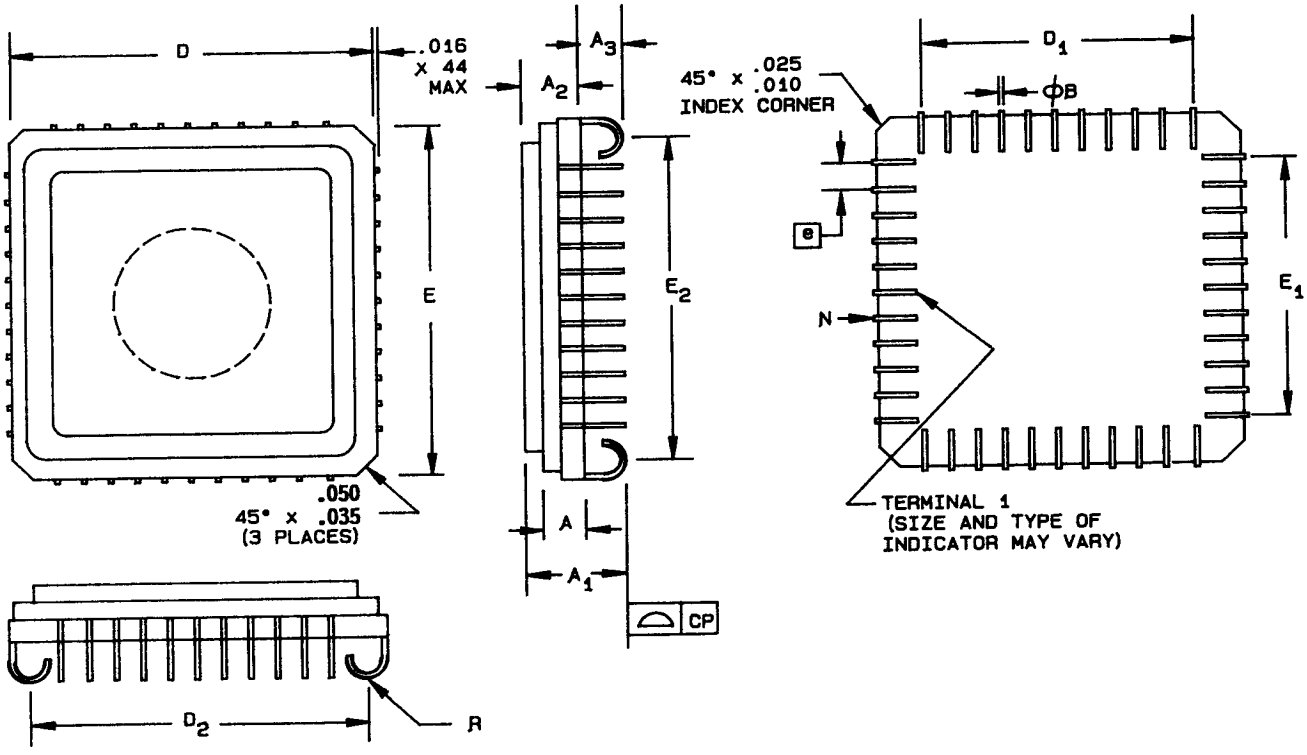


FIGURE 1. Ceramic chip carrier, "J" leaded package.

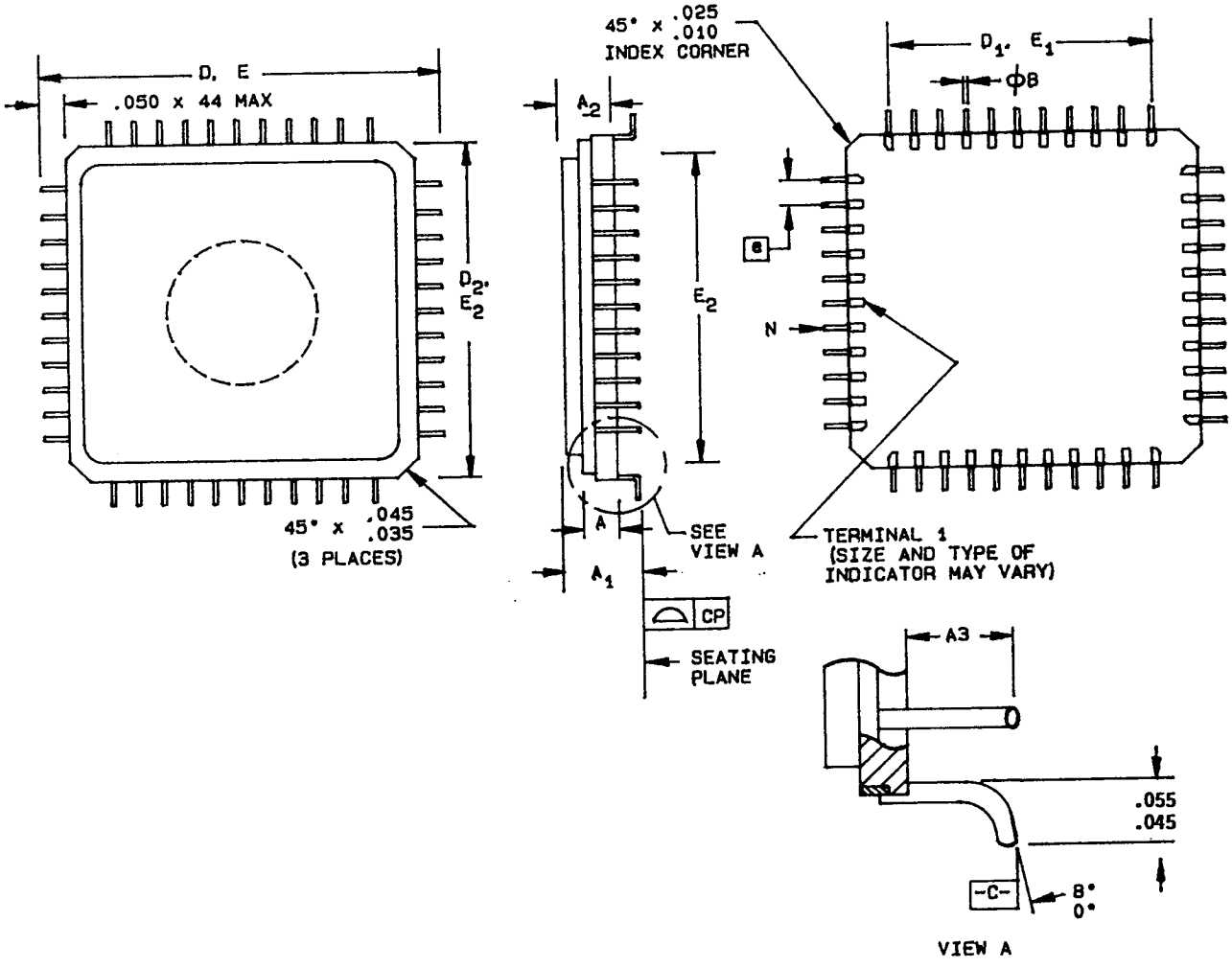
STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90976
		REVISION LEVEL	SHEET 11

Family: Ceramic leadless chip carrier						
Symbol	Inches			Millimeters		
	Min	Max	Notes	Min	Max	Notes
A	.060	.088		1.52	2.23	
A_1	.128	.170		3.25	4.55	
A_2	.073	.102		1.85	2.59	
A_3	.055	.065		1.40	1.65	
B	.014	.018		0.35	0.46	
CP	.000	.004		0.00	0.10	
D	.640	.670		16.25	17.02	
D_1	.500		Reference	12.70		Reference
D_2	.600			15.24		
E	.640	.670		16.25	17.02	
E_1	.500		Reference	12.70		Reference
E_2	.600		Reference	15.24		Reference
|e|	.044	.056		1.12	1.42	
N	44			44		
R	.027	.033		0.69	0.84	

N = Number of terminals

FIGURE 1. Ceramic chip carrier, "J" leaded package - Continued.

Case Z



Ceramic chip carrier, gull-wing leaded package

FIGURE 1. Case outlines - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90976
		REVISION LEVEL	SHEET 13

DESC FORM 193A
JUL 91

Family: Ceramic leadless chip carrier						
Symbol	Inches			Millimeters		
	Min	Max	Notes	Min	Max	Notes
A	.060	.090		1.52	2.29	
A_1	.128	.170		3.25	4.32	
A_2	.073	.102		1.85	2.59	
A_3	.055	.065		1.40	1.65	
B	.014	.018		0.35	0.46	
CP	.000	.004		0.00	0.10	
D,E	.716	.748		18.19	19.00	
D_1,E_1	.500		Reference	12.70		Reference
D_2,E_2	.640	.660		16.25	16.76	
|e|	.044	.056		1.12	1.42	
N	44			44		

N = Number of terminals

FIGURE 1. Ceramic chip carrier, gull wing leaded package - Continued.

Case X

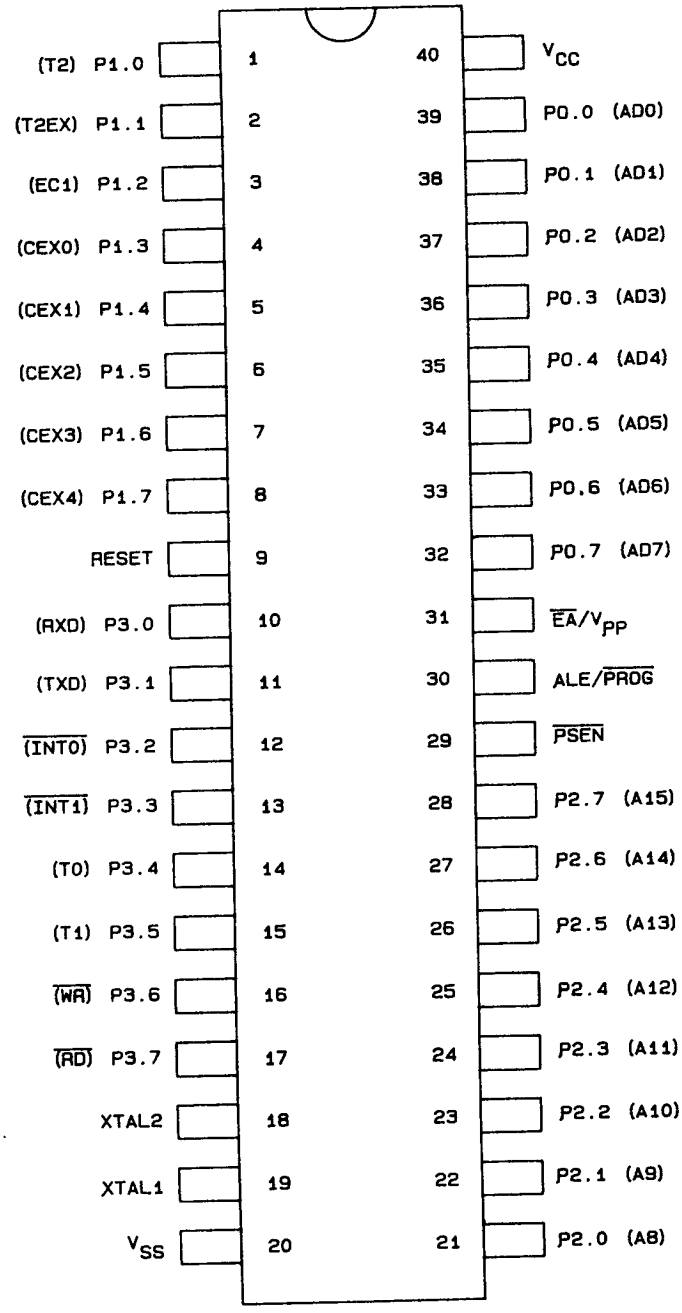
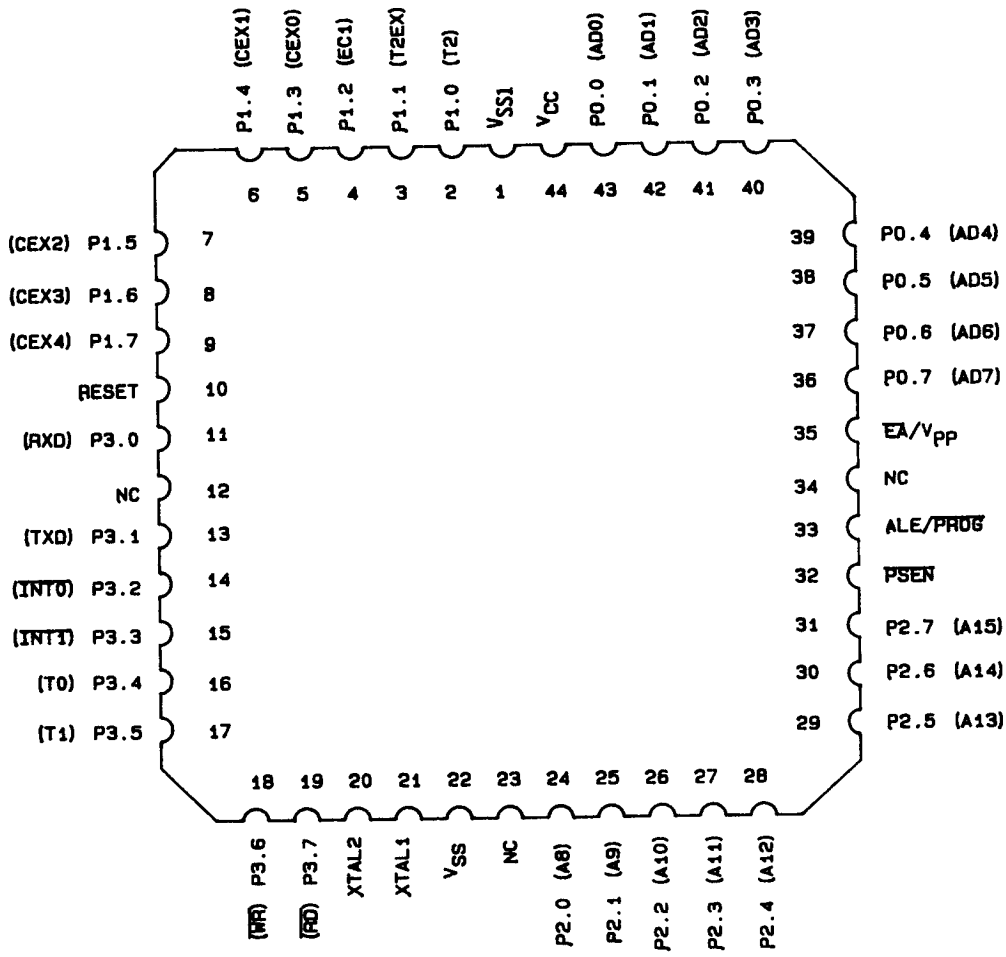


FIGURE 2. Terminal connections.

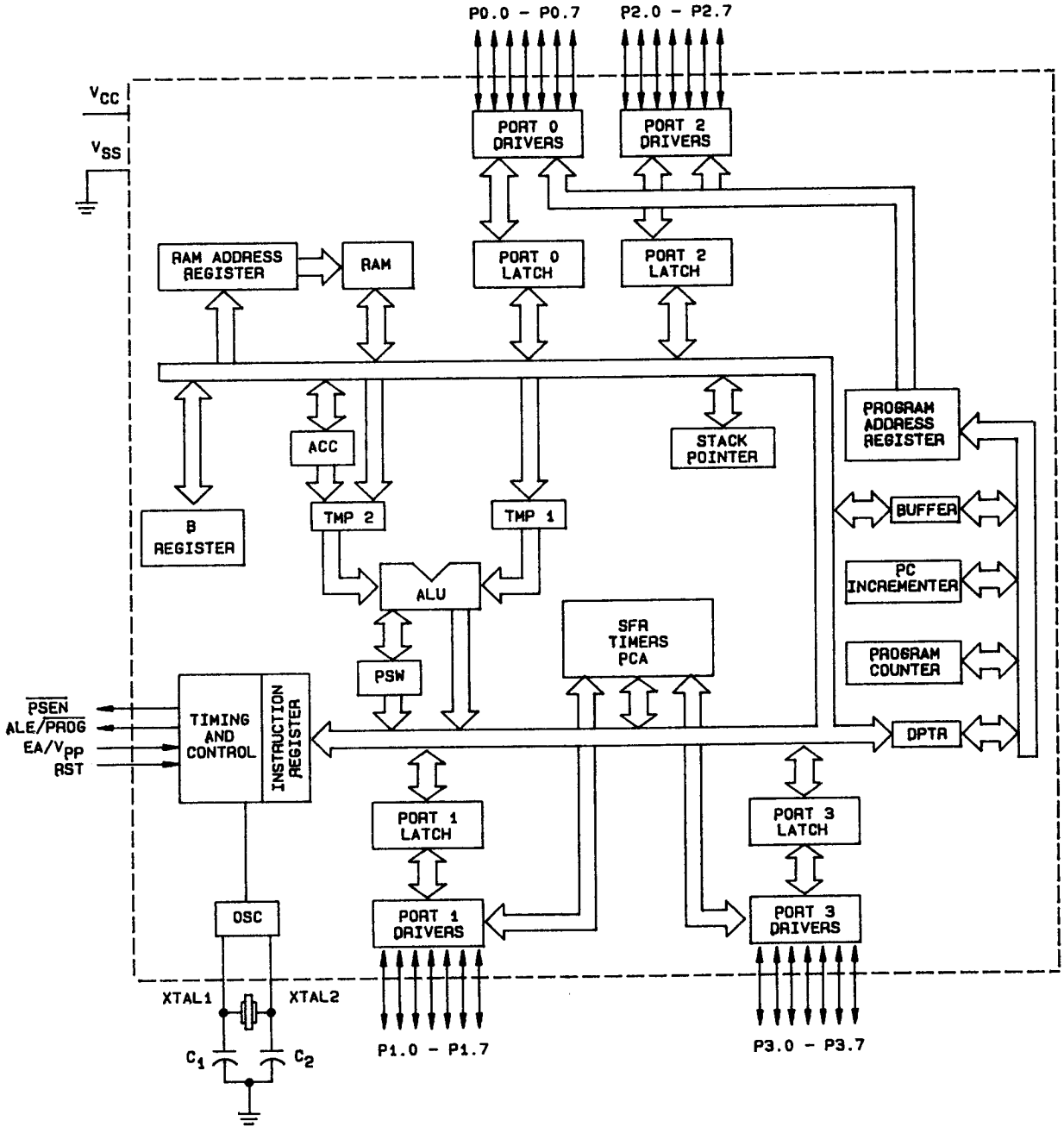
Cases T, U, and Z



NC = NO CONNECTION

Top view

FIGURE 2. Terminal connections - Continued.

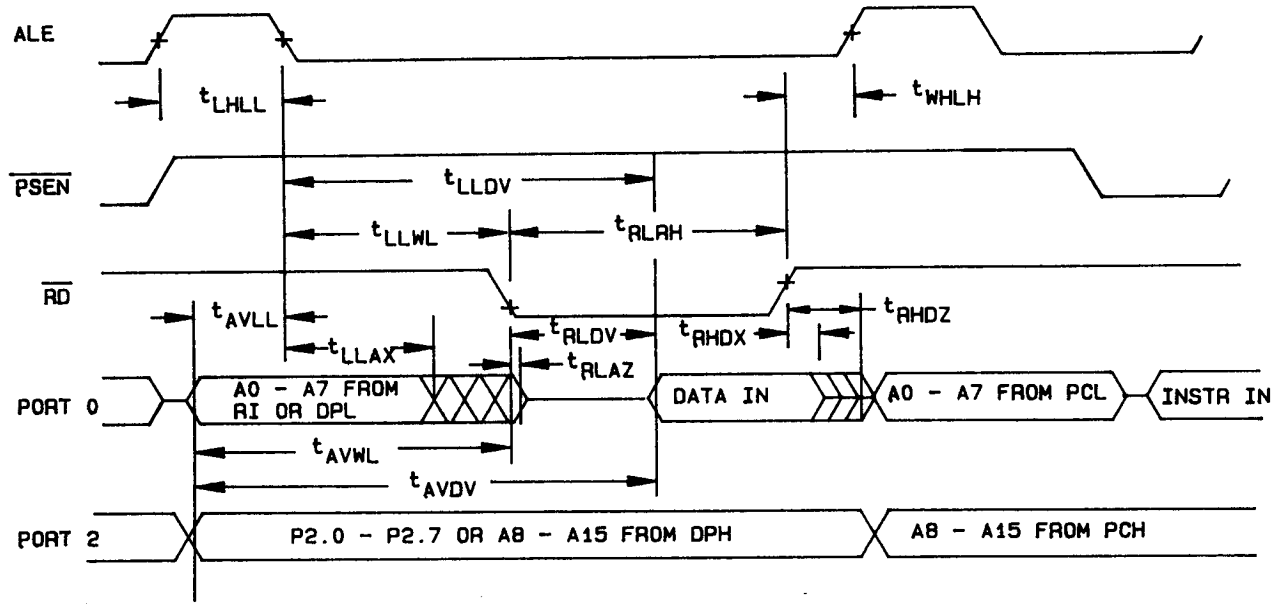


NOTE: C_1, C_2 = 30 pF ±10 pF for crystals.
= 10 pF for ceramic resonators.

FIGURE 3. Functional block diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90976
		REVISION LEVEL	SHEET 17

External data memory read cycle



External program memory read cycle

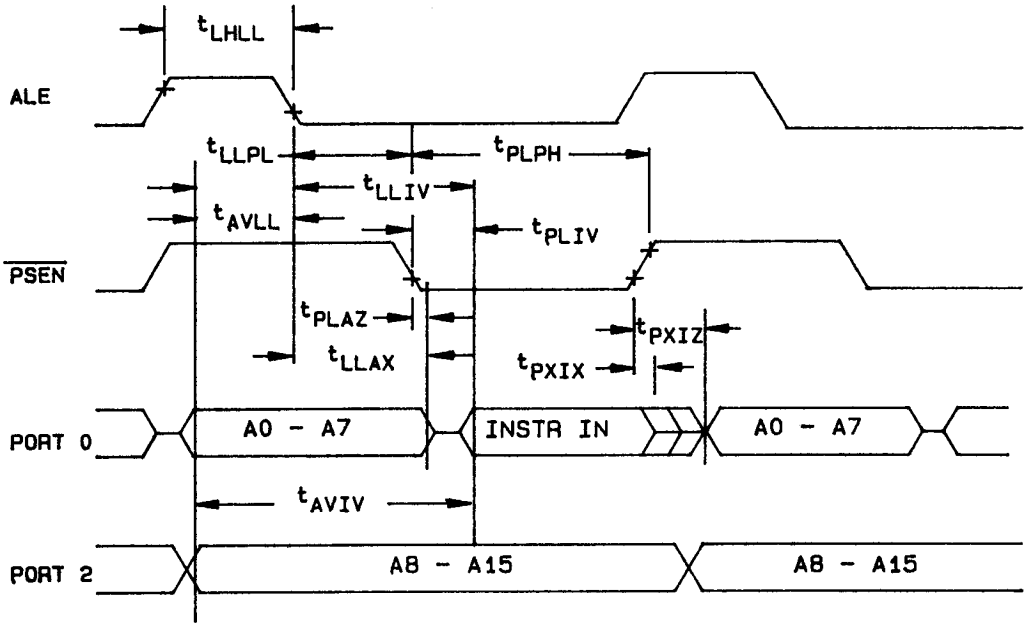
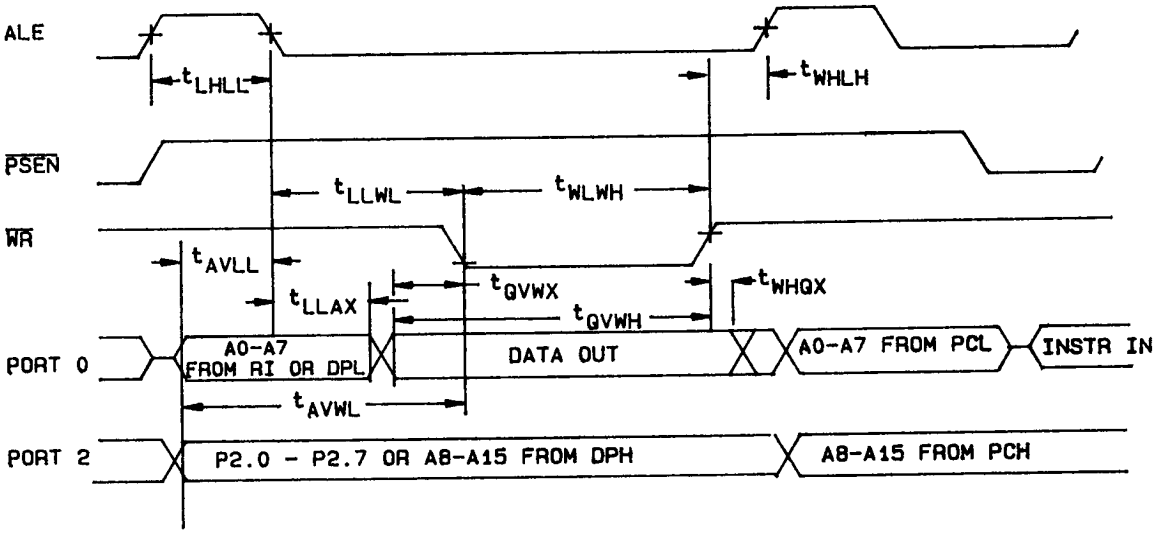


FIGURE 4. Switching waveforms and test circuit.

External data memory write cycle



External clock drive waveform

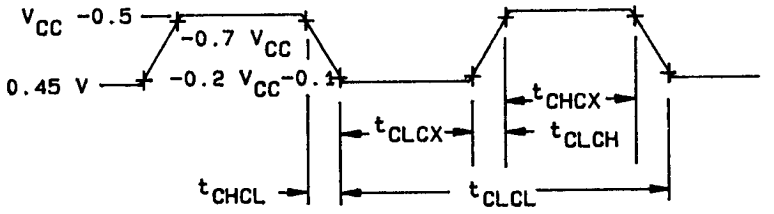
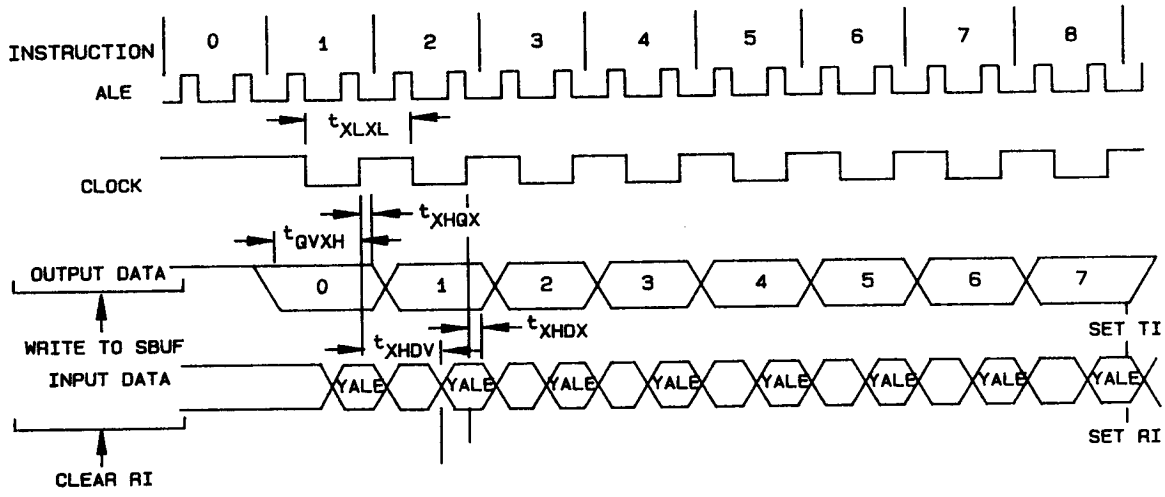
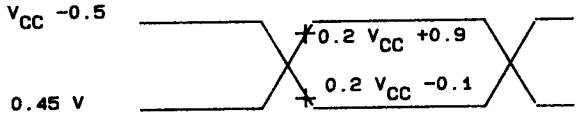


FIGURE 4. Switching waveforms and test circuit - Continued.

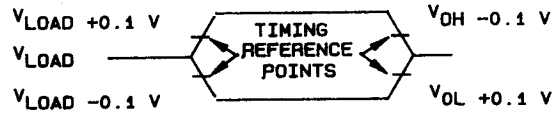
Shift register mode timing waveforms



AC testing input
Input, output waveforms

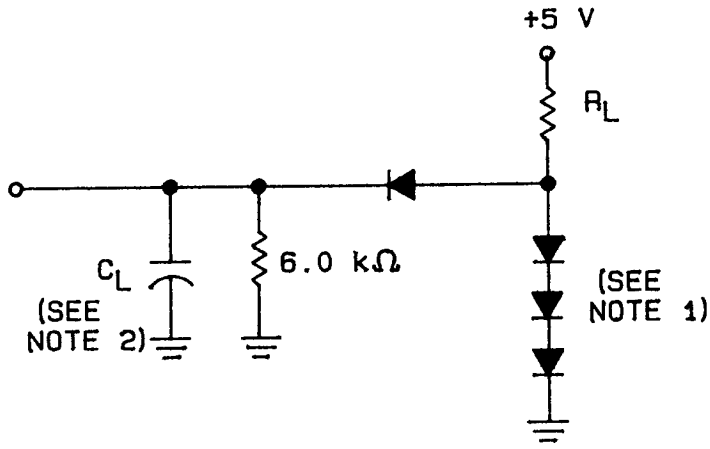


Float waveforms



NOTES:
1. Ac inputs during testing are driven at V_{CC} -0.5 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at V_{IH} minimum for a logic "1" and V_{IL} maximum for a logic "0".
2. For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

FIGURE 4. Switching waveforms and test circuit - Continued.



Output	R_L	C_L
Port 0, ALE, PSEN	1.2 kΩ	100 pF
All other outputs	2.4 kΩ	80 pF

NOTES:
1. All diodes are 1N914 or equivalent.
2. C_L includes tester and fixture capacitance.

FIGURE 4. Switching waveforms and test circuit - Continued.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. These test form a part of the manufacturers test tape and shall be maintained and available from the approved source of supply. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroups 5 and 6 in table I., method 5005 of MIL-STD-883 shall be omitted.

d. Subgroup 4 (C_{IO} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures, and all input and output terminals tested.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 Additional criteria for device classes M, B, and S. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition C or D. For device class M the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S the test circuit shall be submitted to the qualifying activity.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECS with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

4.4.4 Group D inspection. For group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B and S shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the level specified in the acquisition document. RHA tests for device classes Q and V shall be performed in accordance with MIL-I-38535 and 1.2.1 herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)	----		1,7		1,7
Final electrical parameters (see 4.2)	1/ 1,2,3, 7,8,9, 10,11	1/ 1,2,3 7,8,9, 10,11	2/ 1,2,3 7,8,9, 10,11	1/ 1,2,3 7,8,9, 10,11	2/ 1,2,3 7,8,9, 10,11
Group A test requirements (see 4.4)	1,2,3,4 7,8,9, 10,11	1,2,3,4 7,8,9, 10,11	1,2,3,4 7,8,9, 10,11	1,2,3,4 7,8,9, 10,11	1,2,3,4 7,8,9, 10,11
Group B end-point electrical parameters (see 4.4)	----		2,8A,10		
Group C end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10		2,8A,10	2,8A,10
Group D end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10	2,8A,10	2,8A,10	2,8A,10
Group E end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10	2,8A,10	2,8A,10	2,8A,10

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

a. RHA tests for device classes B and S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IIA herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table IIA herein.

d. For device classes M, B, and S the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for RHA level being tested, and meet the post irradiation end-point electrical parameter limits as defined in table I at T_A = 25°C ±5%, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

(1) Inputs tested high, V_{CC} = volts dc, R_{CC} = Ω +5%, V_{IN} = volts dc, R_{IN} = Ω +20%, and all outputs are open.

(2) Inputs tested low V_{CC} = volts dc, R_{CC} = Ω +5%, V_{IN} = 0.0 V dc, and all outputs are open.

f. For device classes M, B, and S subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

Table IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023 or approved alternate	100%
Reverse bias burn-in	1015	100%
Burn-in parameters	1015, total of 240 hrs. at +125°C	100%
Radiographic	2012	100%

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.4 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.5 Pin descriptions.

Port 0 — Port 0 is an 8-bit, open drain, bi-directional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high impedance inputs. Port 0 is also the multiplexed low order address and data memory. In this application it uses strong internal pull-ups when emitting 1's, and can source and sink several LS TTL inputs.

6.5 Pin descriptions - continued.

Port 1 Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pull-ups, and in that state can be used as inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}), because of the internal pull-ups. In addition, Port 1 serves the functions of the following special features of the device:

Port pin	Alternate function
P1.0	T2(external count input to timer/counter 2).
P1.1	T2EX(timer/counter 2 capture/reload trigger and direction control).
P1.2	ECI(external count input to the PCA).
P1.3	CEX0(external I/O for compare/capture module 0).
P1.4	CEX1(external I/O for compare/capture module 1).
P1.5	CEX2(external I/O for compare/capture module 2).
P1.6	CEX3(external I/O for compare/capture module 3).
P1.7	CEX4(external I/O for compare/capture module 4).

Port 2 Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can drive LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups. Port 2 emits the high order address byte during fetches from external program memory and during accesses (MOVX @DPTR). In this application it uses strong internal pull-ups when emitting 1's. During accesses to external data memory that uses 8-bit addresses (MOVX @R1), Port 2 emits the contents of the P2 special function register.

Port 3 Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups. Port 3 serves the functions of various special features of the device as follows:

Port pin	Alternate function
P3.0	RXD (serial input port).
P3.1	TXD (serial output port).
P3.2	$\overline{INT0}$ (external interrupt 0).
P3.3	$\overline{INT1}$ (external interrupt 1).
P3.4	T0 (timer 0 external input).
P3.5	T1 (timer 1 external input).
P3.6	$\overline{WR}$ (external data memory write strobe).
P3.7	$\overline{RD}$ (external data memory read strobe).

RST Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits a power on reset with only a capacitor connected to V_{CC}.

6.5 Pin descriptions - continued.

ALE	Address latch enable output pulse for latching the low byte of the address during accesses to external memory. In normal operation ALE is emitted at a constant rate of 1/6th the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.
$\overline{PSEN}$	Program store enable is the read strobe to external program memory. When the device is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.
$\overline{EA}$	External access enable. $\overline{EA}$ must be strapped to V_{SS} in order to enable the device to fetch code from external program memory.
XTAL1	Input to the inverting oscillator amplifier.
XTAL2	Output from the inverting oscillator amplifier.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), who was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can procure to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.