

REVISIONS

LTR	DESCRIPTION										DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
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SHEET	15	16	17	18	19	20	21	22	23	24	25								
REV STATUS OF SHEETS				REV															
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13
PMIC N/A				PREPARED BY TUAN NGUYEN						DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444									
STANDARDIZED MILITARY DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A				CHECKED BY Jeff Bowling						MICROCIRCUIT, MEMORY, CMOS, 1K X 9 PARALLEL FIFO, MONOLITHIC SILICON									
				APPROVED BY Michael A. Frye															
				DRAWING APPROVAL DATE 93-10-08						SIZE A	CAGE CODE 67268	5962-91585							
				REVISION LEVEL						SHEET	1	OF	25						

DESC FORM 193
JUL 91

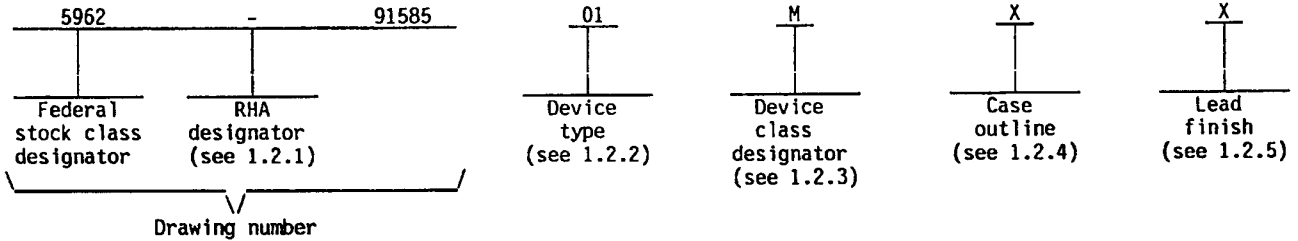
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5962-E569-92

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01		1K X 9 FIFO	120 ns
02		1K X 9 FIFO	80 ns
03		1K X 9 FIFO	65 ns
04		1K X 9 FIFO	50 ns
05		1K X 9 FIFO	40 ns
06		1K X 9 FIFO	30 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level (see 6.6 herein) as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDIP3-T28 or GDIP4-T28	28	Dual-in-line package
Y	CDIP2-T28 or GDIP1-T28	28	Dual-in-line package
Z	GDFP2-F28	28	Flat pack
U	CQCC1-N32	32	Rectangular chip carrier

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-BUL-103.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 2

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 2/

Supply voltage range to ground potential (V_{CC}) - - - - -	-0.5 V dc to +7.0 V dc
DC voltage range applied to Outputs in High Z state - -	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN}) - - - - -	-3.0 V dc to +7.0 V dc
DC output current - - - - -	20 mA
Maximum power dissipation - - - - -	1.0 W
Lead temperature (soldering, 10 seconds) - - - - -	+260°C
Thermal resistance, junction-to-case (θ_{JC}) - - - - -	See MIL-STD-1835
Junction temperature (T_J) - - - - -	+175°C
Storage temperature range (T_{STG}) - - - - -	-65°C to +150°C
Temperature under bias - - - - -	-55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) - - - - -	+4.5 V dc minimum to +5.5 V dc maximum
Ground voltage (GND) - - - - -	0 V dc
Input high voltage (V_{IH}) - - - - -	2.2 V dc minimum
Input low voltage (V_{IL}) - - - - -	0.8 V dc maximum
Case operating temperature range (T_C) - - - - -	-55°C to +125°C

1.5 Logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) - - - - - 3/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

- MIL-M-38510 - Microcircuits, General Specification for.
- MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

- MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
- MIL-STD-883 - Test Methods and Procedures for Microelectronics.
- MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

- MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
 3/ Values will be added when they become available.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 3

DESC FORM 193A
 JUL 91

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. This is a fully characterized military detail specification and is suitable for qualification of device classes B and S to the requirements of MIL-M-38510. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 4

DESC FORM 193A
JUL 91

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B or S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B or S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S and V. All device class S devices shall be serialized in accordance with MIL-M-38510. Class V shall be serialized in accordance with MIL-I-38535.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S

- a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.
- b. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 5

DESC FORM 193A
JUL 91

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output high voltage	V _{OH}	V _{CC} = 4.5 V, I _{OH} = -2.0 mA V _{IN} = V _{IH} (Min), V _{IL} (Max)	1, 2, 3	All	2.4		V
Output low voltage	V _{OL}	V _{CC} = 4.5 V, I _{OL} = 8.0 mA V _{IN} = V _{IH} (Min), V _{IL} (Max)	1, 2, 3	All		0.4	V
Input high voltage	V _{IH} ^{2/}		1, 2, 3	All	2.2		V
Input low voltage	V _{IL} ^{2/}		1, 2, 3	All		0.8	V
Input leakage current	I _{IX}	V _{IN} = 5.5 V to GND	1, 2, 3	All	-10	10	μA
Output leakage current	I _{OZ}	V _{CC} = 5.5 V, R = V _{IH} , V _{OUT} = 5.5 V and GND	1, 2, 3	All	-10	10	μA
Operating supply current	I _{CC1}	V _{CC} = 5.5 V, I _{OUT} = 0 mA f = 1/t _{RC} W, R, D ₀ - D ₈ pins are toggling between 0 V and 3 V FF, X _O /H _F = 0 mA Q ₀ - Q ₈ = 0 mA MR, FL/FT = 3.0 V	1, 2, 3	01-04		115	mA
				05		130	
				06		140	
Standby current	I _{CC2}	V _{CC} = 5.5 V, I _{OUT} = 0 mA All inputs = V _{IH} FF, X _O /H _F = 0 mA Q ₀ - Q ₈ = 0 mA	1, 2, 3	All		30	mA
Power down current	I _{CC3}	V _{CC} = 5.5 V, I _{OUT} = 0 mA All inputs = V _{CC} - 0.2 V FF, X _O /H _F = 0 mA Q ₀ - Q ₈ = 0 mA	1, 2, 3	All		25	mA
Input capacitance	C _{IN} ^{3/}	V _{CC} = 5.0 V, V _{IN} = 0 V T _A = +25°C, f = 1 MHz (see 4.4.1e)	4	All		8	pF
Output capacitance	C _{OUT} ^{3/}	V _{CC} = 5.0 V, V _{OUT} = 0 V T _A = +25°C, f = 1 MHz (see 4.4.1e)	4	All		12	pF

See footnotes at end of table.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 6

DESC FORM 193A
JUL 91

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Functional tests		See 4.4.1c	7,8A, 8B	All			
Read cycle time	t _{RC}	See figure 4	9, 10, 11	01	140		ns
				02	100		
				03	80		
				04	65		
				05	50		
				06	40		
Access time	t _A		9, 10, 11	01		120	ns
				02		80	
				03		65	
				04		50	
				05		40	
				06		30	
Read recovery time	t _{RR}		9, 10, 11	01,02	20		ns
				03,04	15		
				05,06	10		
Read pulse width ^{4/}	t _{PR}		9, 10, 11	01	120		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	30		
Read low to low Z ^{3/ 5/}	t _{LZR}		9, 10, 11	All	3		ns
Read high to data ^{6/} valid	t _{DVR}		9, 10, 11	All	3		ns
Read high to high Z ^{3/ 5/ 6/}	t _{HZR}		9, 10, 11	01		35	ns
				02-04		30	
				05		25	
				06		20	
Write cycle time	t _{WC}		9, 10, 11	01	140		ns
				02	100		
				03	80		
				04	65		
				05	50		
				06	40		
Write pulse width ^{4/}	t _{PW}		9, 10, 11	01	120		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	30		

See footnotes at end of table.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 7

DESC FORM 193A
JUL 91

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit	
					Min	Max		
Write high to low ^{3/ 5/ 7/} Z	t _{HWZ}	See figure 4	9, 10, 11	All	10		ns	
Write recovery time	t _{WR}				9, 10, 11		01,02	20
			03,04	15				
			05,06	10				
Data setup time	t _{SD}		9, 10, 11		01,02	40		ns
					03,04	30		
					05	20		
Data hold time	t _{HD}		9, 10, 11		06	18		ns
					01-03	10		
					04	5		
Master reset cycle time	t _{MRSC}		9, 10, 11		05,06	0		ns
					01	140		
					02	100		
					03	80		
		04			65			
		05			50			
Master reset pulse width ^{4/}	t _{PMR}	9, 10, 11		06	40		ns	
				01	120			
				02	80			
				03	65			
				04	50			
				05	40			
Master reset recovery time	t _{RMR}	9, 10, 11		01,02	20		ns	
				03,04	15			
				05,06	10			
Read high to master reset high ^{8/}	t _{RPW}	9, 10, 11		01	120		ns	
				02	80			
				03	65			
				04	50			
				05	40			
				06	30			
Write high to master reset high ^{8/}	t _{WPW}	9, 10, 11		01	120		ns	
				02	80			
				03	65			
				04	50			
				05	40			
				06	30			
Retransmit cycle time	t _{RTC}	9, 10, 11		01	140		ns	
				02	100			
				03	80			
				04	65			
				05	50			
				06	40			

See footnotes at end of table.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 8

DESC FORM 193A
JUL 91

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Retransmit pulse width ^{4/}	t _{PRT}	See figure 4	9, 10, 11	01	120		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	30		
Retransmit recovery time	t _{RTR}		9, 10, 11	01,02	20		ns
				03,04	15		
				05,06	10		
Master reset to empty flag low	t _{EFL}		9, 10, 11	01		140	ns
				02		100	
				03		80	
				04		65	
				05		50	
				06		40	
Master reset to half- full flag high	t _{HFH}		9, 10, 11	01		140	ns
				02		100	
				03		80	
				04		65	
				05		50	
				06		40	
Master reset to full flag high	t _{FFH}		9, 10, 11	01		140	ns
				02		100	
				03		80	
				04		65	
				05		50	
				06		40	
Read low to empty flag low	t _{REF}		9, 10, 11	01-03		60	ns
				04		45	
				05		35	
				06		30	
Read high to full flag high	t _{RFF}		9, 10, 11	01-03		60	ns
				04		45	
				05		35	
				06		30	
Write high to empty flag high	t _{WEF}		9, 10, 11	01-03		60	ns
				04		45	
				05		35	
				06		30	
Write low to full flag low	t _{WFF}		9, 10, 11	01-03		60	ns
				04		45	
				05		35	
				06		30	

See footnotes at end of table.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 9

DESC FORM 193A
 JUL 91

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Write low to half-full flag low	t _{WHF}	See figure 4	9, 10, 11	01		140	ns
				02		100	
				03		80	
				04		65	
				05		50	
				06		40	
Read high to half-full flag high	t _{RHF}		9, 10, 11	01		140	ns
				02		100	
				03		80	
				04		65	
				05		50	
				06		40	
Effective read pulse width after empty flag high	t _{RPE}		9, 10, 11	01	120		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	30		
Effective write pulse width after full flag high	t _{WPF}		9, 10, 11	01	120		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	30		
Expansion out low delay from clock	t _{XOL}		9, 10, 11	01		120	ns
				02		80	
				03		65	
				04		50	
				05		40	
				06		30	
Expansion out high delay from clock	t _{XOH}		9, 10, 11	01		120	ns
				02		80	
				03		65	
				04		50	
				05		40	
				06		30	

- 1/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load in figure 3, circuit A, unless otherwise specified.
- 2/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
- 3/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
- 4/ Pulse widths less than minimum are not allowed.
- 5/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input.
- 6/ Use output load figure 3 (circuit B).
- 7/ Only applies to read data flow-through mode.
- 8/ If not tested, these parameter limits shall be guaranteed by design.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 10

DESC FORM 193A
JUL 91

Device types	All	
Case outlines	X,Y,Z	U
Terminal number	Terminal symbol	
1	\overline{W}	NC
2	D ₈	\overline{W}
3	D ₃	D ₈
4	D ₂	D ₃
5	D ₁	D ₂
6	D ₀	D ₁
7	\overline{XI}	D ₀
8	\overline{FF}	\overline{XI}
9	Q ₀	\overline{FF}
10	Q ₁	Q ₀
11	Q ₂	Q ₁
12	Q ₃	NC
13	Q ₈	Q ₂
14	GND	Q ₃
15	R	Q ₈
16	Q ₄	GND
17	Q ₅	NC
18	Q ₆	R
19	Q ₇	Q ₄
20	$\overline{XO}/\overline{HF}$	Q ₅
21	\overline{EF}	Q ₆
22	\overline{MR}	Q ₇
23	$\overline{FL}/\overline{RT}$	$\overline{XO}/\overline{HF}$
24	D ₇	\overline{EF}
25	D ₆	\overline{MR}
26	D ₅	$\overline{FL}/\overline{RT}$
27	D ₄	NC
28	V _{CC}	D ₇
29	---	D ₆
30	---	D ₅
31	---	D ₄
32	---	V _{CC}

NC = no connection

FIGURE 1. Terminal connections.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 11

DESC FORM 193A
JUL 91

Reset and retransmit
Single device configuration/width expansion mode

Mode	Inputs			Internal status		Outputs		
	\overline{MR}	\overline{RT}	\overline{XI}	Read pointer	Write pointer	\overline{EF}	\overline{FF}	\overline{HF}
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment $\frac{1}{2}$	Increment $\frac{1}{2}$	X	X	X

$\frac{1}{2}$ Pointer will increment if flag is high.

Reset and first load truth table
Depth expansion/compound expansion mode

Mode	Inputs			Internal status		Outputs	
	\overline{MR}	\overline{FL}	\overline{XI}	Read pointer	Write pointer	\overline{EF}	\overline{FF}
Reset first device	0	0	$\frac{1}{2}$	Location zero	Location zero	0	1
Reset all other devices	0	1	$\frac{1}{2}$	Location zero	Location zero	0	1
Read/Write	1	X	$\frac{1}{2}$	X	X	X	X

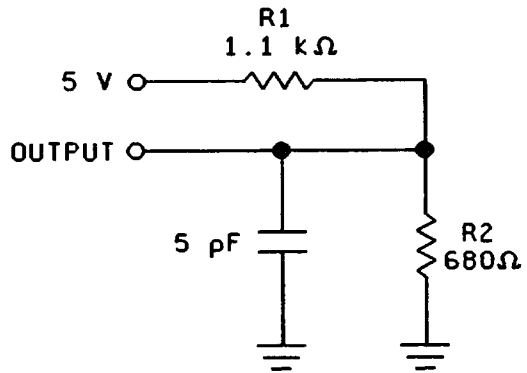
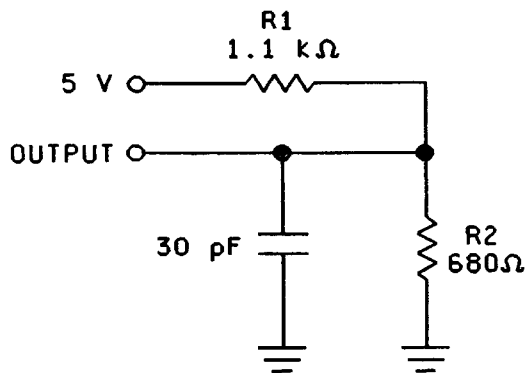
$\frac{1}{2}$ \overline{XI} is connected to $\overline{X0}$ of previous device.

NOTE: \overline{MR} = Reset input, $\overline{FL}/\overline{RT}$ = First load/retransmit \overline{EF} = Empty flag output,
 \overline{FF} = Full flag output, \overline{XI} = Expansion input, and \overline{HF} = Half-full flag output
 0 = Low level voltage
 1 = High level voltage
 X = Don't care

FIGURE 2. Truth tables.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 12

DESC FORM 193A
JUL 91



Circuit A
Output load

Circuit B
Output load

NOTE: Including scope and jig. (minimum values)

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall times	≤ 5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 3. Output load circuit and test conditions.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 13

DESC FORM 193A
JUL 91

Asynchronous read and write timing diagram

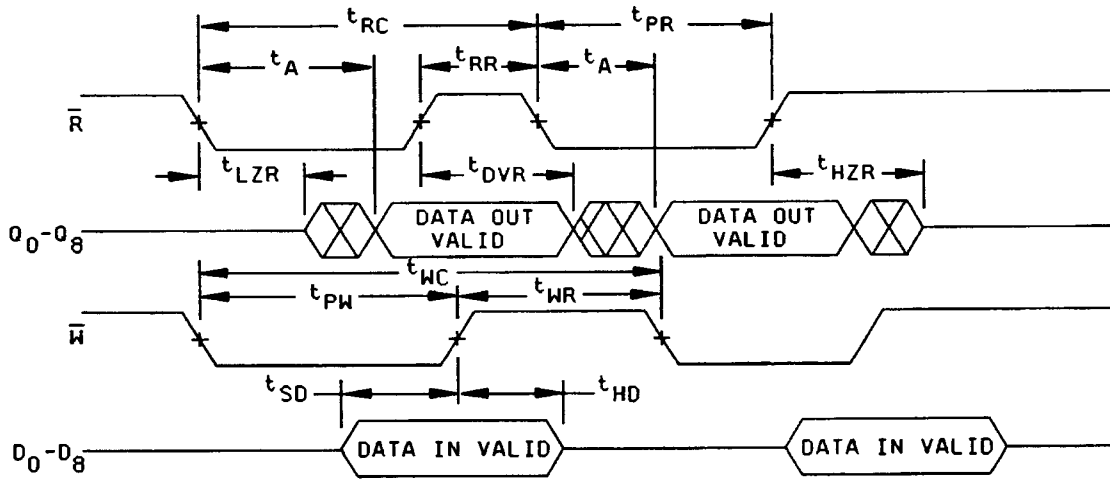
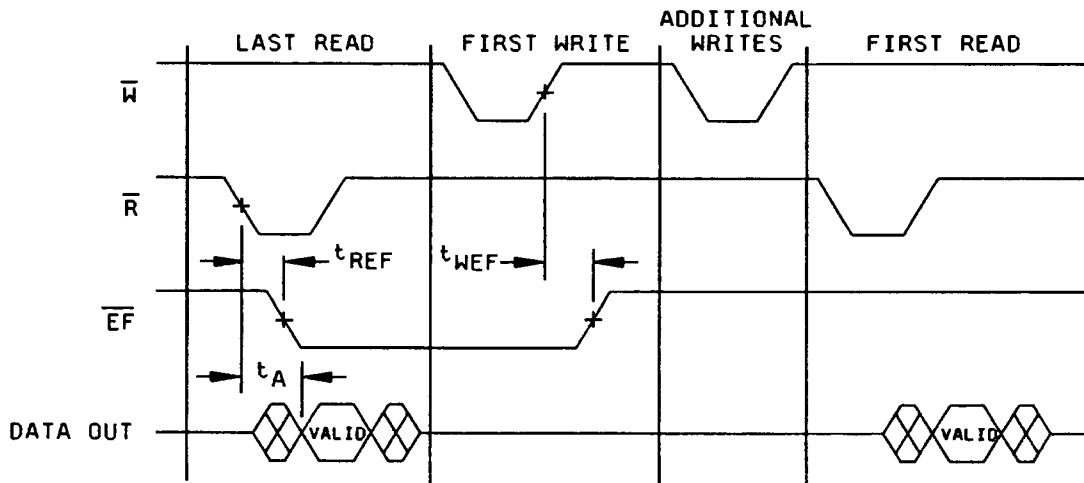


FIGURE 4. Timing waveforms.

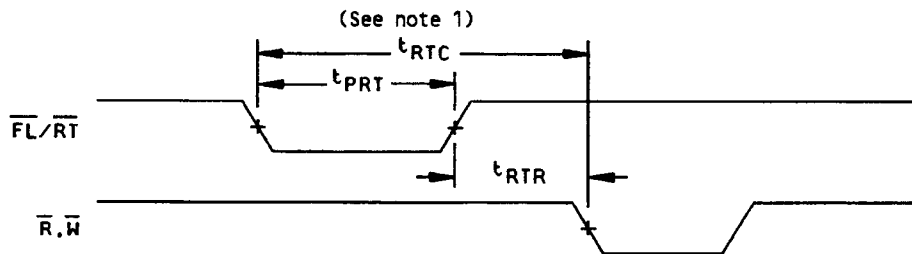
STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 14

DESC FORM 193A
 JUL 91

Last read to first write empty flag timing diagram



Retransmit timing diagram (See note 2)



NOTES:

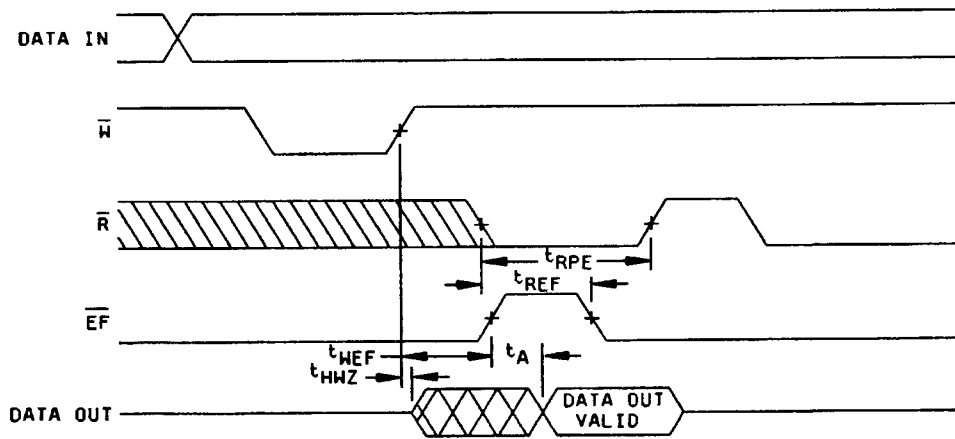
1. $t_{RTC} = t_{PRT} + t_{RTR}$.
2. \overline{EF} , \overline{HF} and \overline{FF} may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC} .

FIGURE 4. Timing waveforms - Continued.

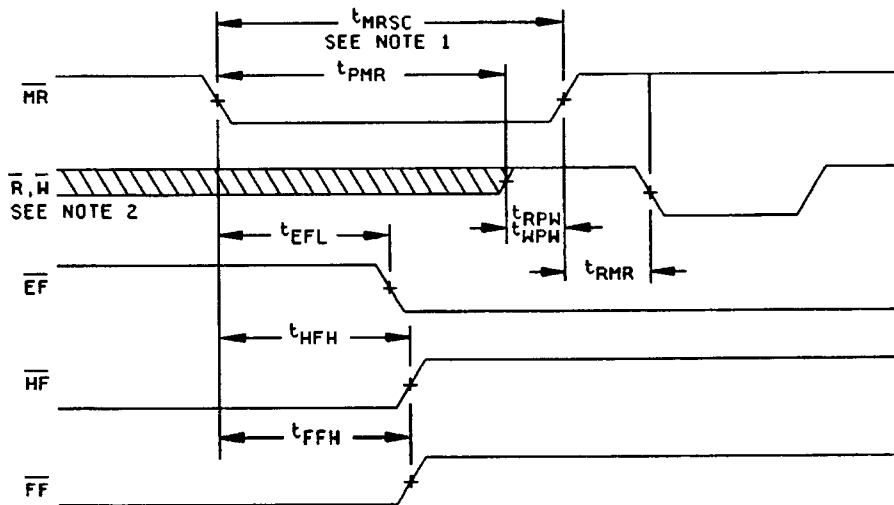
STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 15

DESC FORM 193A
 JUL 91

Empty flag and read bubble-through mode timing diagram



Master reset timing diagram



NOTES:

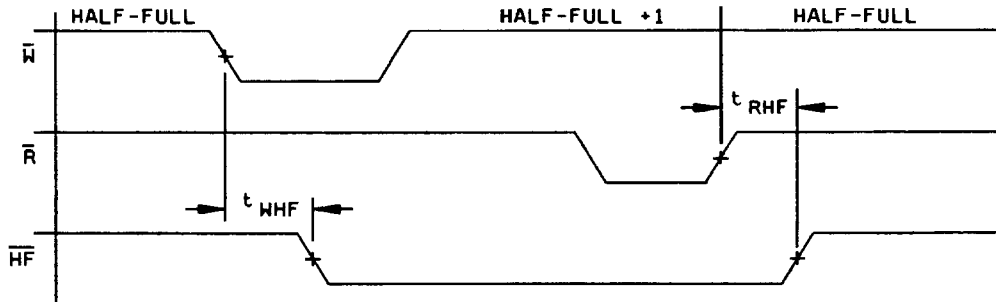
1. $t_{MRSC} = t_{PMR} + t_{RMR}$.
2. \bar{W} and $\bar{R} = V_{IH}$ around the rising edge of \bar{MR} .

FIGURE 4. Timing waveforms - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 16

DESC FORM 193A
 JUL 91

Half-full flag timing diagram



Last write to first read full flag timing diagram

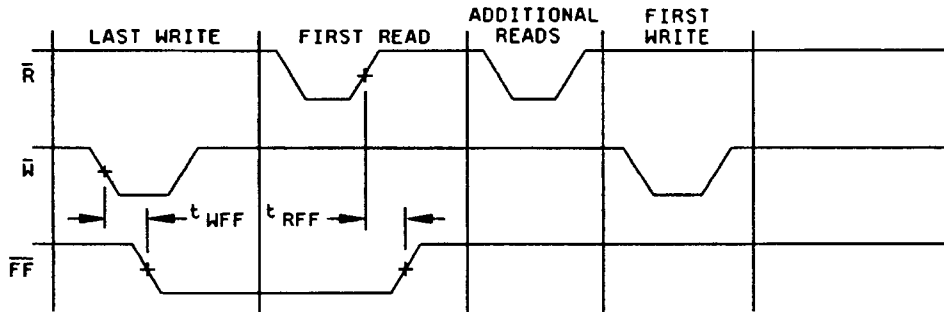


FIGURE 4. Timing waveforms - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 17

DESC FORM 193A
 JUL 91

Full flag and write bubble-through mode timing diagram

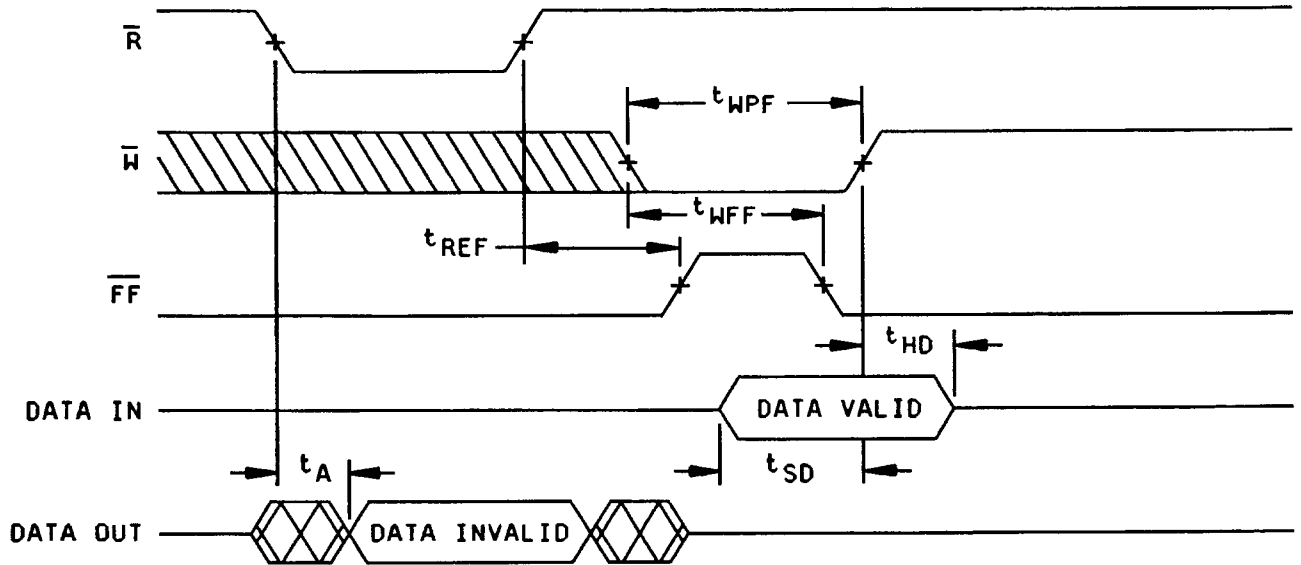
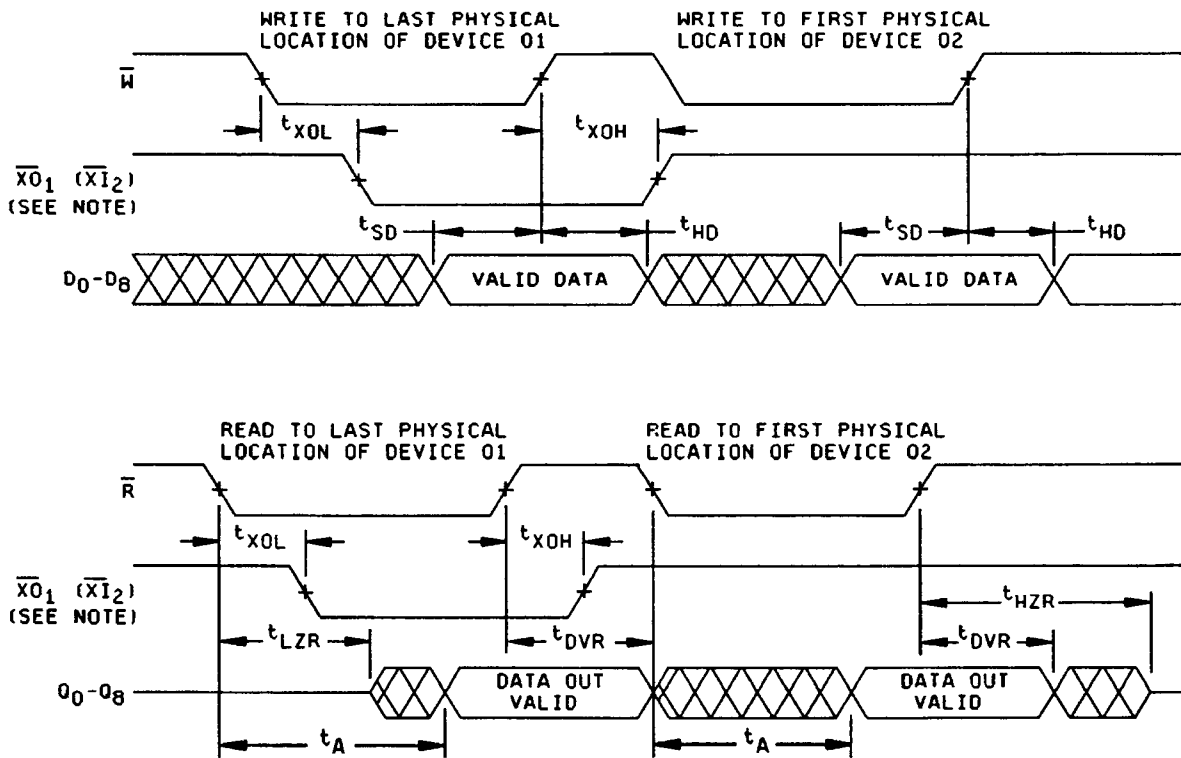


FIGURE 4. Timing waveforms - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 18

DESC FORM 193A
 JUL 91

Expansion timing diagrams



NOTE: Expansion out of device 1 (\overline{XO}_1) is connected to expansion in of device 2 (\overline{XI}_2)

FIGURE 4. Timing waveforms - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A	5962-91585
		REVISION LEVEL SHEET 19

DESC FORM 193A
 JUL 91

4.2.1 Additional criteria for device classes M, B, and S - Continued.

- (1) Static burn-in for device class S (method 1015 of MIL-STD-883, test condition A).
 - (a) All inputs shall be connected to GND. Outputs may be open or connected to 4.5 V minimum. Resistors R1 are optional on both inputs and outputs, and required on outputs connected to $V_{CC} \pm 0.5$ V. $R1 = 220\Omega$ to 47 k Ω . For static II burn-in, reverse all input connections (i.e., V_{SS} to V_{CC}).
 - (b) $V_{CC} = 4.5$ V minimum.
 - (c) Ambient temperature (T_A) shall be +125°C minimum.
 - (d) Test duration for the static test shall be 48 hours minimum. The 48 hour burn-in shall be broken into two sequences of 24 hours each (static I and static II) followed by interim electrical measurements.
 - (2) Dynamic burn-in for device classes M, B, and S (method 1015 of MIL-STD-883, test condition D, for circuit see 4.2.1b herein).
- c. Interim and final electrical parameters shall be as specified in table IIA herein.
- d. For classes S and B devices, post dynamic burn-in electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.2.3 Percent defective allowable (PDA).

- a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.
- b. The PDA for class B devices shall be in accordance with MIL-M-38510 for dynamic burn-in.
- c. Static burn-in I and II failures shall be cumulative for determining PDA.
- d. Those devices whose measured characteristics, after burn-in, exceed the specified delta (Δ) limits or electrical parameter limits specified in table I, subgroup 1, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.
- e. The PDA for device classes Q and V shall be in accordance with MIL-I-38535 for dynamic burn-in.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Qualifying data for subgroups 7, 8A, and 8B shall be attributes only.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 20

DESC FORM 193A
JUL 91

4.3.1.1 Qualification extension for device classes B and S. When authorized by the qualifying activity, if a manufacturer qualifies one device type which is identical (i.e., same die) to other device types on this specification, the slower device types may be part I qualified, upon the request of the manufacturer, without any further testing. The faster device types may be part I qualified by performing only group A qualification testing.

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. For device class M subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes B and S subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).
- d. 0/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes B and S, the procedures and circuits shall be maintained under document revision control by the manufacturer and shall be made available to the qualifying activity upon request. For device classes Q and V, the procedures and circuits shall be shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on 5 devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC standard number 17 may be used for reference.
- e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

- a. For device class S, steady-state life test circuits shall be conducted using test condition D and the circuit described in 4.2.1b herein, or equivalent as approved by the qualifying activity.
- b. For device class S only, end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 5 of group B inspections and shall consist of tests specified in table IIB herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 21

DESC FORM 193A
JUL 91

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005 table I)			Subgroups (in accordance with MIL-I-38535, table III)	
		Device class M	Device class B	Device class S	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9	1,7,9	1,7,9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required	Not required	Required
3	Same as line 1			1*,7* Δ		1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required	Required	Required
5	Same as line 1			1*,7* Δ		1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9 10,11	1*,2,3,7*, 8A,8B,9 10,11	1*,2,3,7*, 8A,8B,9 10,11	1*,2,3,7*, 8A,8B,9 10,11	1*,2,3,7*, 8A,8B,9 10,11
7	Group A test requirements	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11
8	Group B end-point electrical parameters			1,2,3,7, 8A,8B,9, 10,11 Δ		
9	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B Δ		1,2,3,7, 8A,8B Δ	1,2,3,7, 8A,8B,9, 10,11 Δ
10	Group D end-point electrical parameters	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7, 8A,8B
11	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

- 1/ Blank spaces indicate tests are not applicable.
- 2/ Any or all subgroups may be combined when using high-speed testers.
- 3/ Subgroups 7 and 8 functional tests shall verify the truth table.
- 4/ * indicates PDA applies to subgroup 1 and 7.
- 5/ ** see 4.4.1e.
- 6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
- 7/ See 4.4.1d

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 22

DESC FORM 193A
JUL 91

TABLE IIB. Delta limits at +25°C.

Parameter ^{1/}	Device types
	All
I _{CC2} standby	±10% of specified value in table I
I _{IX} , I _{OZ}	±10% of specified value in table I

^{1/} The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.
- b. T_A = +125°C, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.4 Group D inspection. For group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B and S shall be M, D, R, and H and for device class M shall be M and D.

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device classes B, S, Q, and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, and 9.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 23

DESC FORM 193A
 JUL 91

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

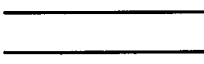
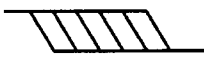

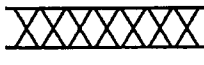
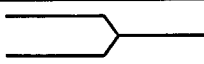
- C_{IN} - - - - - Input terminal capacitance.
- C_{OUT} - - - - - Output and bidirectional output terminal capacitance.
- GND - - - - - Ground zero voltage potential.
- I_{CC} - - - - - Supply current.
- I_{IX} - - - - - Input current.
- I_{OZ} - - - - - Output current.
- T_C - - - - - Case temperature.
- V_{CC} - - - - - Positive supply voltage.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 24

DESC FORM 193A
JUL 91

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN'S. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

<u>Military documentation format</u>	<u>Example PIN under new system</u>	<u>Manufacturing source listing</u>	<u>Document listing</u>
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91585
		REVISION LEVEL	SHEET 25

DESC FORM 193A
JUL 91