Data Sheet
September 1999

microelectronics group

Lucent Technologies
Bell Labs Innovations

W3011
1 GHz Quadrature Modulator

Features

- Guaranteed performance at 2.7 V power supply
- Output power of 3 dBm into 50 Ω load (single-ended) with 3 V operation
- Direct RF modulation with or without offset mixer
- Automatic power control (APC) capability
- Accurate 90° phase shifter for carrier
- Double-balanced active mixers minimize carrier feedthrough (origin offset)
- Low-current sleep mode

Applications

- PDC 800 and American digital cellular mobile terminals
- Cellular base stations

Description

The W3011 1 GHz Quadrature Modulator is a monolithic integrated circuit that provides direct modulation of an RF carrier by I & Q baseband inputs. It is particularly suited for use in mobile and handheld cellular telephones designed to the IS-136 (North American 824 MHz to 849 MHz), PDC (Japan RCR-STD27 889 MHz to 958 MHz), and other digital personal-communications standards.

The circuit block diagram is shown in Figure 1. From two LO signals, LOL and LOH, the offset mixer produces an internal LO signal, which prevents the external VCOs from being pulled by the large transmitted signal. The phase shifter splits the LO signal into two carriers with 90° phase separation and equal amplitude.

These signals are fed to the in-phase (I) and quadrature-phase (Q) double-balanced mixers. The resulting signals are summed and fed into the output amplifier. This amplifier can provide 0 dBm linear output power, minimum, into a 50 Ω load.

The output power can be attenuated up to 50 dB by applying a control voltage to the APC input. Nominally, the output power is at maximum (+3 dBm) with V_{APC} > 2.2 V, and at minimum (–50 dBm) with V_{APC} < 0.8 V.

A CMOS/TTL-compatible logic input allows the device to be put into a powerdown mode in which less than 10 µA of supply current is consumed.

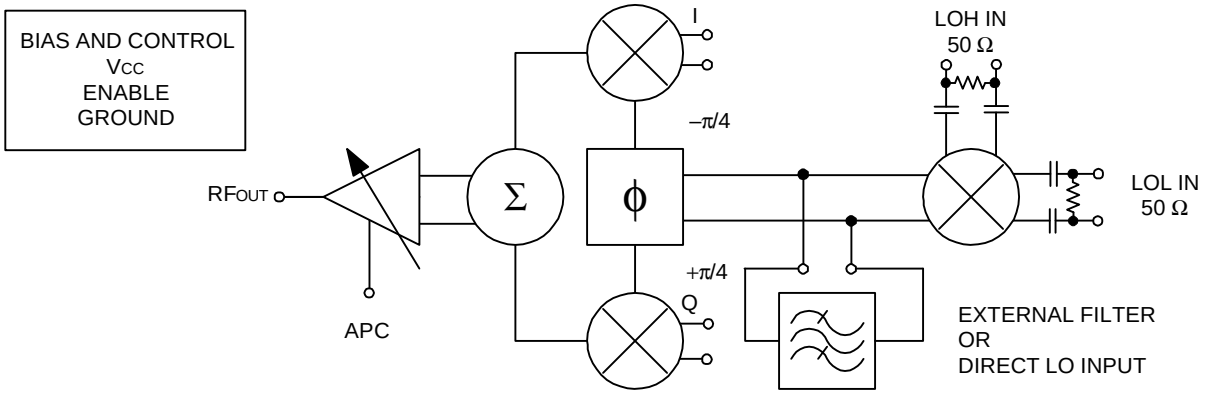


Figure 1. Circuit Block Diagram

Pin Information

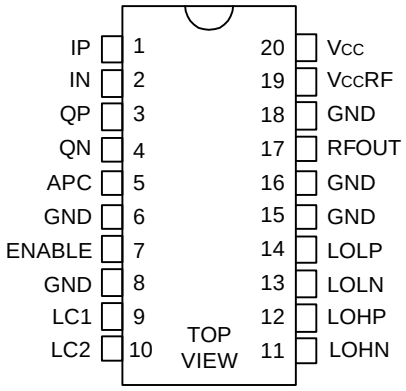


Figure 2. Pin Configuration

Table 1. Pin Descriptions

Pin	Name	Function
1	IP	Differential Baseband Input (in-phase)
2	IN	Differential Baseband Input (in-phase)
3	QP	Differential Baseband Input (quad-phase)
4	QN	Differential Baseband Input (quad-phase)
5	APC	Automatic Power Control dc Input
6	GND	dc Ground
7	ENABLE	Logic Enable
8	GND	dc Ground
9	LC1	Differential LO Input/External Filter
10	LC2	Differential LO Input/External Filter
11	LOHN	Differential High-frequency Local Oscillator Input
12	LOHP	Differential High-frequency Local Oscillator Input
13	LOLN	Differential Low-frequency Local Oscillator Input
14	LOLP	Differential Low-frequency Local Oscillator Input
15	GND	dc Ground
16	GND	dc Ground
17	RF_{OUT}	Open-collector RF Output
18	GND	dc Ground
19	$V_{CC}RF$	Positive Power Supply for RF Output Stage
20	V_{CC}	Positive Power Supply (nonoutput circuits)

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only, as shown in Table 2. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Ambient Operating Temperature	T_A	–35	85	°C
Storage Temperature	T_{stg}	–65	150	°C
Lead Temperature (soldering, 10 s)	—	—	300	°C
Positive Supply Voltage	V_{CC}	–0.3	4.5	V
Power Dissipation	P_D	—	650	mW
ac p-p Input Voltage	Vp-p	–0.3	V_{CC}	V
Digital Voltages	—	–0.3	V_{CC}	V

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent Technologies Microelectronics Group employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters:

ESD Threshold Voltage	
Model	**Rating**
HBM	2000
CDM (corner pins) CDM (noncorner pins)	500 500

Operating Ranges

The W3011 operating ranges are shown in Table 3. Performance is not guaranteed over the full range of all conditions possible within this table. However, the table lists the ranges of external conditions in which the W3011 provides general functionality, which may be useful in specific applications, without risk of permanent damage. The conditions for guaranteed performance are described in Tables 4 and 5.

Table 3. Operating Ranges

Parameter	Min	Max	Unit
V_{CC}	2.7	3.6	Vdc
Ambient Operating Temperature	–35	85	°C
f_{LO} Direct Mode (pins 9 and 10)	800	1000	MHz
P_{LO} Direct Mode (pins 9 and 10)	110	600	mVp-p
Offset Local Oscillator (LOL) Frequency	50	800	MHz
LOL Input Level	–15	–3	dBm
UHF Local Oscillator (LOH) Frequency	100	1300	MHz
LOH Input Level	–15	–3	dBm
External dc Bias Voltage for I & Q Inputs with 0.282 Vrms ac Input Level: Differential ac Input	1.2	V_{CC} – 0.7	Vdc

Electrical Characteristics

Table 4. dc and Digital Electrical Specifications

Conditions unless otherwise noted: 2.7 ≤ V_{CC} ≤ 3.3 Vdc; T_A = 25 °C ± 3 °C; RL = 50 Ω, VAPC = 2.7 Vdc; f_{RF} = 900 MHz, f_{LOL} = 130 MHz, f_{LOH} = 1030 MHz, –13 dBm < P_{LOL}, P_{LOH} < –5 dBm; I – $\overline{I}$ = 0.4 cos(2πt • 80 kHz), Q – $\overline{Q}$ = 0.4 cos(2πt • 80 kHz – π/2), Vbias of I, $\overline{I}$, Q, and $\overline{Q}$ = 1.22 Vdc.

Parameter	Symbol	Min	Typ	Max	Unit
Enable Input					
Logic High Voltage	V_{IH}	0.7 V_{CC}	—	V_{CC} + 0.4	V
Logic Low Voltage	V_{IL}	GND – 0.4	—	0.3 V_{CC}	V
Logic High Current (V_{IH} = 3.3 V)	I_{IH}	—	—	10	µA
Logic Low Current (V_{IL} = 0.4 V)	I_{IL}	—	—	10	µA
Powerup/down (after ENABLE change)	—	—	—	4	µs
Power Supply Current					
Powerdown (ENB = 0)	I_{PDN}	—	0.3	50	µA
Transmit (ENB = V_{CC}): (offset mixer on, APC @ max power) (offset mixer off, APC @ max power)	 I_{CC}(on) I_{CC}(on)	 — —	 52 50	 66 64	 mA mA
Transmit (ENB = V_{CC}): (offset mixer on, APC @ P_{OUT} < P_{MAX} – 10 dB) (offset mixer off, APC @ P_{OUT} < P_{MAX} – 10 dB)	 — —	 — —	 46 43	 — —	 mA mA

Electrical Characteristics (continued)

Table 5. ac Specifications

Conditions unless otherwise noted: 2.7 ≤ V_{CC} ≤ 3.3 Vdc; T_A = 25 °C ± 3 °C; RL = 50 Ω, VAPC = 2.7 Vdc; f_{RF} = 900 MHz, f_{LOL} = 130 MHz, f_{LOH} = 1030 MHz, –15 dBm < P_{LOL}, P_{LOH} < –5 dBm; I – $\overline{I}$ = 0.4 cos(2πt • 80 kHz), Q – $\overline{Q}$ = 0.4 cos(2πt • 80 kHz – π/2), Vbias of I, $\overline{I}$, Q, and $\overline{Q}$ = 1.22 Vdc.

Parameter	Min	Typ	Max	Unit
I & Q				
I & Q Signal Path 0.5 dB Bandwidth	—	5	—	MHz
I & Q Input Resistance	—	200	—	kΩ
I & Q Input Capacitance to Ground	—	5	—	pF
I & Q Input Differential Signal for Max Output	—	0.8	—	Vp-p
Offset Mixer				
LOL Input Impedance	—	50	—	Ω
LOH Input Impedance	—	50	—	Ω
LO Input Impedance (pins LC1, LC2)	—	480//1	—	Ω//pF
LOL Input IP3	—	10	—	dBm
Modulation Accuracy (P_{OUT} = –1 dBm)				
Carrier Suppression (P_{OUT} = –1 dBm)	—	–35	–28	dBUSB
Carrier Suppression (entire usable APC range)	—	—	–26	dBUSB
Origin Offset (DQPSK inputs, all usable APC levels)	—	—	–23	dBc
Error Vector Magnitude (See Explanation of Error Vector Magnitude (EVM) Testing section.)	—	2.5	5	%
Lower Sideband (LSB) Suppression (See Figure 3.)	—	–43	–34	dBUSB
RF Output				
Output Power (0.8 Vp-p differential or single-ended 80 kHz sine-wave inputs to I and Q, with 90° between I and Q)	–1	3	—	dBm
Adjacent Channel Suppression (0.282 Vrms differential I and Q inputs, π/4 – DQPSK modulation, random data):				
Per PDC (RCR STD-27):				
±50 kHz, All Usable APC Levels	—	–65	–55	dBc
±100 kHz, All Usable APC Levels	—	—	–62	dBc
±100 kHz, Max RF Output (APC > 2.2)	—	–75	–65	dBc
Per IS-136/IS-137 800 MHz Digital Mode:				
±30 kHz, All Usable APC Levels	—	–45	–36	dBc
±60 kHz, All Usable APC Levels	—	–60	–50	dBc
Noise Floor Suppression, F_C ± >100 kHz	—	–120	–112	dBc/Hz
APC (Automatic Power Control) Function				
Range of Usable Output Power Control for Japan PDC (RCR STD-27), from Max Power at APC = 2.7 V to Minimum APC Voltage Where Requirements for ACP and Carrier Suppression Are Still Met Using π/4 – DQPSK/α = 0.5 Modulation at 0.282 Vrms Differential I and Q Inputs:				
Offset Mixer Not Used	29	40	—	dB
Offset Mixer Used	39	45	—	dB
Output Power Variation Due to Temperature, within Usable Control Range	—	4	6	dB
RF Power Change Time (after APC change)	—	—	2	µs
APC Voltage for Max Output Power	—	2.2	—	Vdc
APC Voltage for Min Output Power	—	0.8	—	Vdc

Explanation of Error Vector Magnitude (EVM) Testing

Error vector magnitude (EVM) is estimated by feeding signals to the W3011 as described above in Table 5. A typical narrowband, sine-wave modulation output spectrum appears in Figure 3.

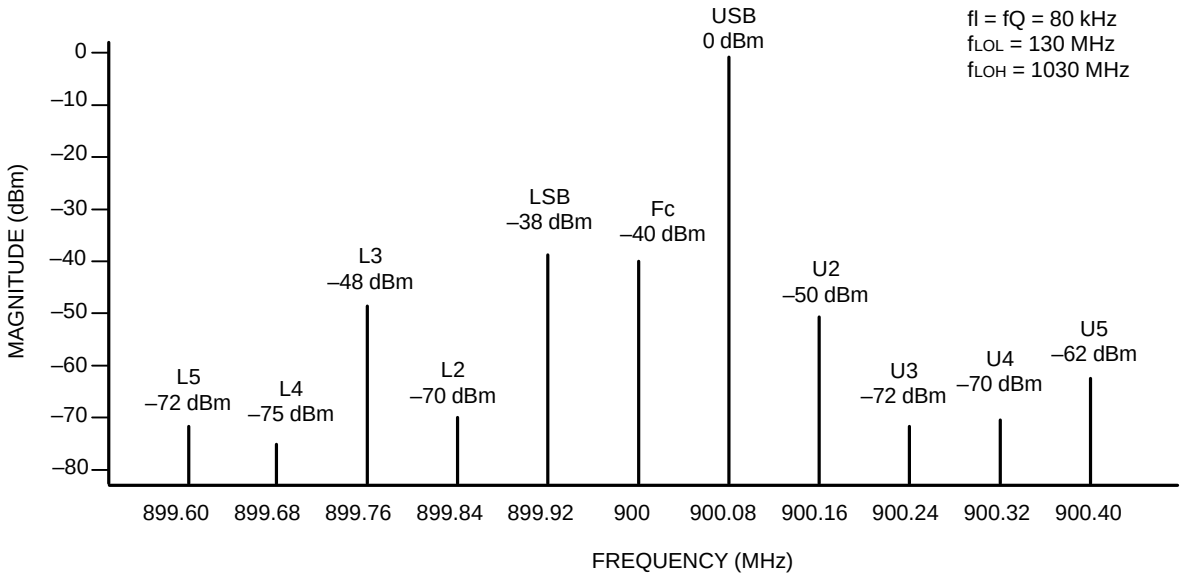


Figure 3. W3011 Sine-Wave Modulation Output Spectrum

Data from this spectrum is used to estimate EVM by the formula:

$$EVM\ (\%) = 100 \bullet [10^{P(L5)/20} + 10^{P(L4)/20} + 10^{P(L3)/20} + 10^{P(L2)/20} + 10^{P(LSB)/20} + 10^{P(U2)/20} + 10^{P(U3)/20} + 10^{P(U4)/20} + 10^{P(U5)/20}]/10^{P(USB)/20}$$

The data presented in the spectrum above would yield:

$$EVM\ (\%) = 100 \bullet [251e{-}6 + 178e{-}6 + 3981e{-}6 + 316e{-}6 + 12589e{-}6 + 3162e{-}6 + 251e{-}6 + 316e{-}6 + 794e{-}6]/1000e{-}3$$

$$= 2.18\%$$

This approximates worst-case digital modulation results, because the sine-wave modulation estimate assumes all spurious outputs are in phase and adds their magnitudes as scalars. In addition, this estimate includes full-amplitude measurements of spurious peaks that would appear in adjacent and alternate channels, where a receiver would otherwise provide attenuation. The L3 third-order intermodulation peak and LSB (lower sideband) are normally the unwanted output frequencies that dominate the EVM estimate.

RFOUT Matching: Basic Open Collector Termination

The W3011 RF output uses an open collector output architecture. To operate properly, this requires that dc bias current be provided through the output pin (pin 17). Thus, the output matching network must always provide a shunt dc connection to the positive power supply. Examples of such a connection include a shunt-matching inductor or a shunt RF choke. Figure 4 illustrates a simple RFOUT matching configuration.

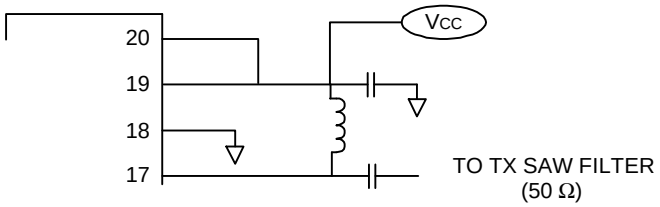


Figure 4. W3011 RF Output Diagram

Offset Mixer

W3011 with Offset Mixer Disabled

If the offset mixer in the W3011 is not required for the frequency plan, the offset mixer may be turned off by connecting the positive supply (VCC) to any or all of pins 11 (LOHN), 12 (LOHP), 13 (LOLN), or 14 (LOLP), as illustrated in Figure 5 below. Disabling the offset mixer reduces current consumption 2 mA to 3 mA. If pin 11 is connected to VCC, pins 12, 13, and 14 must be connected to VCC or no-connect (NC). Connect the RF VCO to either pin 9 or pin 10 through a low-impedance coupling capacitor, and connect the unused pin (10 or 9) through a similar capacitor to ground.

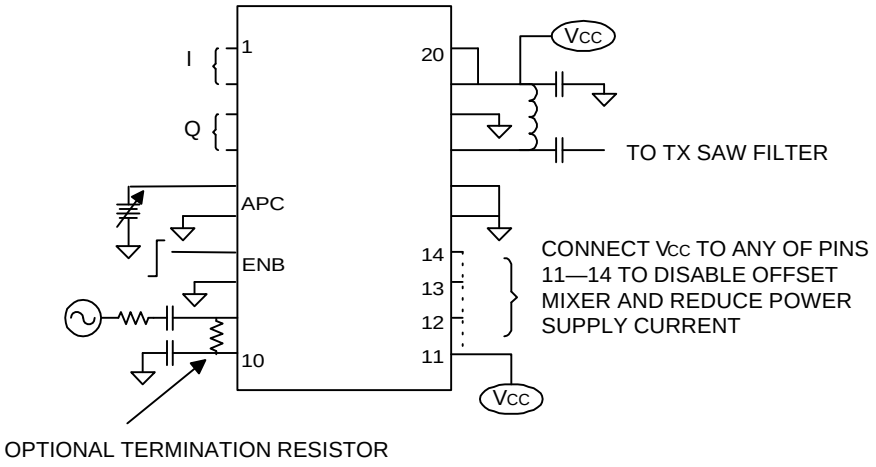


Figure 5. W3011 Application with Offset Mixer Disabled

Offset Mixer (continued)

W3011 Using Offset Mixer

If the W3011 offset mixer is required, two VCOs must be connected (see Figure 6). A low-frequency (VHF) oscillator may be dc-coupled to either pin 13 (LOLN) or pin 14 (LOLP) if the VCO contains a dc-blocking capacitor at its output. Otherwise, use a low-impedance series capacitor between the VCO output and the LOL input. The other LOL pin must be dc-grounded (no external capacitor for the grounded pin). As shown in Figure 1, there is a 50 Ω termination resistor on chip, connected between pins 13 and 14.

In the same way, as shown in Figure 6, one of the pins 11 (LOHN) or 12 (LOHP) must be connected to dc ground. The other pin is connected to a high-frequency (UHF) VCO, using either dc coupling (if the VCO contains a dc-blocking capacitor at its output) or a low-impedance series-coupling capacitor. There is also a 50 Ω termination resistor on chip connected between pins 11 and 12.

When the offset mixer is used, it is necessary to filter the offset mixer output signal with a parallel-tuned LC filter between pins 9 and 10. The resonant frequency of this filter should be approximately the center of the transmit RF band (for example, about 920 MHz for PDC 800). The filter should be adjusted for lowest EVM at RFOUT.

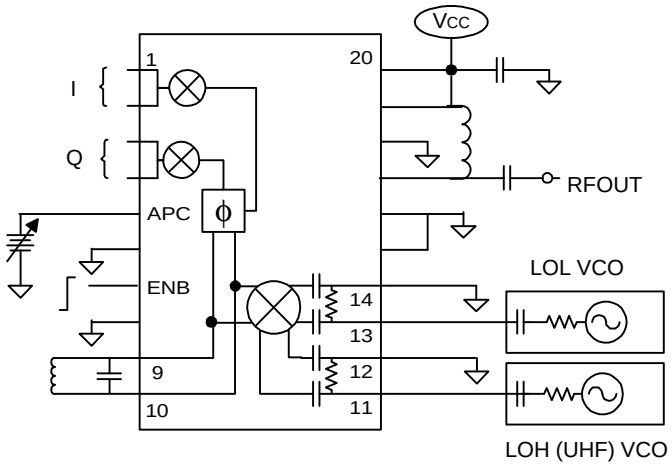


Figure 6. W3011 Application Using Offset Mixer

Characteristic Curves

Conditions unless otherwise noted: V_{CC} = 2.7; T_A = 25 °C ± 3 °C; LOH = 755 MHz @ –12.5 dBm, LOL = 185 MHz @ –12.5 dBm; I/Q= 0.8 Vp-p π/4 – DQPSK; α = 0.5 (random data); I/Q Vcm = 1.22 Vdc; LC filter = 10 nH//2.2 pF; RFOUT = 940 MHz.

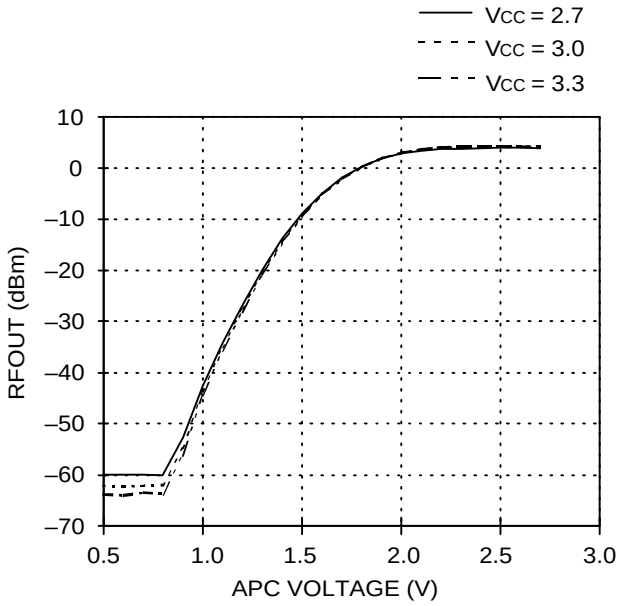


Figure 7. Output Power vs. APC and Supply Voltage

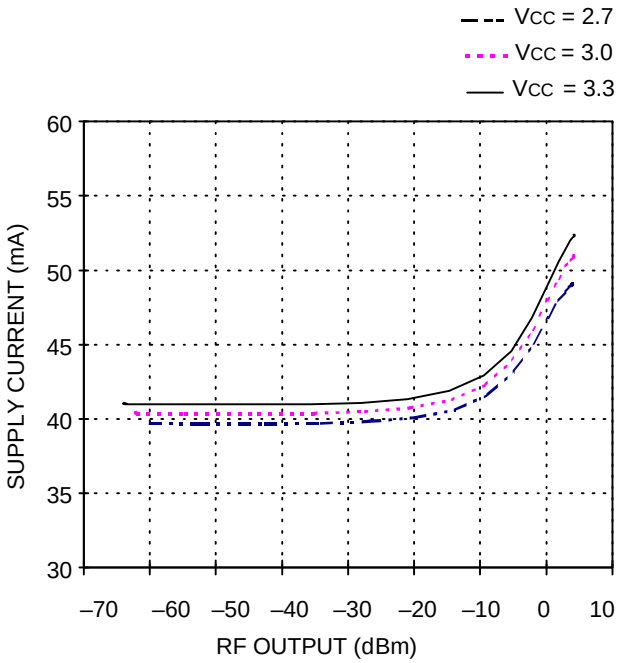


Figure 9. Supply Current vs. Output Power

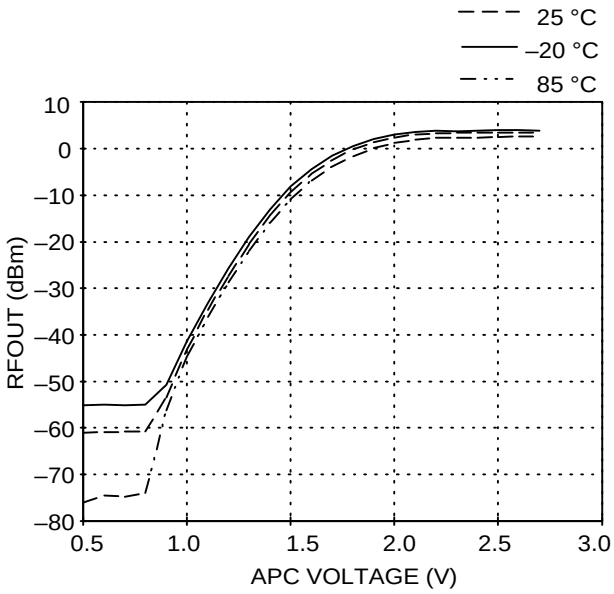


Figure 8. Output Power vs. APC Voltage and Temperature

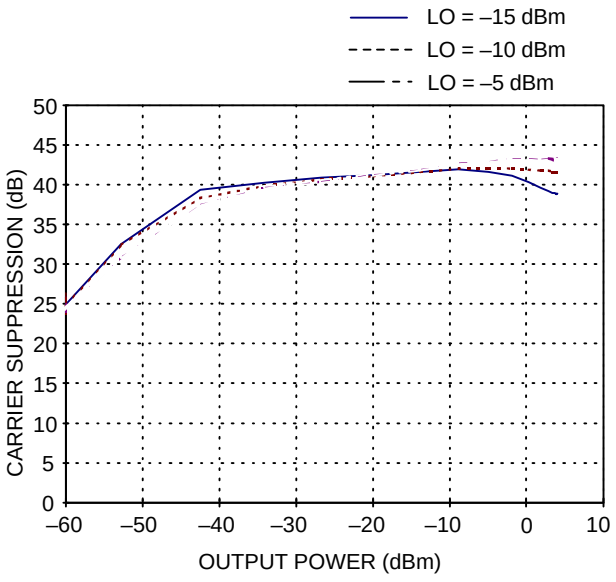


Figure 10. Carrier Suppression vs. Output Power and LO Level

Characteristic Curves (continued)

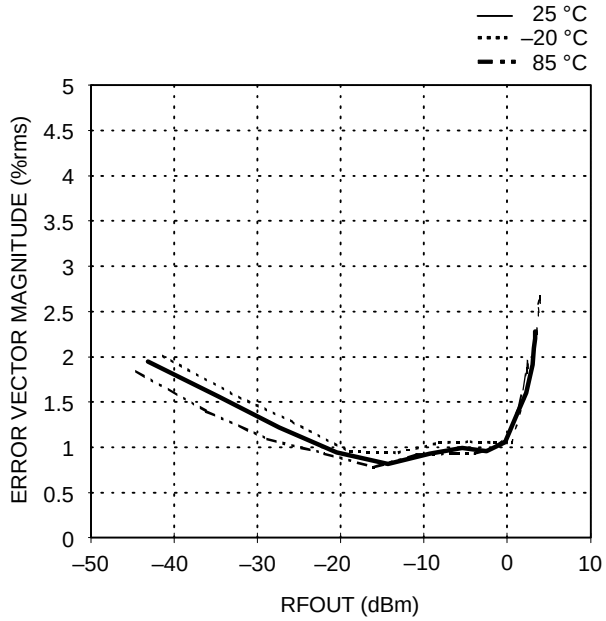


Figure 11. EVM vs. Output Power and Temperature

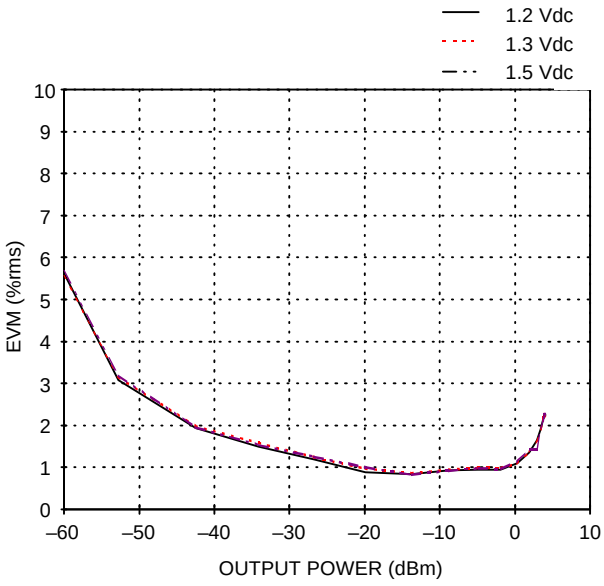


Figure 12. EVM vs. Output Power and I/Q Common-Mode Voltage

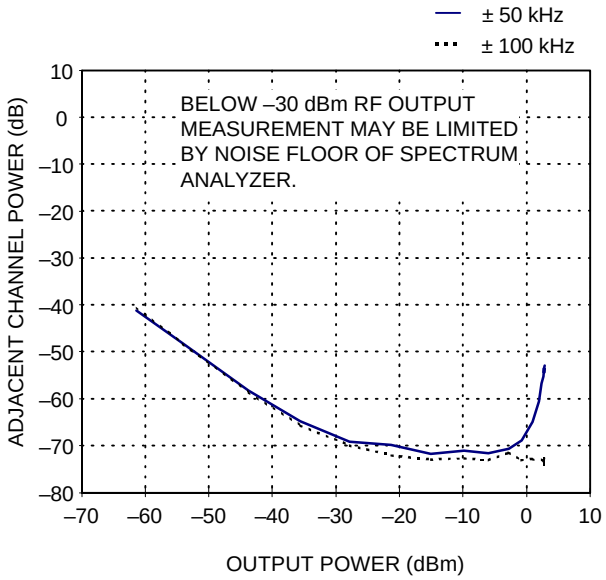
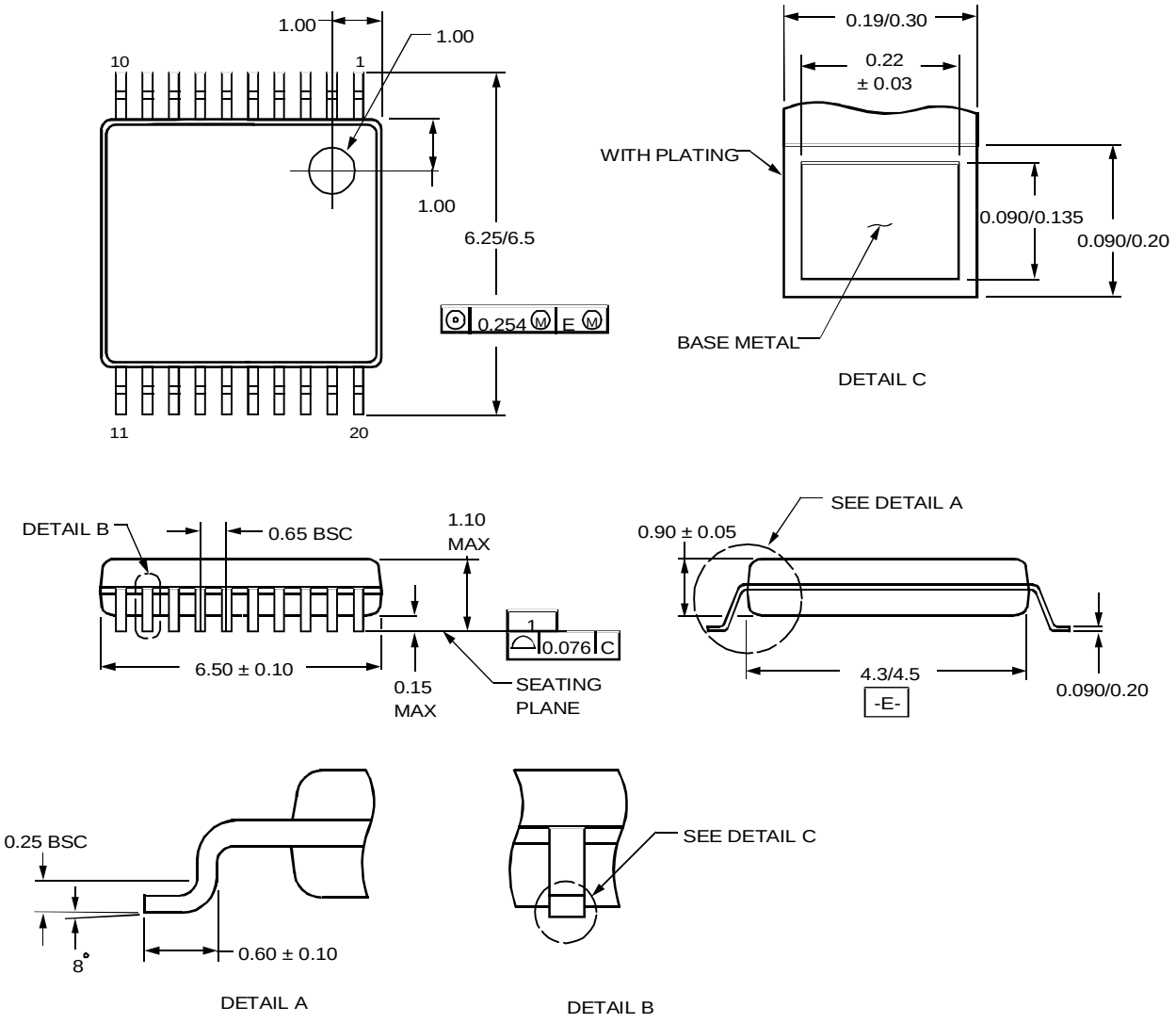


Figure 13. Adjacent Channel Power Suppression for PDC

Package Outline

20-Pin TSSOP

Dimensions are in millimeters.



Manufacturing Information

This device may be assembled in any of the following locations: assembly codes P, M, or T.

Ordering Information

Device Code	Description	Package	Comcode
LUCW3011FCL	1 GHz Quadrature Modulator	20-pin TSSOP	108 131 400
LUCW3011FCL-TR*	1 GHz Quadrature Modulator	20-pin TSSOP, tape and reel	108 131 426
EVB3011	Evaluation Board	—	108 131 913

* Contact your Lucent Technologies Microelectronics Group Account Manager for minimum order requirements.

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