



LC33832P, S, M, PL, SL, ML-70/80/10

256 K (32768 words × 8 bits) Pseudo-SRAM

Overview

The LC33832 series is composed of pseudo static RAM that operates on a single 5 V power supply and is organized as 32768 words × 8 bits. By using memory cells each composed of a single transistor and capacitor, together with peripheral CMOS circuitry, this series achieves ease of use with high density, high speed, and low power dissipation. The LC33832 series can easily accomplish auto-refresh and self-refresh by means of OE/RFSH input. As with asynchronous static RAM, WE input uses a system for incorporating input data at the WE rise, thereby facilitating interfacing with a microcomputer.

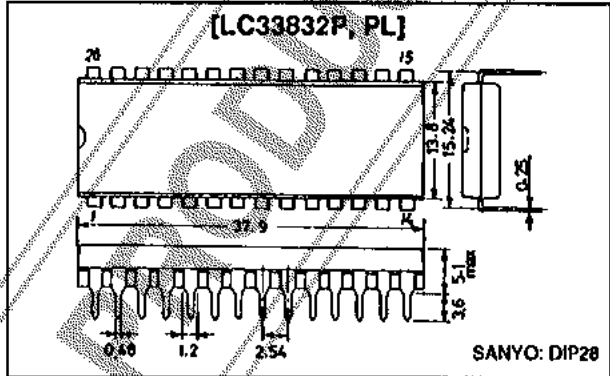
The LC33832 series features pin compatibility with 256 K static RAM (the LC36256A series), and available packages are the standard 28-pin DIP with widths of 600 mil or 300 mil, and the SOP with a width of 450 mil.

CE-only refresh can be accomplished by selecting address 256 (A0 to A7) within 4 ms.

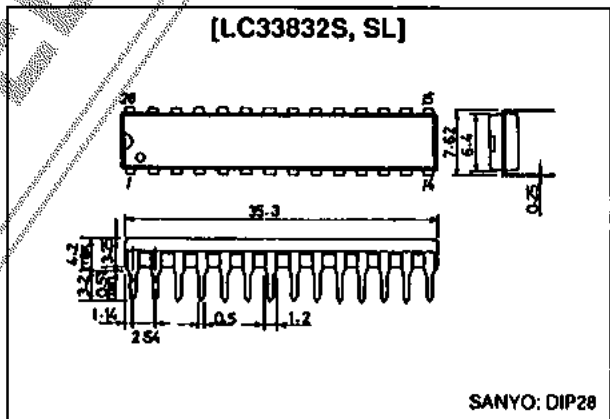
Package Dimensions

unit : mm

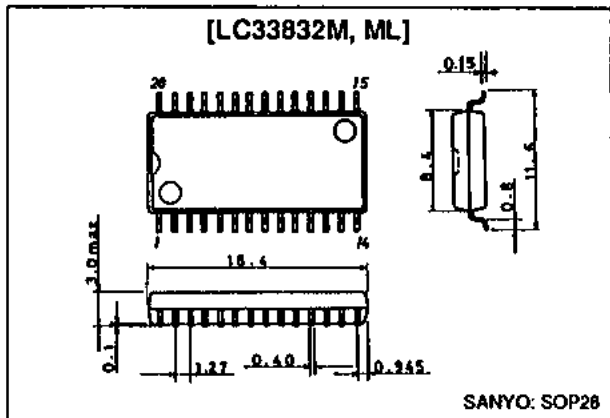
3012A-DIP28



3123-DIP28



3158-SOP28



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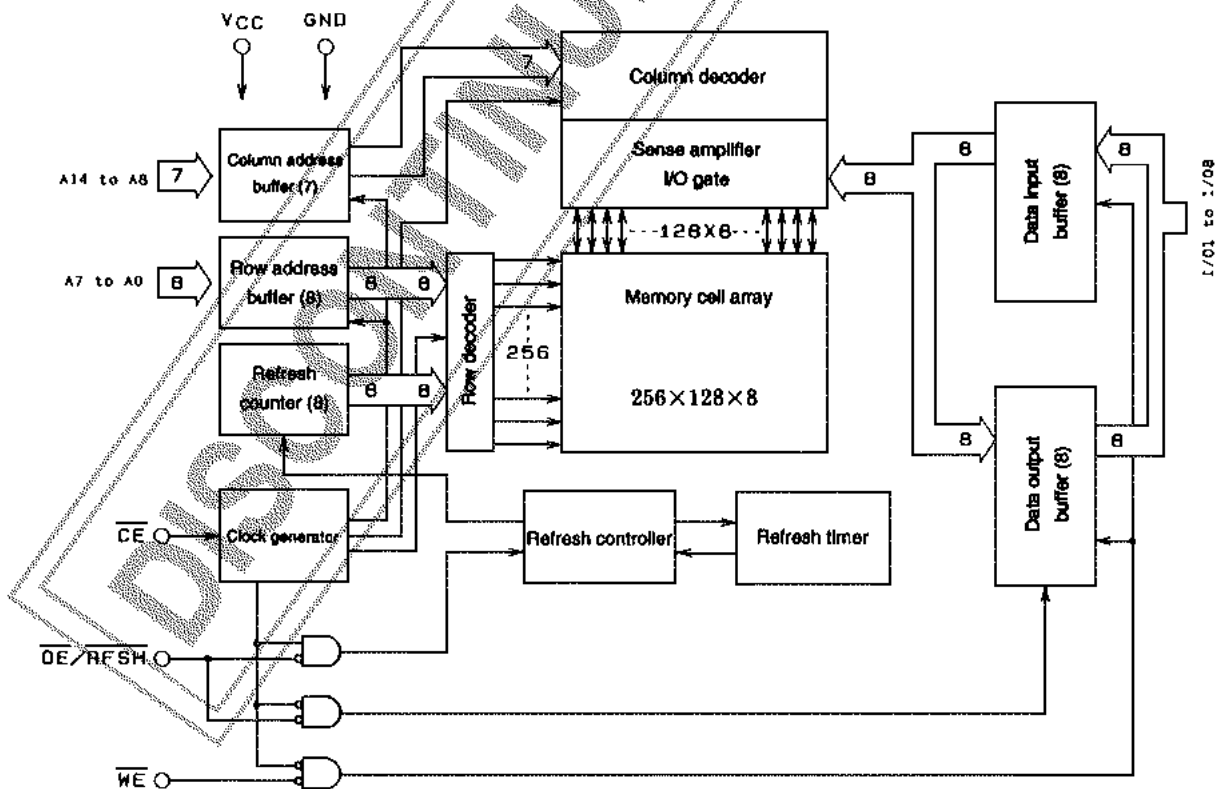
Features

- 32768 words x 8 bits configuration.

Parameter		LC33832P, S, M, PL, SL, ML		
		-70	-80	-10
CE Access Time		70ns	80ns	100ns
OE Access Time		30ns	35ns	40ns
Cycle Time		115ns	130ns	160ns
Current Drain	Operating	65mA	60mA	50mA
	Standby	1mA/100µA (L version)		

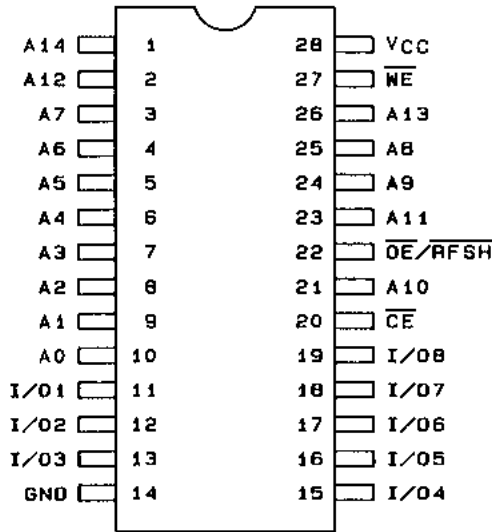
- Single 5 V ±10% power supply
- All input and output (I/O) TTL compatible
- Fast access times and low power dissipation
- 4 ms refresh using 256 refresh cycle
- CE-only refresh, auto-refresh, and self-refresh
- Low-power version: 100µA self-refresh current
- Standard 28-pin plastic package

Block Diagram



Pin Assignment

DIP28, DIP28 (slim), SOP28



A0 to A14	Address input
\overline{WE}	Read/Write input
$\overline{OE/RFSH}$	Output-enable input/refresh input
\overline{CE}	Chip-enable input
I/O1 to I/O8	Data input/output
V _{CC}	Power supply
GND	Ground

Top View

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Functional Logic

\overline{CE}	$\overline{OE/RFSH}$	\overline{WE}	A0 to 7	A8 to 14	I/O1 to 8	State
H	H	X	X	X	HZ	Standby
L	L	H	VX	VX	OUT	Read
L	H	L	VX	VX	IN	Write
L	H	H	VX	X	HZ	\overline{CE} -only refresh
H	L	X	X	X	HZ	Self-refresh
H	NP	X	X	X	HZ	Auto-refresh

- HHigh-level input of $V_{IN} = 6.5\text{ V to }V_{IH}(\text{min})$
- LLow-level input of $V_{IN} = V_{IL}(\text{max}) \text{ to } -1.0\text{ V}$
- X.....High- or low-level input
- NP.....Negative-polarity pulse input
- VX....."IN" when $\overline{CE} = L$ is confirmed, then "X"
- HZ.....High impedance
- IN.....Input state
- OUT.....Output state

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Maximum supply voltage	V_{CC} max	-1.0 to +7.0	V	1
Input voltage	V_{IN}	-1.0 to +7.0	V	1
Output voltage	V_{OUT}	-1.0 to +7.0	V	1
Allowable power dissipation	P_d max	600	mW	1
Output short-circuit current	I_{OUT}	50	mA	1
Operating temperature range	T_{opr}	0 to +70	°C	1
Storage temperature range	T_{stg}	-55 to +150	°C	1

Note: 1) Stresses greater than the above listed maximum values may result in damage to the device.

DC Recommended Operating Ranges at $T_a = 0$ to +70°C

Parameter	Symbol	min	typ	max	Unit	Note
Power supply voltage	V_{CC}	4.5	5.0	5.5	V	2
Input high level voltage	V_{IH}	2.4		6.5	V	2
Input low level voltage	V_{IL}	-1.0		+0.8	V	2

Note: 2) All voltages are referenced to GND.

DC Electrical Characteristics at $T_a = 0$ to +70°C, $V_{CC} = 5V \pm 10\%$

Parameter	Symbol	Conditions	min	max	Unit	Note	
Operating current	I_{CCA}	Average current during operation	cycle time	115ns	65	mA	3,4
				130ns	60		
				160ns	50		
Standby current 1	I_{CCS1}	$\overline{CE} = \overline{OE}/RFSH = V_{IH}$		1	mA		
Standby current 2	I_{CCS2}	$\overline{CE} = \overline{OE}/RFSH = V_{CC} - 0.2V$	LC33832P, S, M	1	mA		
			LC33832PL, SL, ML	100	μA		
Self-refresh current	I_{CCSR}	$\overline{CE} = V_{CC} - 0.2V, \overline{OE}/RFSH = 0.2V$	LC33832P, S, M	1	mA		
			LC33832PL, SL, ML	100	μA		
Input leakage current	I_{IL}	$0V \leq V_{IH} \leq V_{CC}$, pins other than measuring pin = 0V	-10	+10	μA		
Output leakage current	I_{OL}	Output disable, $0V \leq V_{OUT} \leq V_{CC}$	-10	+10	μA		
Output high level voltage	V_{OH}	$I_{OUT} = -5mA$	2.4		V		
Output low level voltage	V_{OL}	$I_{OUT} = 4.2mA$		0.4	V		

Notes: 3) All current values are measured at minimal cycle rate. Since current flows inmoderately, cycle times may become longer and shorter than shown here.

4) Dependent on output load. Maximum value is value during free state.

Capacitance Characteristics at $V_{CC} = 5V \pm 10\%$, $f = 1MHz$, $T_a = 25^\circ C$

Symbol	Parameter	min	max	unit	Measuring conditions
C_{IN1}	Input capacitance (A_0 to A_{14})		5	pF	$V_{IN1} = 0V$
C_{IN2}	Input capacitance ($\overline{CE}, \overline{OE}/RFSH, \overline{WE}$)		7	pF	$V_{IN2} = 0V$
$C_{I/O}$	I/O capacitance		10	pF	$V_{I/O} = 0V$

Sampling inspections, and not full-lot inspections, are carried out for these parameters.

Recommended AC Operating Ranges at $V_{CC} 5V \pm 10\%$, $T_a = 0$ to $+70^\circ\text{C}$ (Notes 5, 6, 7, 8, 9)

Parameter	Symbol	-70		-80		-10		unit	note
		min	max	min	max	min	max		
Random Read and Write Cycle Time	t_{RC}	115		130		160		ns	
Read-Write Cycle Time	t_{RMW}	165		195		240		ns	
\overline{CE} Pulse Width	t_{CE}	70	10000	80	10000	100	10000	ns	
\overline{CE} Precharge Time	t_p	35		40		50		ns	
\overline{CE} Access Time	t_{CEA}		70		80		100	ns	
\overline{OE} Access Time	t_{OEA}		30		35		40	ns	
\overline{CE} Output Enable Time	t_{CLZ}	10		10		10		ns	
\overline{OE} Output Enable Time	t_{OLZ}	0		0		0		ns	
\overline{WE} Output Enable Time	t_{WLZ}	0		0		0		ns	
\overline{CE} Output Disable Time	t_{CHZ}	0	20	0	25	0	30	ns	10
\overline{OE} Output Disable Time	t_{OHZ}	0	20	0	25	0	30	ns	10
\overline{WE} Output Disable Time	t_{WHZ}	0	20	0	25	0	30	ns	10
\overline{OE} Hold Time for \overline{CE}	t_{OHC}	0		0		0		ns	
\overline{OE} Setup Time for \overline{CE}	t_{OSC}	10		10		10		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time	t_{RCH}	0		0		0		ns	
Write Pulse Width	t_{WP}	55		60		70		ns	
Write Command Hold Time	t_{WCH}	55		60		70		ns	
Write Command Lead Time	t_{CWL}	55		60		70		ns	
Input Data Setup Time for \overline{WE}	t_{DSW}	30		35		40		ns	11
Input Data Setup Time for \overline{CE}	t_{DSC}	30		35		40		ns	11
Input Data Hold Time for \overline{WE}	t_{DHW}	0		0		0		ns	11
Input Data Hold Time for \overline{CE}	t_{DHC}	0		0		0		ns	11
Address Setup Time for \overline{CE}	t_{ASC}	0		0		0		ns	12
Address Hold Time for \overline{CE}	t_{AHC}	15		20		25		ns	12
Auto-Refresh Cycle Time	t_{FC}	115		130		160		ns	
RFSH Delay Time for \overline{CE}	t_{RFD}	35		40		50		ns	
RFSH Pulse Width (Auto-Refresh)	t_{FAP}	75	8000	80	8000	80	8000	ns	13
RFSH Precharge Time (Auto-Refresh)	t_{FP}	30		30		30		ns	13
RFSH Active \overline{CE} Delay Time (Auto-Refresh)	t_{FCE}	135		160		190		ns	13
RFSH Pulse Width (Self-Refresh)	t_{FAS}	8000		8000		8000		ns	13
RFSH Precharge \overline{CE} Delay Time (Self-Refresh)	t_{FRS}	135		160		190		ns	13
Refresh Time	t_{REF}		4		4		4	ms	
Rise and Fall Time	t_T	3	50	3	50	3	50	ns	

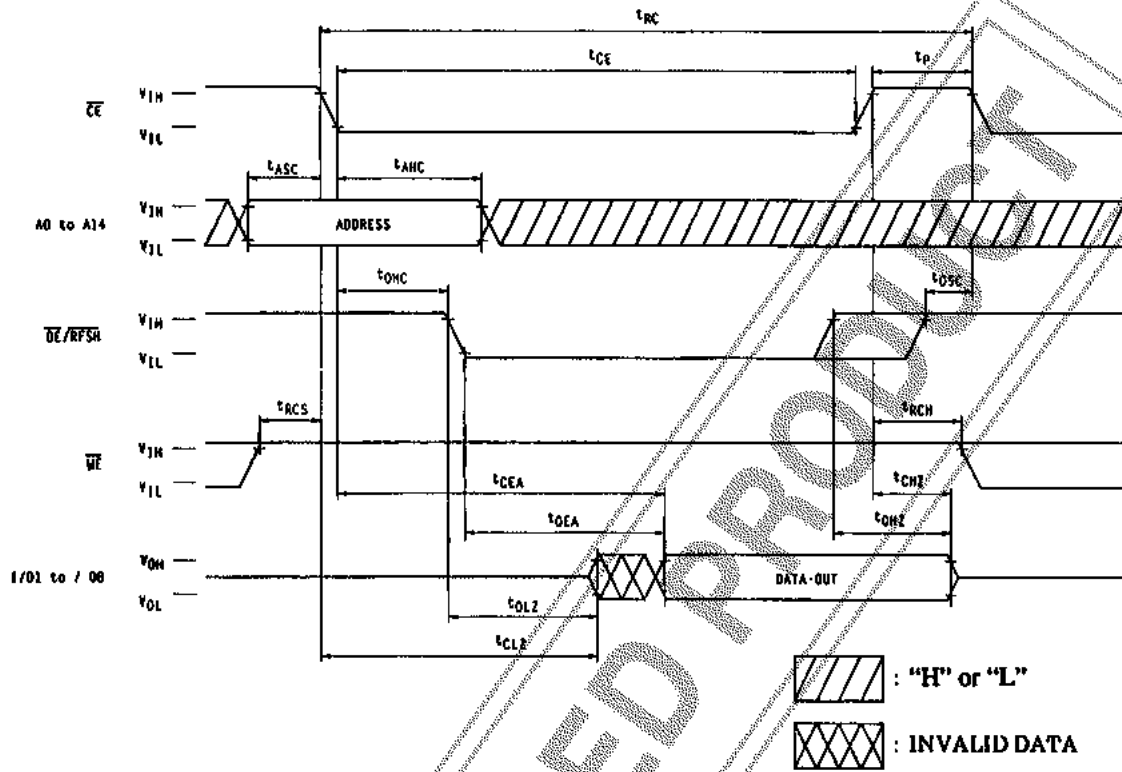
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- Notes : 5) To accomplish internal initialization, \overline{CE} and $\overline{OE/RFSH}$ are fixed at V_{IH} for an interval of 1 ms when V_{CC} reaches the specified voltage after power is switched on.
- 6) Measured at $t_T = 5$ ns.
- 7) When measuring input signal timing, V_{IH} (min) and V_{IL} (max) are reference levels.
- 8) Measured using an equivalent of 100 pF and two standard TTL loads.
- 9) $\overline{OE/RFSH}$ input functions as output-enable input (\overline{OE}) when $\overline{CE} = V_{IL}$, and as refresh input (\overline{RFSH}) when $\overline{CE} = V_{IH}$.
- 10) t_{CHZ} , t_{OHZ} , and t_{WHZ} are defined as the time until output enters the open circuit state and the output voltage level becomes immeasurable.
- 11) As with ordinary static RAM, write data is incorporated at the rise of \overline{WE} input or \overline{CE} input, whichever is earlier, and write data is therefore held during t_{DSW} , t_{DSC} , t_{DHW} , or t_{DHC} .
- 12) Because address input is incorporated at the fall of \overline{CE} , the address is maintained during t_{ASC} or t_{AHC} .
- 13) Auto-refresh and self-refresh are determined by $\overline{OE/RFSH}$ pulse width when $\overline{CE} = V_{IH}$, and are defined as auto-refresh when below t_{FAP} (max), or as self-refresh when above t_{FAS} (min). In order to activate \overline{CE} after the completion of each refresh, t_{FCE} must be assured for auto-refresh, or t_{FRS} must be assured for self-refresh.

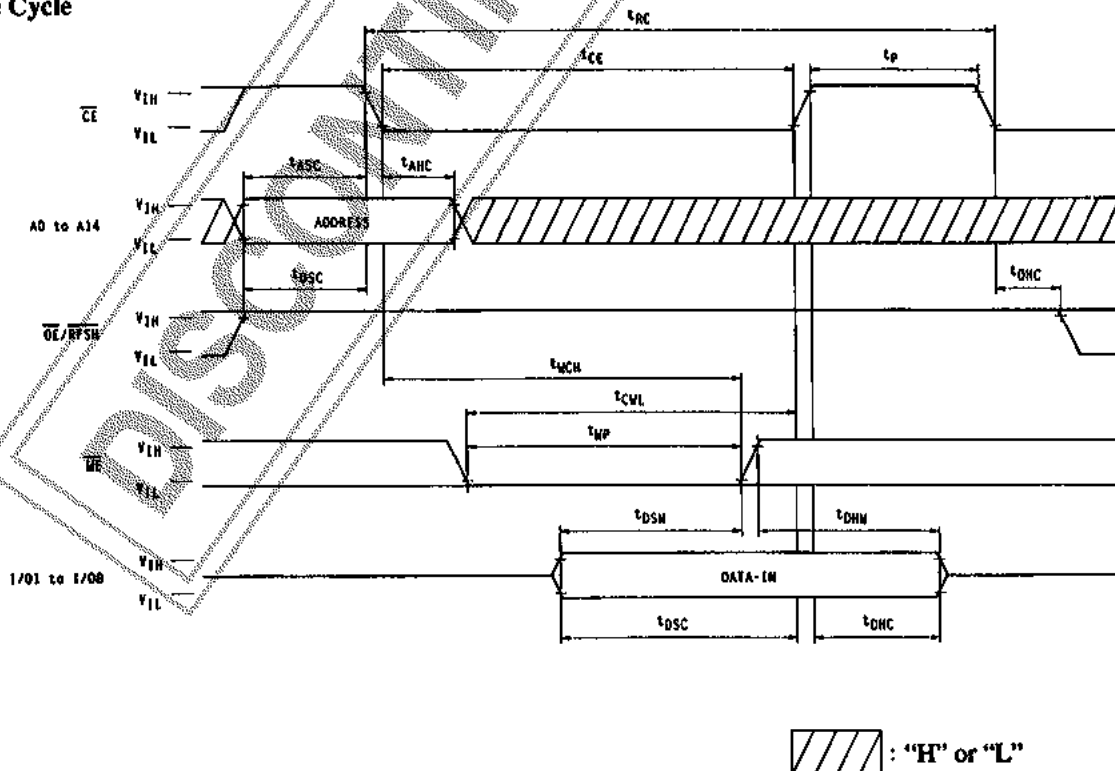
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Timing Chart
Read Cycle



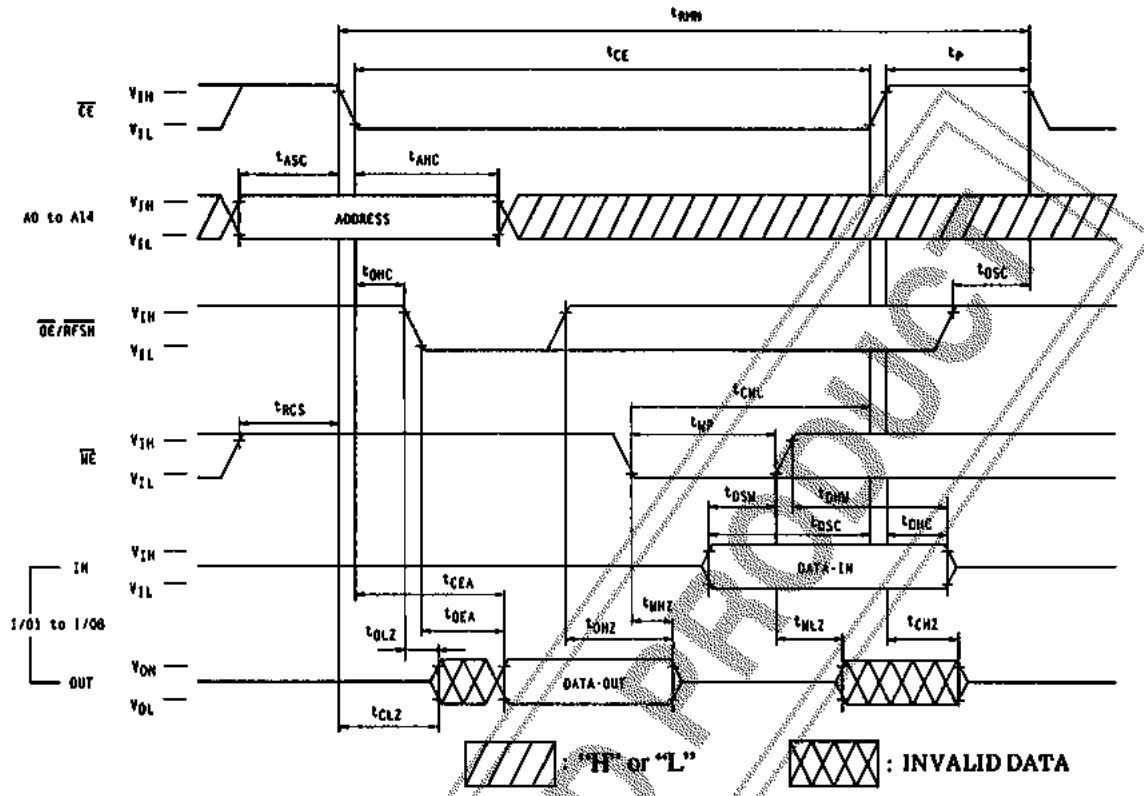
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Write Cycle



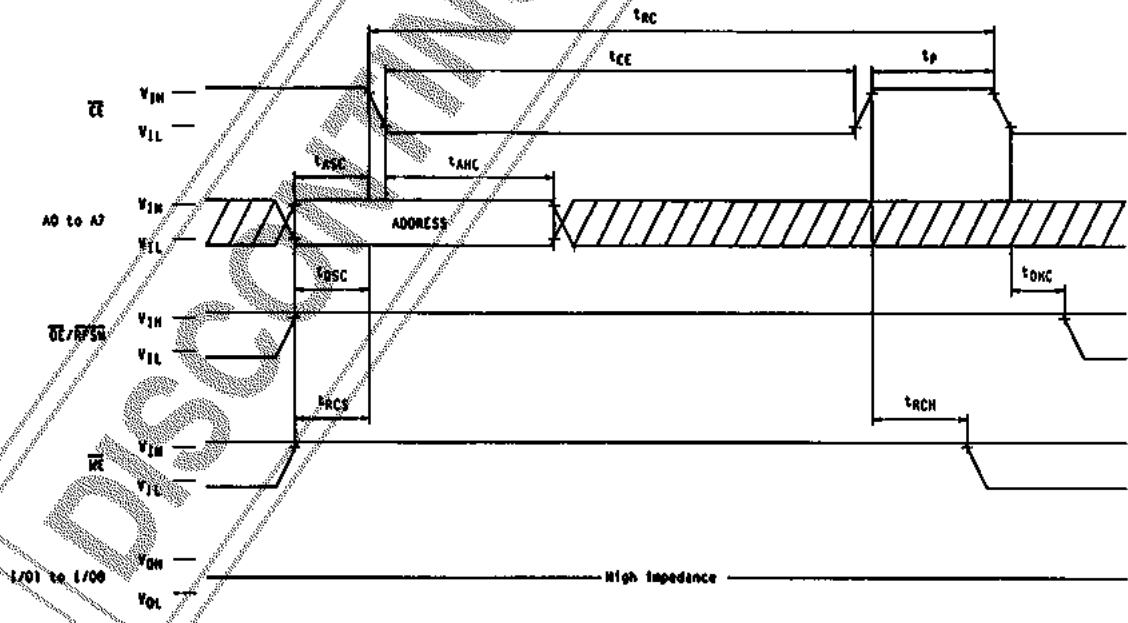
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Read-Write Cycle



AO1180

\overline{CE} -Only Refresh Cycle

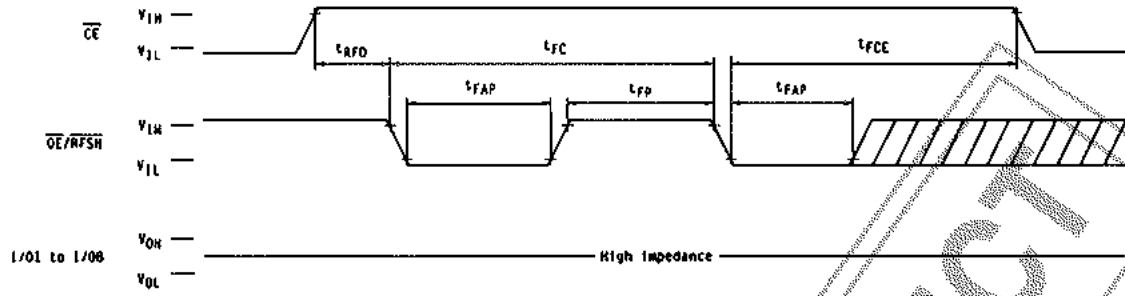


Note) A8 to A14: "H" or "L"

Hatched Area : "H" or "L"

AO1180

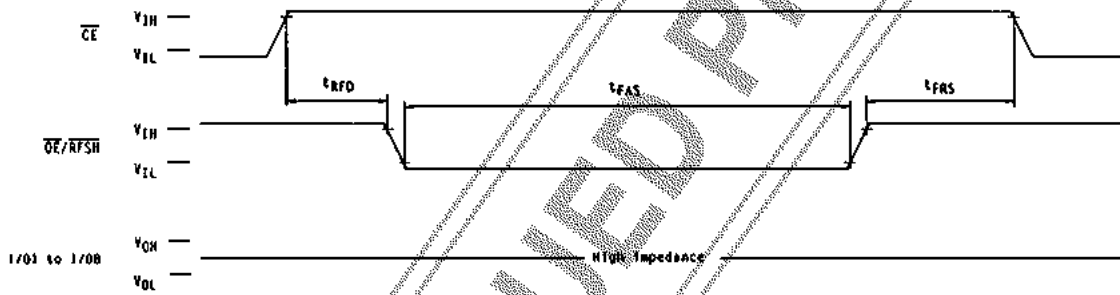
Auto-Refresh Cycle



Note) A0 to A14, \overline{WE} : "H" or "L"



Self-Refresh Cycle



Note) A0 to A14, \overline{WE} : "H" or "L"

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