DATA SHEET

ELPIDA

MOS INTEGRATED CIRCUIT

MC-45V16AB642

16M-WORD BY 64-BIT VirtualChannel™ DYNAMIC RAM MODULE UNBUFFERED TYPE

Description

The MC-45V16AB642 is a 16,777,216 words by 64 bits VirtualChannel dynamic RAM module on which 8 pieces of 128M VirtualChannel DRAM : μPD45V128821 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 16,777,216 words by 64 bits organization
- Clock frequency and access time from CLK

Part number	Read latency	Clock frequency MHz (MAX.)	Access time from CLK ns (MAX.)	Maximum supply current mA				
				Operating			Refresh	
				Prefetch	Restore	Channel read / write (Burst)	Auto	Self
MC-45V16AB642KF-A75	2	133	5.4	1,200		520	1,840	16

- Fully Standard Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Dual internal banks controlled by BA0 (Bank Select)
- Wrap sequence (interleave)
- Burst length (4)
- Read latency (2)
- Prefetch read latency (4)
- Auto precharge and without auto precharge
- Auto refresh and self refresh
- Single 3.3 V ± 0.3 V power supply
- Interface: LVTTL
- Refresh cycle: 4K cycles/64 ms
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Unbuffered type
- Serial PD

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Not all devices/types available in every country. Please check with local Elpida Memory, Inc. for availability and additional information.

Document No. E0027N10 (1st edition)
(Previous No. M15112EJ2V0DS00)
Date Published January 2001 CP (K)
Printed in Japan

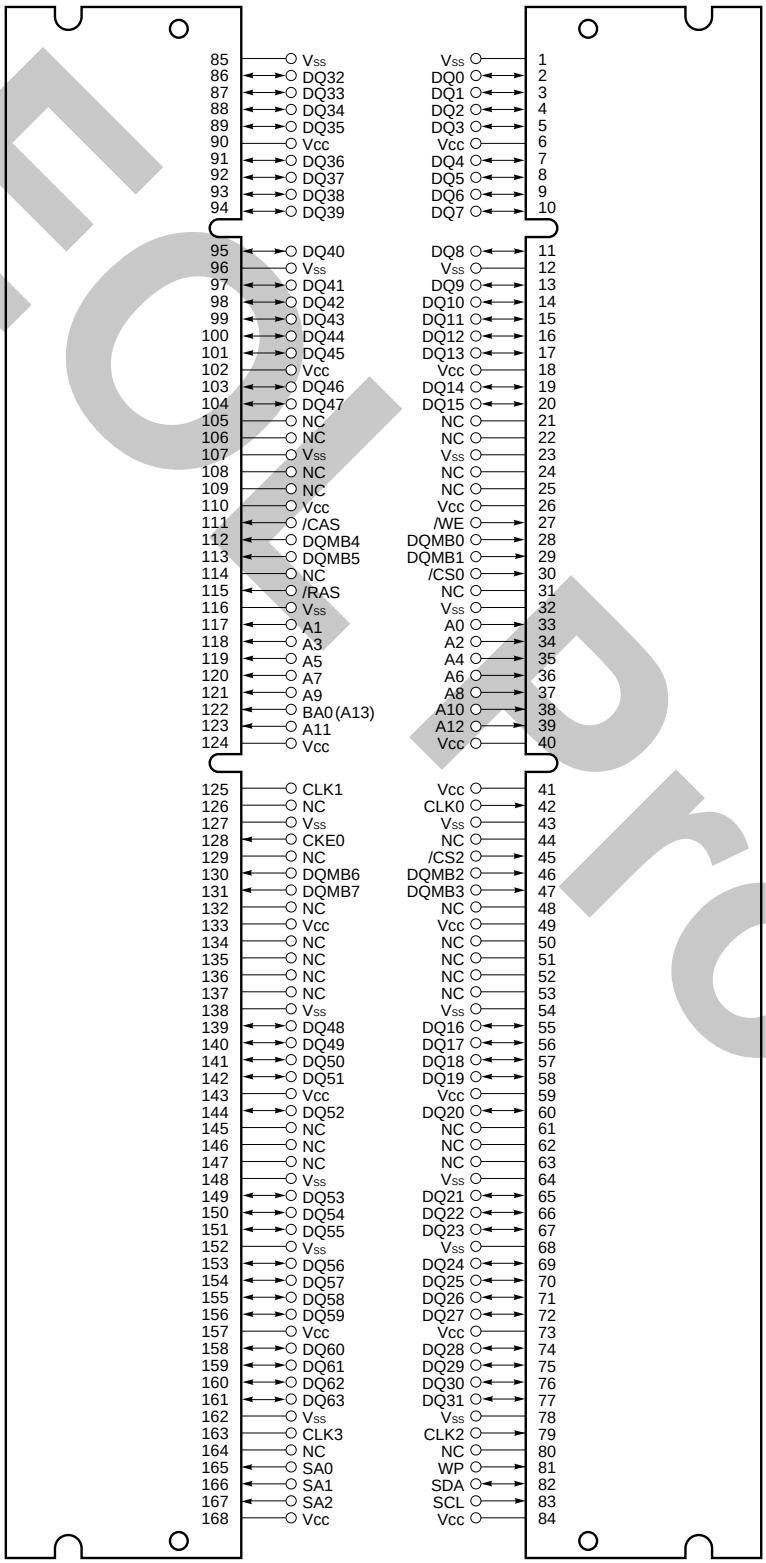
Elpida Memory, Inc. is a joint venture DRAM company of NEC Corporation and Hitachi, Ltd.

Ordering Information

Part number	Clock frequency MHz (MAX.)	Read latency	Prefetch read latency	Package	Mounted devices
MC-45V16AB642KF-A75	133	2	4	168-pin Dual In-line Memory Module (Socket Type) Edge connector : Gold plated 34.93 mm height	8 pieces of μPD45V128821G5 (10.16 mm (400) TSOP (II))

Pin Configuration

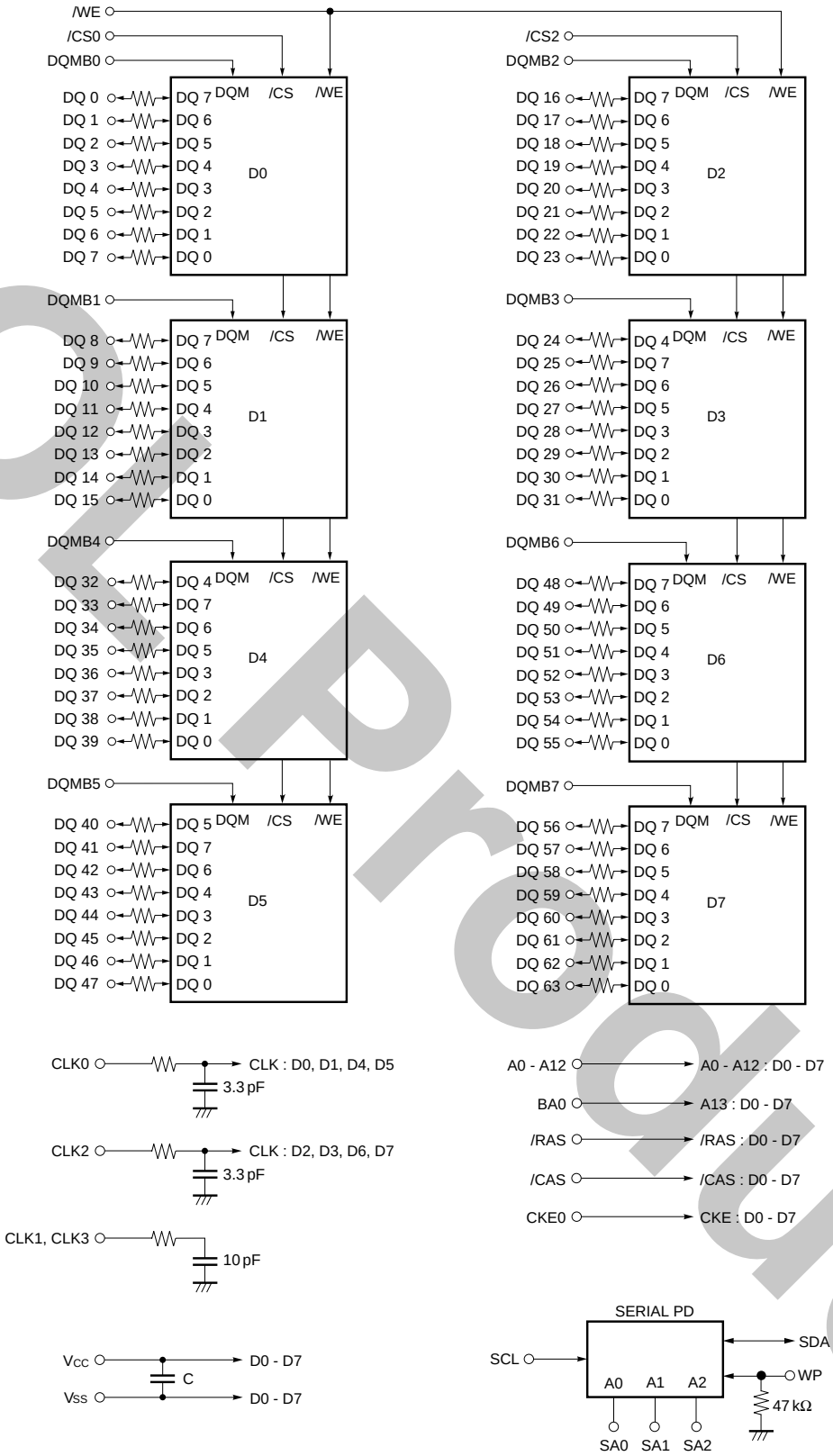
168-pin Dual In-line Memory Module Socket Type (Edge connector: Gold plated)



/xxx indicates active low signal.

A0 - A12	: Address Inputs
[Row: A0 - A12, Column: A0 - A7]	
BA0 (A13)	: VirtualChannel DRAM Bank Select
DQ0 - DQ63	: Data Inputs/Outputs
CLK0 - CLK3	: Clock Input
CKE0	: Clock Enable Input
/CS0, /CS2	: Chip Select Input
/RAS	: Row Address Strobe
/CAS	: Column Address Strobe
/WE	: Write Enable
DQMB0 - DQMB7	: DQ Mask Enable
SA0 - SA2	: Address Input for EEPROM
SDA	: Serial Data I/O for PD
SCL	: Clock Input for PD
V_{CC}	: Power Supply
V_{SS}	: Ground
WP	: Write Protect
NC	: No Connection

Block Diagram



Remarks 1. The value of all resistors is 10 Ω except WP.

2. D0 - D7: μPD45V128821 (8M words × 8 bits × 2 banks)

Electrical Specifications

- All voltages are referenced to V_{SS} (GND).
- After power up, wait more than 100 μs and then, execute power on sequence and auto refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V_{CC}		–0.5 to +4.6	V
Voltage on input pin relative to GND	V_T		–0.5 to +4.6	V
Short circuit output current	I_O		50	mA
Power dissipation	P_D		8	W
Operating ambient temperature	T_A		0 to 70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		–0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A12, BA0 (A13), /RAS, /CAS, /WE	38		62	pF
	C_{I2}	CLK0, CLK2	24		40	
	C_{I3}	CKE0	32		52	
	C_{I4}	/CS0, /CS2	17		29	
	C_{I5}	DQMB0 - DQMB7	7		13	
Data input/output capacitance	$C_{I/O}$	DQ0 - DQ63	7		13	pF

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Parameter	Symbol	Test condition	Grade	MIN.	MAX.	Unit	Notes
Operating current (Prefetch mode at one bank active)	$I_{CC1}P$	$t_{RC} \geq t_{RC\ (MIN.)}$ Prefetch is executed one time during t_{RC}.	-A75		1,200	mA	1
Operating current (Restore mode at one bank active)	$I_{CC1}R$	$t_{RC} \geq t_{RC\ (MIN.)}$	-A75		1,200	mA	1
Precharge standby current in power down mode	$I_{CC2}P$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = 15 ns			9.6	mA	
	$I_{CC2}PS$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = ∞			9.6		
Precharge standby current in non power down mode	$I_{CC2}N$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = 15 ns, /CS ≥ $V_{IH\ (MIN.)}$, Input signals are changed one time during 30 ns.			160	mA	
	$I_{CC2}NS$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = ∞ , Input signals are stable.			80		
Active standby current in power down mode	$I_{CC3}P$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = 15 ns			48	mA	
	$I_{CC3}PS$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = ∞			48		
Active standby current in non power down mode	$I_{CC3}N$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = 15 ns, /CS ≥ $V_{IH\ (MIN.)}$, Input signals are changed one time during 30 ns.			240	mA	
	$I_{CC3}NS$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = ∞, Input signals are stable.			160		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK\ (MIN.)}$, I_O = 0 mA Background : precharge standby	-A75		520	mA	2
Auto Refresh current	I_{CC5}	$t_{RCF} \geq t_{RCF\ (MIN.)}$	-A75		1,840	mA	3
Self refresh current	I_{CC6}	CKE ≤ 0.2 V	-A75		16	mA	
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V, All other pins not under test = 0 V		–8	+8	μA	
Output leakage current	$I_{O\ (L)}$	D_{OUT} is disabled, V_O = 0 to 3.6 V		–1.5	+1.5	μA	
High level output voltage	V_{OH}	I_O = – 4.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = + 4.0 mA			0.4	V	

Notes 1. I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during $t_{CK\ (MIN.)}$.

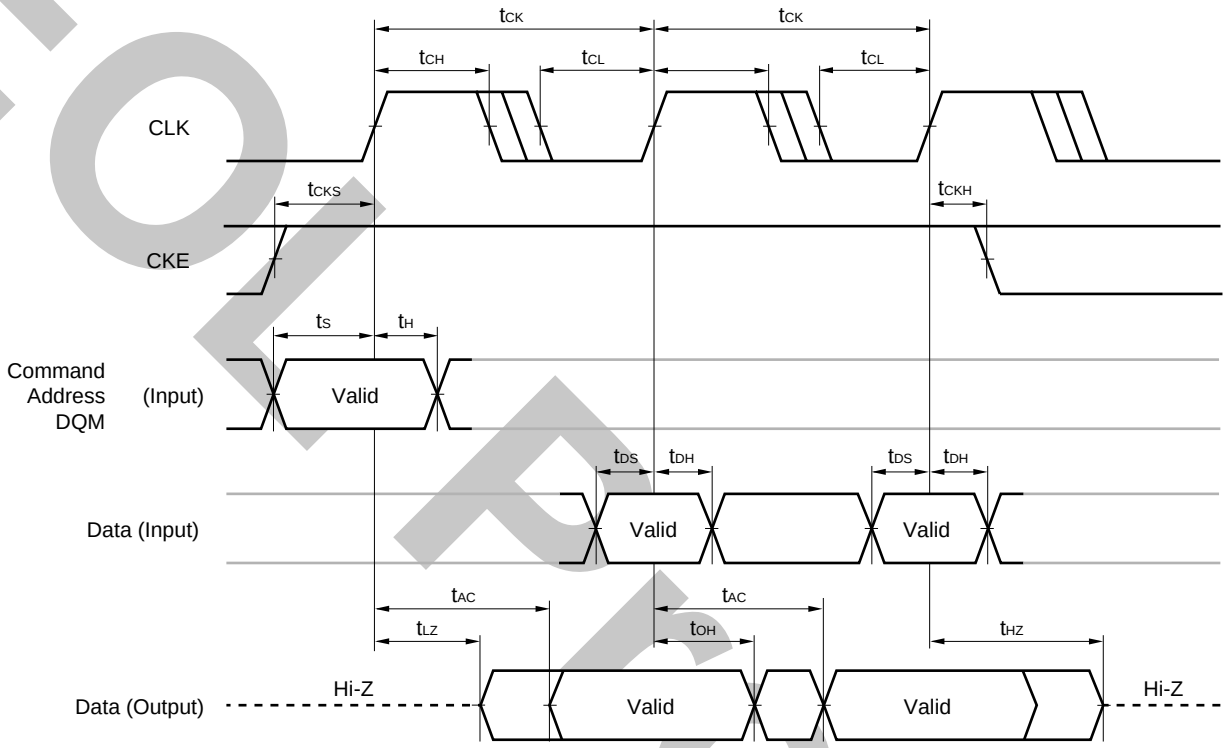
2. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during $t_{CK\ (MIN.)}$.

3. I_{CC5} is measured on condition that addresses are changed only one time during $t_{CK\ (MIN.)}$.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

Test Conditions

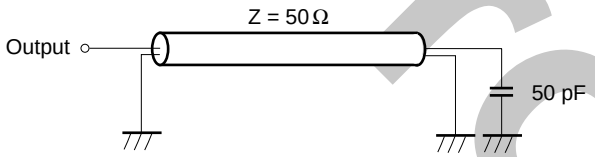
- AC measurements assume t_T = 1 ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL}.
- If t_T is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH\ (MIN.)}$ and $V_{IL\ (MAX.)}$.
- An access time is measured at 1.4 V.



AC characteristics

Parameter	Symbol	-A75		Unit	Note
		MIN.	MAX.		
Clock cycle time	t_{CK2}	7.5	–	ns	
Access time from CLK	t_{AC2}	–	5.4	ns	1
CLK high level width	t_{CH}	2.5	–	ns	
CLK low level width	t_{CL}	2.5	–	ns	
Data-out hold time	t_{OH}	2.7	–	ns	1
Data-out low-impedance time	t_{LZ}	0	–	ns	
Data-out high-impedance time	t_{HZ2}	2.5	5.4	ns	
Data-in setup time	t_{DS}	1.5	–	ns	
Data-in hold time	t_{DH}	0.8	–	ns	
Address, Command, DQM setup time	t_S	1.5	–	ns	
Address, Command, DQM hold time	t_H	0.8	–	ns	
CKE setup time	t_{CKS}	1.5	–	ns	
CKE hold time	t_{CKH}	0.8	–	ns	
CKE setup time (Power down exit)	t_{CKSP}	1.5	–	ns	
Transition time	t_T	0.5	30	ns	
Refresh time (4,096 refresh cycle)	t_{REF}	–	64	ms	
Mode register set cycle time	t_{RSC}	2	–	CLK	

Note 1. Output load.



AC characteristics (Background to Background operation)

Parameter	Symbol	-A75		Unit	Notes
		MIN.	MAX.		
Same Bank Operation					
ACT to ACT / REF Command period	t_{RC}	67.5	–	ns	
REF to REF / ACT Command period	t_{RCF}	67.5	–	ns	
ACT to PRE Command period	t_{RAS}	52.5	120,000	ns	
PRE to ACT / REF Command period	t_{RP}	20	–	ns	
ACT to PFC / PFCA Command delay time	t_{APD}	15	–	ns	
ACT to PFR Command delay time (Prefetch Read Operation)	t_{APRD}	15	–	ns	
PFC to PRE Command delay time	t_{PPL}	22.5	–	ns	
PFCA / PFR to ACT / REF Command delay time	t_{PAL}	45	–	ns	
RST / RSTA to ACT(R) Note1 Command delay time	t_{RAD}	7.5	30	ns	2
Same, Other Bank Operation					
ACT(R) Note1 to PFC / PFCA / PFR Command delay time	t_{RPD}	37.5	–	ns	
PFC to PFC / PFCA Command delay time	t_{PPD}	22.5	–	ns	
Other Bank Operation					
ACT to ACT / ACT(R) or ACT(R) to ACT Command delay time	t_{RRD}	15	–	ns	
ACT(R) to ACT(R) Command delay time	t_{RRDR}	30	–	ns	
PFC / PFCA to RST / RSTA Command delay time	t_{PRD}	22.5	–	ns	

Notes 1. ACT (R) command is ACT command after RST command.

2. The another background operation and same channel foreground operation are illegal while t_{RAD} period.

AC characteristics (Foreground to Foreground operation)

Parameter	Symbol	-A75		Unit	Note
		MIN.	MAX.		
READ/WRITE to READ/WRITE Command delay time	t_{CCD}	7.5	–	ns	

AC characteristics (Background to Foreground operation)
(after same channel Prefetch/Restore)

Parameter	Symbol	-A75		Unit	Note
		MIN.	MAX.		
PFC/PFCA to READ/WRITE Command delay time	t_{PCD}	15	–	ns	
ACT(R) to READ/WRITE Command delay time	t_{RCD}	30	–	ns	1

Note 1. ACT (R) command is ACT command after RST command.

Serial PD

(1/2)

Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
0	Defines the number of bytes written into serial PD memory		80H	1	0	0	0	0	0	0	0	128 bytes
1	Total number of bytes of serial PD memory		08H	0	0	0	0	1	0	0	0	256 bytes
2	Fundamental memory type		08H	0	0	0	0	1	0	0	0	VC DRAM
3	Number of row addresses		0DH	0	0	0	0	1	1	0	1	13 rows
4	Number of column addresses		08H	0	0	0	0	1	0	0	0	8 columns
5	Number of banks		01H	0	0	0	0	0	0	0	1	1 bank
6	Data width		40H	0	1	0	0	0	0	0	0	64 bits
7	Data width (continued)		00H	0	0	0	0	0	0	0	0	0
8	Voltage interface standard		01H	0	0	0	0	0	0	0	1	LVTTL
9	Read latency (/CAS latency) = 2 cycle time	-A75	75H	0	1	1	1	0	1	0	1	7.5 ns
10	Read latency (/CAS latency) = 2 access time	-A75	54H	0	1	0	1	0	1	0	0	5.4 ns
11	DIMM configuration type		00H	0	0	0	0	0	0	0	0	None
12	Refresh rate / type		80H	1	0	0	0	0	0	0	0	Normal
13	VC DRAM width		08H	0	0	0	0	1	0	0	0	×8
14	Error checking DRAM width		00H	0	0	0	0	0	0	0	0	None
15	Minimum clock delay		01H	0	0	0	0	0	0	0	1	1 clock
16	Burst length supported		04H	0	0	0	0	0	1	0	0	4
17	Number of banks on each VC DRAM		02H	0	0	0	0	0	0	1	0	2 banks
18	Read latency (/CAS latency) supported		02H	0	0	0	0	0	0	1	0	2
19	/CS latency supported		01H	0	0	0	0	0	0	0	1	0
20	/WE latency supported		01H	0	0	0	0	0	0	0	1	0
21	VC DRAM module attributes		00H	0	0	0	0	0	0	0	0	
22	VC DRAM device attributes : general		0EH	0	0	0	0	1	1	1	0	
23-26			00H	0	0	0	0	0	0	0	0	
27	$t_{RP\ (MIN.)}$	-A75	14H	0	0	0	1	0	1	0	0	20 ns
28	$t_{RRD\ (MIN.)}$	-A75	0FH	0	0	0	0	1	1	1	1	15 ns
29	$t_{APD\ (MIN.)}$	-A75	0FH	0	0	0	0	1	1	1	1	15 ns
30	$t_{RAS\ (MIN.)}$	-A75	34H	0	0	1	1	0	1	0	0	52.5 ns

(2/2)

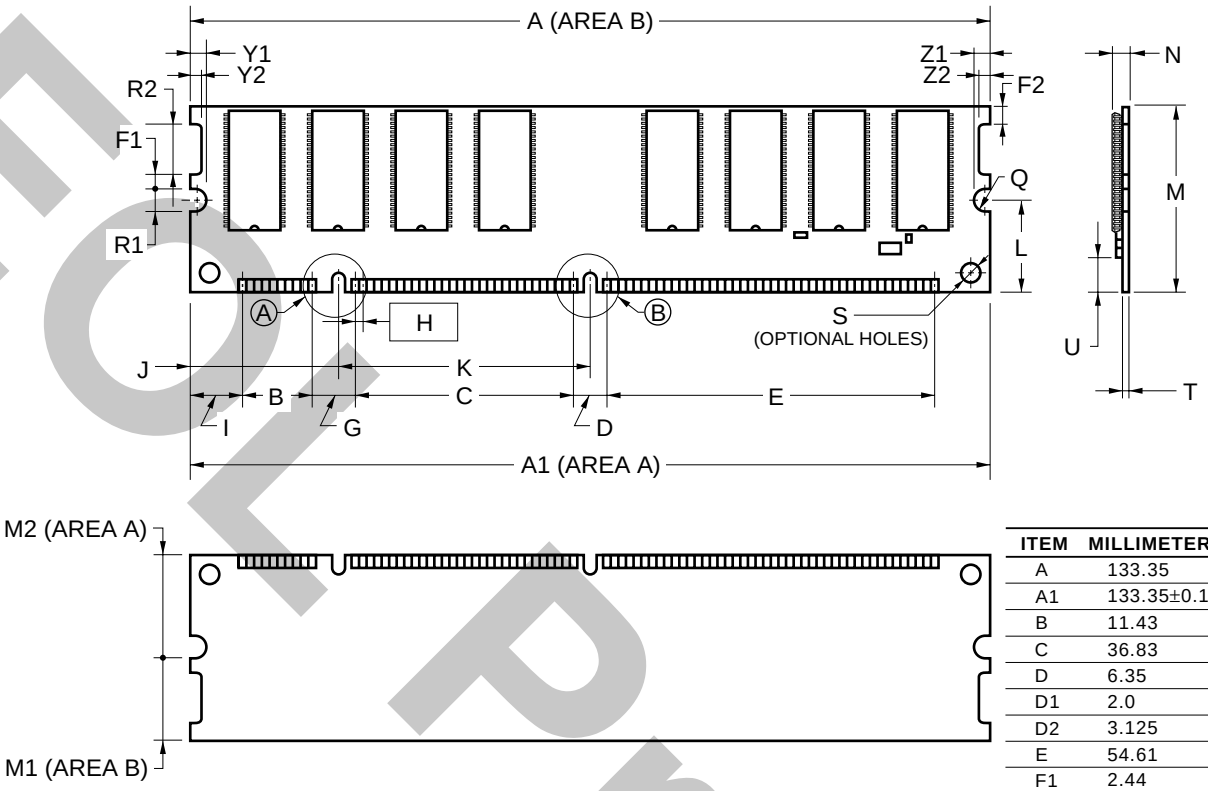
Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
31	Module bank density		20H	0	0	1	0	0	0	0	0	128M bytes
32	Address and command signal input setup time	-A75	15H	0	0	0	1	0	1	0	1	1.5 ns
33	Address and command signal input hold time	-A75	08H	0	0	0	0	1	0	0	0	0.8 ns
34	Data signal input setup time	-A75	15H	0	0	0	1	0	1	0	1	1.5 ns
35	Data signal input hold time	-A75	08H	0	0	0	0	1	0	0	0	0.8 ns
36	Prefetch read latency	-A75	04H	0	0	0	0	0	1	0	0	4 clocks
37	$t_{PCD\ (MIN.)}$	-A75	0FH	0	0	0	0	1	1	1	1	15 ns
38	Number of segment addresses		02H	0	0	0	0	0	0	1	0	2 bits
39	Number of channels		04H	0	0	0	0	0	1	0	0	16
40	Depth of channels		08H	0	0	0	0	1	0	0	0	256 bits
41-61												
62	SPD revision		02H	0	0	0	0	0	0	1	0	2.0
63	Checksum for bytes 0 - 62	-A75	34H	0	0	1	1	0	1	0	0	
64-71	Manufacture's JEDEC ID code											
72	Manufacturing location											
73-90	Manufacture's P/N											
91-92	Revision code											
93-94	Manufacturing date											
95-98	Assembly serial number											
99-125	Mfg specific											

Timing Charts

Please refer to the ***μ*PD45V128421, 45V128821, 45V128161 Data sheet** (E0025N).

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS
A	133.35
A1	133.35±0.13
B	11.43
C	36.83
D	6.35
D1	2.0
D2	3.125
E	54.61
F1	2.44
F2	3.18
G	6.35
H	1.27 (T.P.)
I	8.89
J	24.495
K	42.18
L	17.78
M	34.93±0.13
M1	15.15
M2	19.78
N	3.0 MAX.
P	1.0
Q	R2.0
R1	4.0±0.10
R2	9.53
S	ϕ3.0
T	1.27±0.1
U	4.0 MIN.
V	0.2±0.15
W	1.0±0.05
X	2.54±0.10
Y1	3.0 MIN.
Y2	2.26
Z1	3.0 MIN.
Z2	2.26

Revision History

Edition / Date	Page		Description	
	This edition	Previous edition	Type of edition	Location
NEC Corporation (M15112E)				
1st edition / Sep. 2000	–	–	–	–
2nd edition / Dec. 2000	p.1, 2	p.1, 2	Deletion	-A10
	p.6, 8, 9, 10, 11, 12	p.6, 8, 9, 10, 11, 12		-A10 specs
Elpida Memory, Inc. (E0027N)				
1st edition / Jan. 2001	–	–	–	Republished by Elpida Memory, Inc.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory IC, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

When re-packing memory modules, be sure the modules are NOT touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

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