Application Note AN-6027

Design of Power Factor Correction Circuit Using FAN7530

1. Introduction

The FAN7530 is an active power factor correction (PFC) controller for the boost PFC application that operates in the critical conduction mode (CRM). The critical conduction mode boost power factor converter operates at the boundary of continuous conduction mode and discontinuous conduction mode. The CRM PFC controllers are of two kinds: the current-mode CRM PFC controller and the voltage-mode CRM PFC controller. For the current mode, a boost switch is turned on when the inductor current reaches zero and turned off when the inductor current meets the desired current reference. In this case, the rectified AC line voltage should be sensed to generate the current reference, as in the FAN7527B; however, the sensing network can cause additional power loss. In the voltage mode, the switch turn-on is the same as that of the current mode, but the switch turn-off is determined by an internal ramp signal. The ramp signal is compared with an error amplifier output and the switch turn-on time is controlled to be constant, as shown in Figure 1. If the turn-on time is constant, the peak inductor current is proportional to the rectified AC line voltage, as shown in Figure 2. In this way, the input current waveform follows the waveform of the input voltage, thereby obtaining a good power factor. The FAN7530 is a voltage-mode CRM PFC controller. Because the voltage-mode CRM PFC controller does not need the rectified AC line voltage information, it can save the power loss of the sensing network.

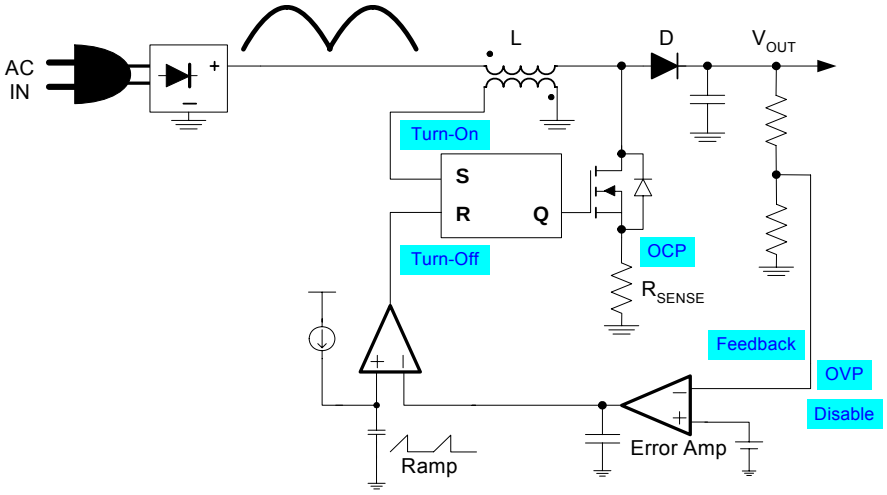


Figure 1. Voltage Mode CRM Boost PFC Circuit

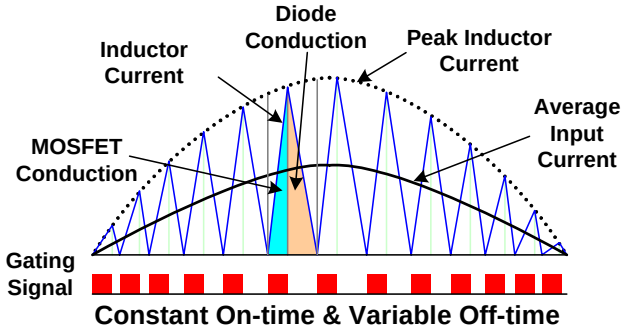


Figure 2. CRM Boost PFC Inductor Current Waveform

Figure 3 shows the block diagram of the FAN7530. The only difference between the FAN7529 and the FAN7530 is the pin configuration of pin 2 and pin 3. For the FAN7529, the INV pin and the COMP pin are adjacent, but because the voltage of pin 1 is 2.5V and the operating range of pin 2 is from 1V to 5V, the PFC output voltage can increase at light load if pins 1 and 2 are shorted. For the FAN7530, however, the INV pin and the MOT pin are adjacent. Because the voltage of the MOT pin is 2.9V, the over-voltage protection works if pin 1 and pin 2 are shorted.

Block Diagram

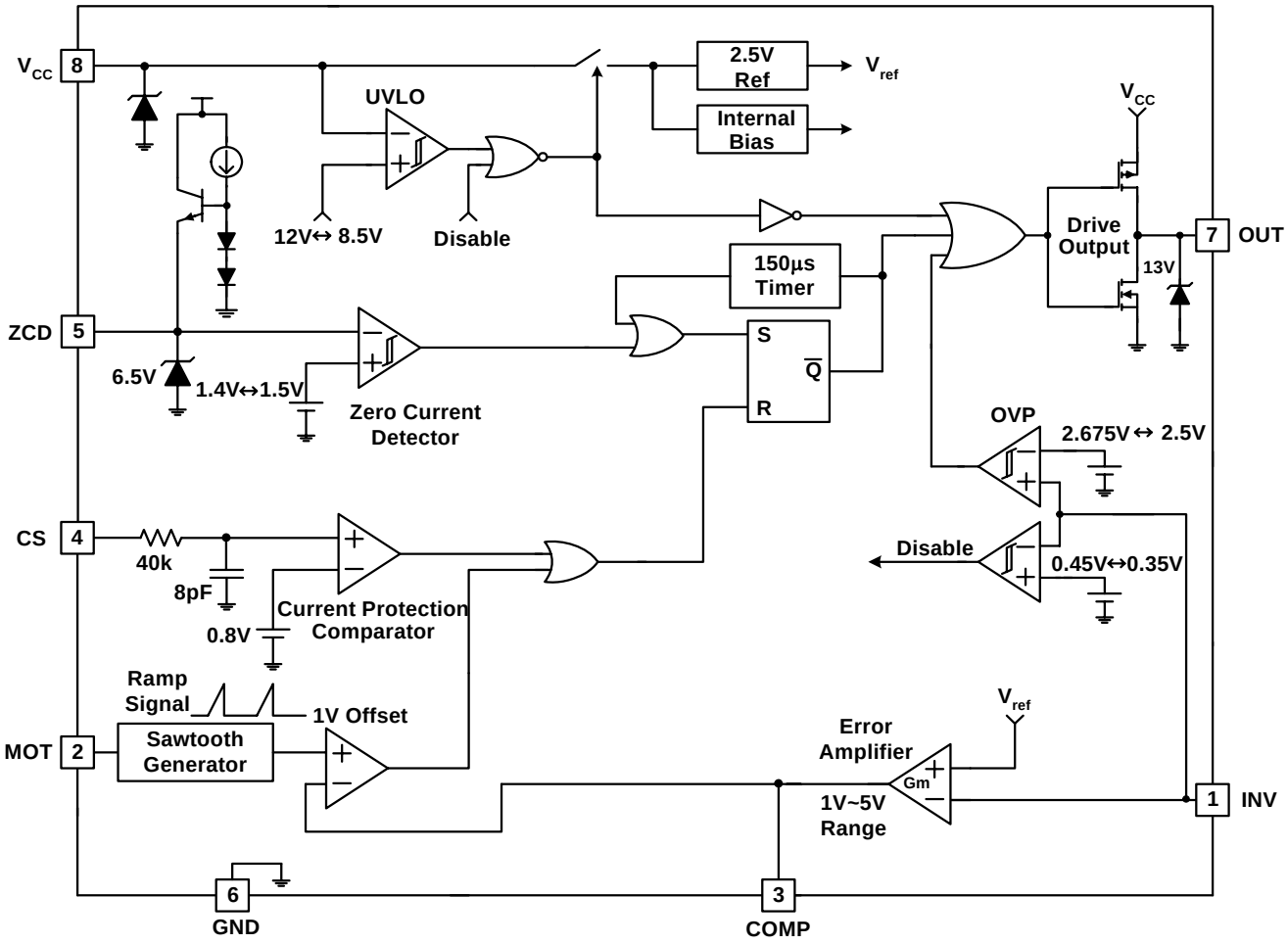


Figure 3. Block Diagram of the FAN7530 Showing Error Amplifier Block, Zero Current Detector Block, Sawtooth Generator Block, Over-Current Protection Block, and Switch Drive Block

2. Device Block Description

2.1 Error Amplifier Block

The error amplifier block consists of a transconductance amplifier, output OVP comparator, and disable comparator. For the output voltage control, a transconductance amplifier is used instead of the conventional voltage amplifier. The transconductance amplifier (voltage controlled current source) aids the implementation of OVP and disable function. The output current of the amplifier changes according to the voltage difference of the inverting input and the non-inverting input of the amplifier. The output voltage of the amplifier is compared with the internal ramp signal to generate the switch turn-off signal. The OVP comparator shuts down the output drive block when the voltage of the INV pin is higher than 2.675V and there is 0.175V hysteresis. The disable comparator disables the operation of the FAN7530 when the voltage of the inverting input is lower than 0.45V and there is 100mV hysteresis. An external, small-signal MOSFET can be used to disable the IC, as shown in Figure 4. The IC operating current decreases to under 65µA to reduce power consumption if the IC is disabled.

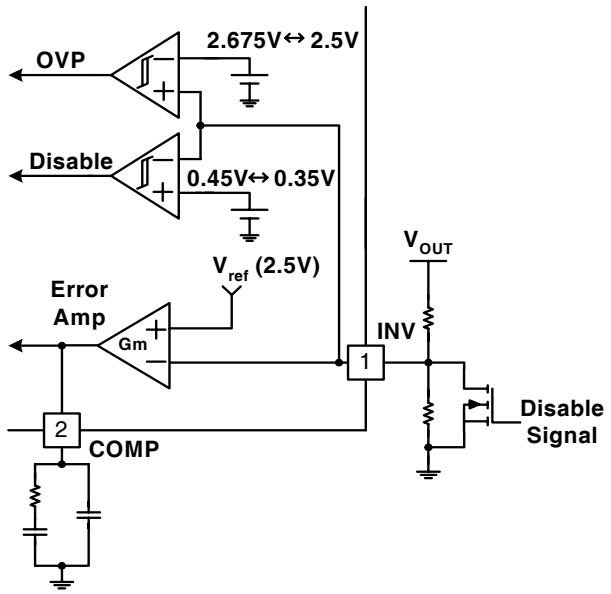


Figure 4. Error Amplifier Block

2.2 Zero Current Detection Block

The zero current detector (ZCD) generates the turn-on signal of the MOSFET when the boost inductor current reaches zero using an auxiliary winding coupled with the inductor. Because the polarity of the auxiliary winding is opposite the inductor winding, the auxiliary winding voltage is negative and proportional to the rectified AC line voltage when the MOSFET is turned on. If the MOSFET is turned off, the voltage becomes positive and proportional to the difference between V_{OUT} and V_{IN}. If the inductor current reaches zero, the junction capacitor of the MOSFET resonates with the boost inductor and the auxiliary winding voltage decreases resonantly. If it reaches 1.4V, the zero current detector turns on the MOSFET. The ZCD pin is protected internally by two clamps: the 6.5V HIGH clamp and the 0.65V LOW clamp, as shown in Figure 5.

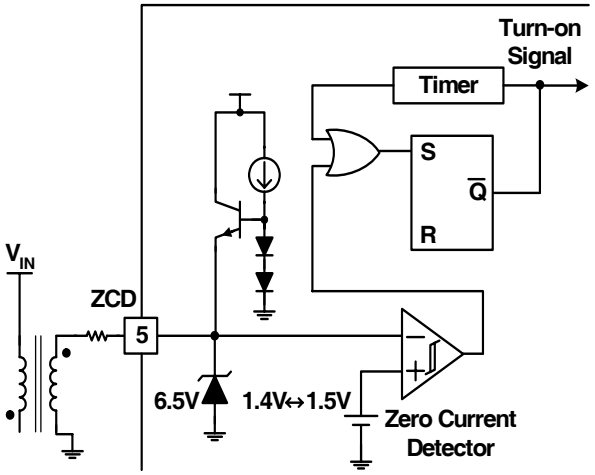


Figure 5. Zero Current Detector Block

Figure 6 shows typical ZCD-related waveforms. Because the ZCD pin has some capacitance, there can be some delay caused by R_{zcd} and the turn-on time can be delayed.

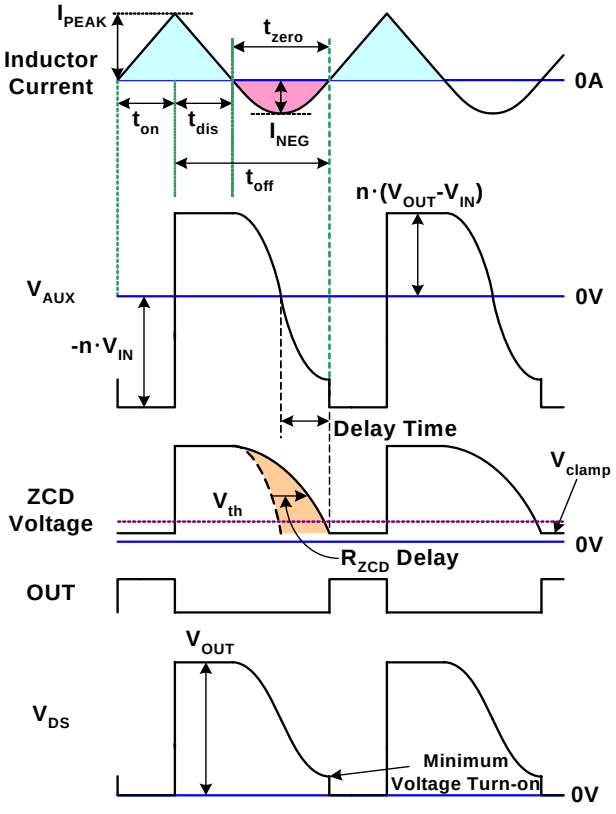


Figure 6. Zero Current Detector Waveform

Ideally, the switch must be turned on when the inductor current reaches zero; but because of the structure of the ZCD block and R_{zcd} delay, it is turned on after some delay time. During this delay time, the stored charge of the C_{OSS} (MOSFET output capacitor) is discharged through the path indicated in Figure 7. This charge is transferred into a small filter capacitor, C_{in1}, which is connected to the bridge diode. Therefore, there is no current flow from the input side, meaning the input current I_{in} is zero during this period. For better total harmonic distortion (THD), it is important to make t_{zero} / T_S as small as possible. As shown in Figure 6, t_{zero} is proportional to $\sqrt{L \cdot C_{oss}}$ but t_{on} and t_{dis} are proportional to L. Therefore t_{zero} / T_S is approximately inversely proportional to $\sqrt{L}$. Therefore THD increases as the inductance decreases. Reducing the inductance can decrease the inductor size and cost but the switching loss increases because of the increased switching frequency. In real case, boost diode's junction capacitance and boost inductor's parasitic capacitance should be added to C_{OSS} when calculating t_{zero}. That means it is important to minimize the parasitic capacitance of the boost inductor and diode junction capacitance for better THD.

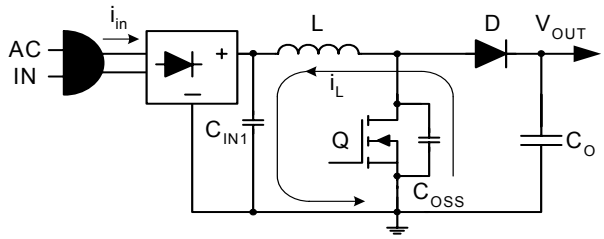


Figure 7. Current Flow During t_{zero}

In the ZCD block, there is an internal timer to provide a means to start or restart the switching if the drive output has been low for more than 150μs from the falling edge of the drive output. Without this timer, the PFC converter does not work because the inductor current is always zero when the IC initially starts operation and the ZCD winding voltage does not become positive without any switching.

2.3 Sawtooth Generator Block

The output of the error amplifier and the output of the sawtooth generator are compared to determine the MOSFET turn-off instant. The slope of the sawtooth is determined by an external resistor connected at the maximum on time (MOT) pin. The voltage of the MOT pin is 2.9V and the slope is proportional to the current flowing output of the MOT pin. The maximum on time is determined when the output of the error amplifier is 5V. When a 40.5kΩ resistor is connected, the maximum on time is 24μs. As the resistance increases, the maximum on time increases, because the slope decreases. The MOSFET on time is zero when the output of the error amplifier is lower than 1V.

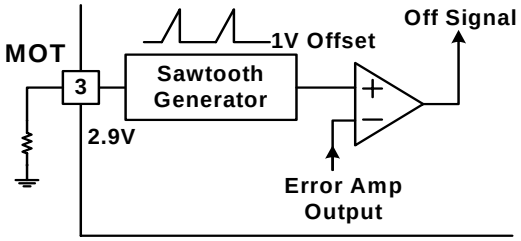


Figure 8. Sawtooth Generator Block

2.4 Over-Current Protection Block

The MOSFET current is sensed using an external sense resistor for over-current protection. If the CS pin voltage is higher than 0.8V, the over-current protection comparator generates a protection signal to turn off the MOSFET. An internal R/C filter has been included to filter switching noise.

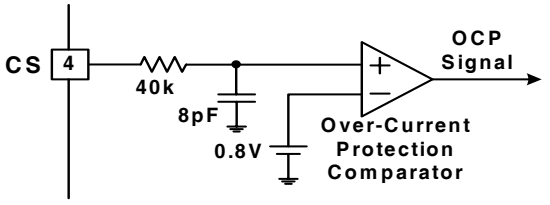


Figure 9. Over-Current Protection Block

2.5 Switch Drive Block

The FAN7530 contains a single totem-pole output stage designed specifically for a direct drive of a power MOSFET. The drive output is capable of up to 500mA peak sourcing current and 800mA peak sinking current with a typical rise and fall time of 50ns with a 1.0nF load. Additional circuitry has been added to keep the drive output in a sinking mode whenever the UVLO is active. The output voltage is clamped at 13V to protect the MOSFET gate even when the V_{CC} voltage is higher than 13V.

3.Circuit Components Design

3.1 Power Stage Design

1) Boost Inductor Design

The boost inductor value is determined by the output power and the minimum switching frequency. The minimum switching frequency must be above the audio frequency (20kHz) to prevent audible noise. The maximum switching period, $T_{S(max)}$, is a function of $V_{in(peak)}$ and V_o, the output voltage. It can have a maximum value at the highest input voltage or at the lowest input voltage according to V_o. Compare $T_{S(max)}$ at $V_{in(peak\_min)}$ and $V_{in(peak\_max)}$, then select the higher value for the maximum switching period. The boost inductor value can be obtained by Equation 6.

$$t_{on} = L \cdot \frac{I_{L(peak)}(t)}{V_{in(peak)}\sin(\omega t)} = L \cdot \frac{2 \cdot I_{in(peak)}\sin(\omega t)}{V_{in(peak)}\sin(\omega t)} = L \cdot \frac{2 \cdot I_{in(peak)}}{V_{in(peak)}} \quad (1)$$

$$t_{off} = L \cdot \frac{I_{L(peak)}(t)}{V_o - V_{in(peak)}\sin(\omega t)} = L \cdot \frac{2 \cdot I_{in(peak)}\sin(\omega t)}{V_o - V_{in(peak)}\sin(\omega t)} \quad (2)$$

$$I_{in(peak)} = \frac{2 \cdot V_o \cdot I_o}{\eta \cdot V_{in(peak)}} \quad (3)$$

$$T_S = t_{on} + t_{off} = 2 \cdot L \cdot I_{in(peak)}\left(\frac{1}{V_{in(peak)}} + \frac{\sin(\omega t)}{V_o - V_{in(peak)}\sin(\omega t)}\right) = \frac{4 \cdot L \cdot V_o \cdot I_o}{\eta \cdot V_{in(peak)}^2}\left(1 + \frac{V_{in(peak)} \cdot \sin(\omega t)}{V_o - V_{in(peak)}\sin(\omega t)}\right) \quad (4)$$

$$T_{S(max)} = \frac{4 \cdot L \cdot V_o \cdot I_{o(max)}}{\eta \cdot V_{in(peak)}^2}\left(1 + \frac{V_{in(peak)}}{V_o - V_{in(peak)}}\right) \quad (5)$$

$$L = \frac{\eta \cdot V_{in(peak)}^2}{4 \cdot f_{sw(min)} \cdot V_o \cdot I_{o(max)}\left(1 + \frac{V_{in(peak)}}{V_o - V_{in(peak)}}\right)} \quad (6)$$

2) Auxiliary Winding Design

The auxiliary winding voltage is lowest at the highest line. So the turn number of the auxiliary winding can be obtained by Equation 7. The voltage should be higher than the ZCD threshold voltage of 1.5V.

$$N_{aux} > \frac{1.5V \cdot N_P}{(V_o - \sqrt{2}V_{in(peak\_max)})} \quad (7)$$

3) Input Capacitor Design

The voltage ripple of the input capacitor is maximum when the line is lowest and the load is heaviest. If $f_{sw(min)} >> f_{ac}$, the input current can be assumed to be constant during a switching period.

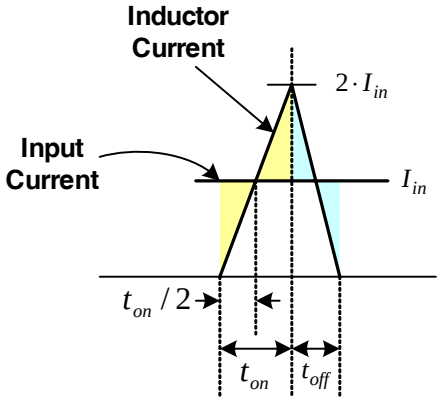


Figure 10. Input Current and Inductor Current Waveform During a Switch Cycle

$$C_{in} \geq \frac{2}{\Delta V_{in(max)}}\int_0^{\frac{t_{on}}{2}}\left(I_{in(peak\_max)} - 2\frac{I_{in(peak\_max)}}{t_{on}}t\right)dt \geq \frac{t_{on} \cdot I_{in(peak\_max)}}{2 \cdot \Delta V_{in(max)}} \geq \frac{L \cdot I_{o(max)}^2 \cdot V_o^2}{\Delta V_{in(max)} \cdot V_{in(peak\_min)}^3} \quad (8)$$

The input capacitor must be larger than the value calculated by Equation 8 and the maximum input capacitance is limited by the input displacement factor (IDF), defined as IDF≡cosθ. As shown in Figure 11, the input capacitor generates 90°

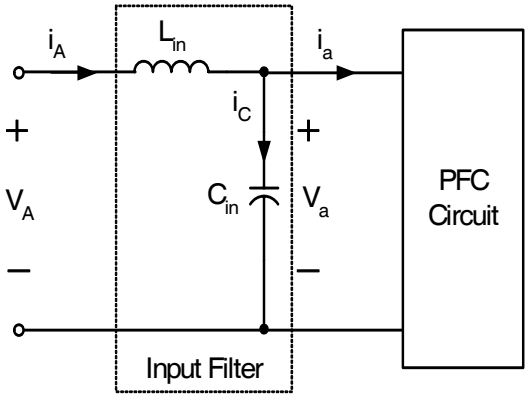
leading current, which causes phase difference between the line current and the line voltage. The phase difference increases as the capacitance of the input capacitor increases. Therefore, the input capacitor must be smaller than $C_{in(max)}$ calculated by Equation 12. $C_{in(max)}$ is the sum of all the capacitors connected at the input side.

$$V_a = V_A = V_{in(peak)} \cos(\omega t) \tag{9}$$

$$i_a = I_a \cos(\omega t)$$
$$i_A = i_a + i_c = I_a \cos(\omega t) - \omega \cdot C_{in} \cdot V_{in(peak)} \sin(\omega t) \tag{10}$$

$$\theta = \tan^{-1}\left(\frac{\omega \cdot C_{in} \cdot V_{in(peak)}}{I_a}\right) \tag{11}$$

$$C_{in(\max)} = \frac{I_a}{\omega \cdot V_{in(peak)}} \tan\left(\cos^{-1}(IDF)\right)$$
$$= \frac{2 \cdot V_o \cdot I_o}{\omega \cdot V_{in(peak\_\max)}^2} \tan\left(\cos^{-1}(IDF)\right) \tag{12}$$



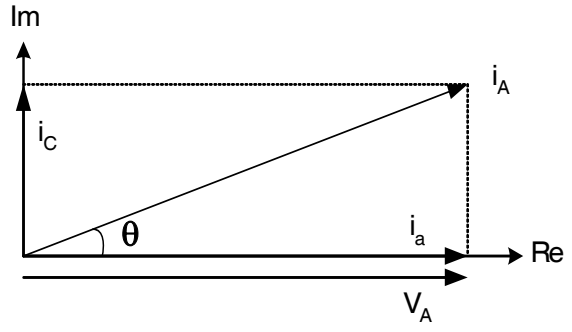


Figure 11. Input Voltage and Current Displacement Due to Input Filter Capacitance

4) Output Capacitor Design

The output capacitor is selected by the relationship between the input and output power. As shown in Figure 13, the minimum output capacitance is determined by Equation 14.

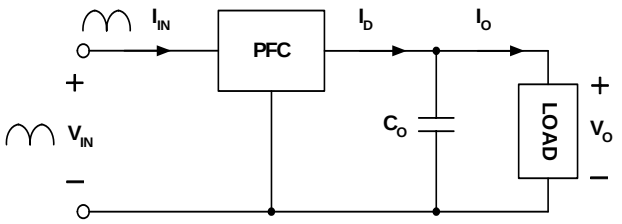


Figure 12. PFC Configuration

$$P_{in} = I_{in(rms)} \cdot V_{in(rms)} \cdot \left(1 - \cos(2\omega t)\right) = I_D V_o$$
$$I_D = \frac{I_{in(rms)} \cdot V_{in(rms)}}{V_o}\left(1 - \cos(2\omega t)\right)$$
$$= I_o \cdot \left(1 - \cos(2\omega t)\right) \tag{13}$$

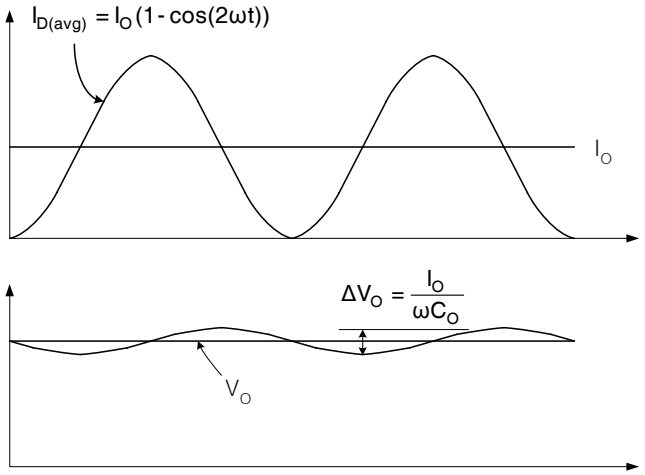


Figure 13. Diode Current and Output Voltage Waveform

$$C_{o(\min)} \geq \frac{I_{o(\max)}}{2\pi \cdot f_{ac} \cdot \Delta V_{o(\max)}} \tag{14}$$

5) MOSFET and Diode Selection

The maximum MOSFET RMS current is obtained by Equation 15 and the conduction loss of the MOSFET is calculated by Equation 16. When MOSFET turns on, the MOSFET current rises from zero, so the turn-on loss is negligible. The MOSFET turn-off loss and the MOSFET discharge loss are obtained by Equations 17 and 18, respectively. The switching frequency of the critical conduction mode boost PFC converter varies according to the line and load conditions.

The switching frequency is the average value during a line period. The total MOSFET loss can be calculated by Equation 19 and a MOSFET can be selected considering the MOSFET thermal characteristic.

$$I_{Qrms} = I_{L(peak\_max)}\sqrt{\frac{1}{6}-\frac{4\sqrt{2}\cdot V_{in(LL)}}{9\pi\cdot V_o}} = \frac{2\sqrt{2}\cdot V_o\cdot I_{o(max)}}{\eta\cdot V_{in(LL)}}\sqrt{\frac{1}{6}-\frac{4\sqrt{2}\cdot V_{in(LL)}}{9\pi\cdot V_o}} \quad (15)$$

$$P_{on} = I_{Qrms}^2\cdot R_{DSon} \quad (16)$$

$$P_{turn-off} = \frac{1}{6}V_o\cdot I_{L(peak\_max)}\cdot t_f\cdot f_{sw} = \frac{\sqrt{2}}{3}\frac{V_o^2\cdot I_{o(max)}}{\eta\cdot V_{in(LL)}}\cdot t_f\cdot f_{sw} \quad (17)$$

$$P_{discharge} = \frac{4}{3}C_{oss.Vo}\cdot V_o^2\cdot f_{sw} \quad (18)$$

$$P_{MOSFET} = P_{on} + P_{turn-off} + P_{discharge} \quad (19)$$

The diode average current can be calculated by Equation 20. The total diode loss can be calculated by Equation 21. Select a diode considering diode thermal characteristic.

$$I_{Davg} = I_{o(max)} \quad (20)$$

$$P_{Diode} = V_f\cdot I_{Davg} \quad (21)$$

3.2 Control Circuit Design

1) Output Voltage Sensing Resistor and Feedback Loop Design

The output voltage sensing resistors, R_{o1} and R_{o2}, are determined by the output voltage at the high line by Equation 22. The output voltage sensing resistors cause power loss, therefore R_{o1} should be higher than 1MΩ. Too high resistance can cause some delay of the OVP circuit due to internal capacitance (Cp), which may slightly increase the OVP level.

$$\frac{R_{o1}}{R_{o2}} = \frac{V_{o\_high}-2.5}{2.5} \quad (22)$$

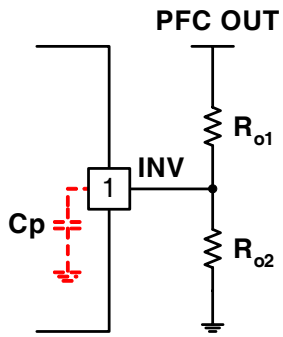


Figure 14. Output Voltage Sensing Circuit

The feedback loop bandwidth must be lower than 20Hz for the PFC application. If the bandwidth is higher than 20Hz, the control loop may try to reduce the 120Hz ripple of the output voltage and the line current may be distorted, decreasing the power factor. A capacitor is connected between COMP and GND to eliminate the 120Hz ripple voltage by 40dB. If a capacitor is connected between the output of the error amplifier and the GND, the error amplifier works as an integrator and the error amplifier compensation capacitor can be calculated by Equation 23. To improve the power factor, C_{comp} must be higher than the calculated value. If the value is too high, the output voltage control loop may become slow.

$$C_{comp} = gm\cdot\frac{R_{o2}}{0.01\cdot 2\pi\cdot 120Hz\cdot(R_{o1}+R_{o2})} \quad (23)$$

To improve the output voltage regulation, a resistor and a capacitor can be added to a simple integrator, as shown in Figure 15. The resistor, R_{comp}, increases mid-band gain and the capacitor, C_{filter}, which is 1/10~1/5 of the C_{comp}, is used to filter high-frequency noise. The gain of the error amplifier with the circuit in Figure 15 is shown in Figure 16.

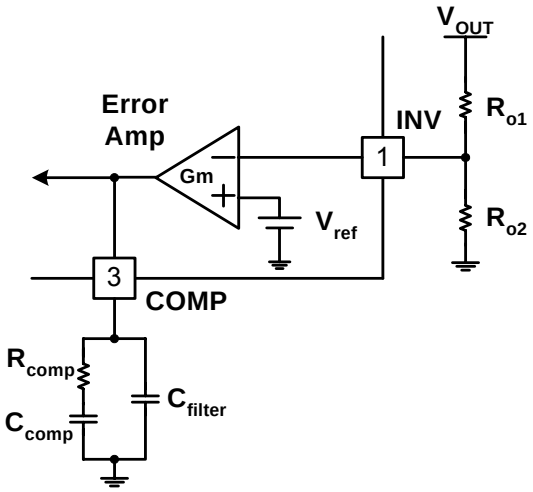


Figure 15. Error Amplifier Circuit

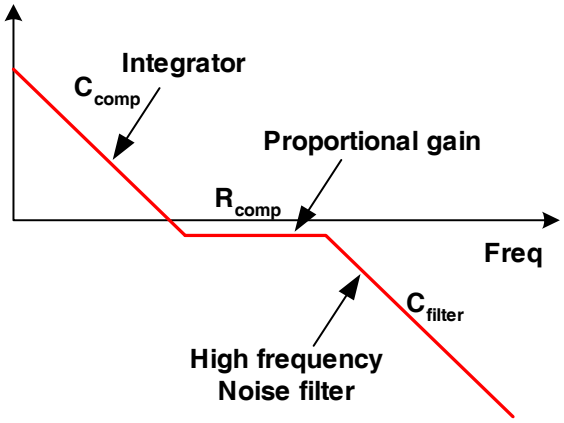


Figure 16. Gain of the Error Amplifier

2) Zero Current Detection Resistor Design

The ZCD current should be less than 10mA; therefore the zero current detection resistor, R_{ZCD} is determined by Equation 24.

$$R_{ZCD} = \left(\frac{N_{aux} \cdot V_o}{N_p} - 5.8V \right) / 10mA \qquad (24)$$

Because the ZCD pin has some capacitance, the ZCD resistor and the capacitor cause some delay for ZCD detection, as shown in Figure 17. Because of this delay, the MOSFET is not turned on when the inductor current reaches zero and the MOSFET junction capacitor and the inductor resonate. The inductor current changes its direction and flows negatively. The peak value of this negative current is determined by Equation 25. As shown in Equation 25, the negative current increases as the input voltage is close to zero and C_{OSS} increases. This negative current decreases average inductor current and causes zero crossing distortion near the zero crossing point of the AC line, as shown in Figure 18. To minimize the zero crossing distortion, C_{OSS} must be minimized and a larger inductor should be used. There is a limitation in minimizing C_{OSS} and using a large inductor because a small MOSFET increases MOSFET conduction loss and a larger inductor is more expensive.

$$I_{NEG} = \sqrt{\frac{C_{oss}}{L}} \cdot (V_o - V_{in}) \qquad (25)$$

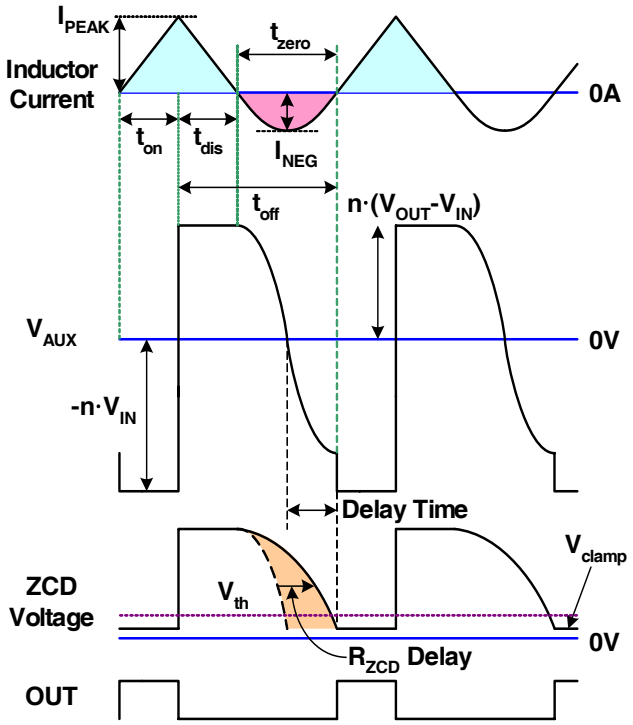


Figure 17. ZCD Waveforms

If the R_{ZCD} is selected appropriately, the MOSFET can be turned on when the V_{ds} voltage is minimum to reduce switching loss. It is recommended to design the R_{ZCD} to turn on the MOSFET when the V_{ds} voltage is minimum.

To improve the zero crossing distortion, the MOSFET turn-on time should be increased near the AC line zero crossing point. If a resistor is connected between the MOT and the auxiliary winding, as shown in Figure 19, the function can be implemented easily. Because the auxiliary winding voltage is negatively proportional to the input voltage during the MOSFET turn-on time, the current I2 is proportional to the input voltage (as shown in Figure 19). Therefore, the slope of the internal ramp changes according to input voltage as the current flowing out of the MOT pin changes, as shown in Figure 20. I2 current is maximum at the highest line voltage and the zero crossing improvement is best when I2 is 100% ~ 200% of I1. R2 value should be chosen by experiment.

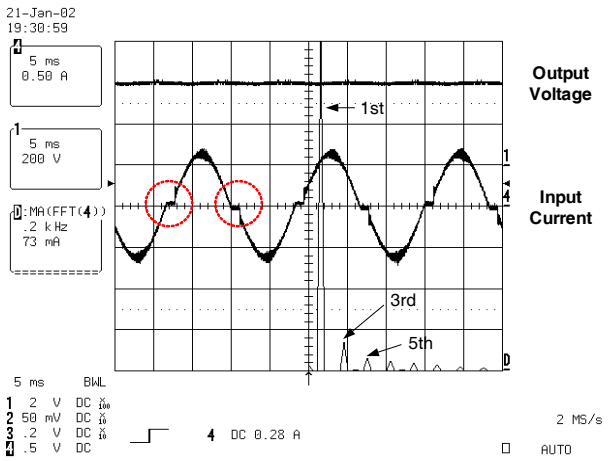


Figure 18. Zero Crossing Distortion

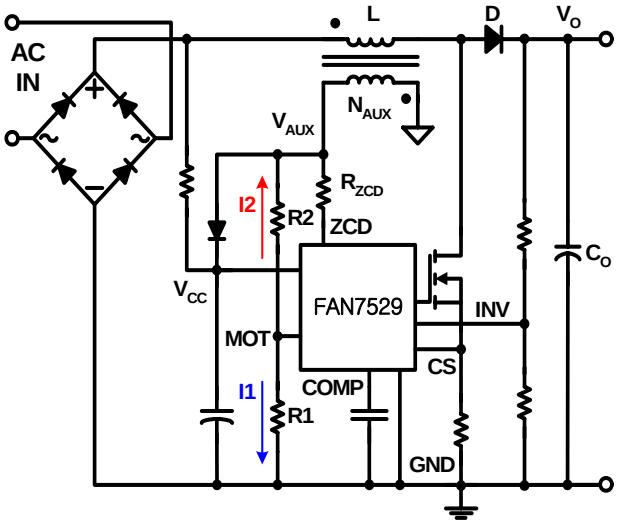


Figure 19. Zero Crossing Improvement Circuit

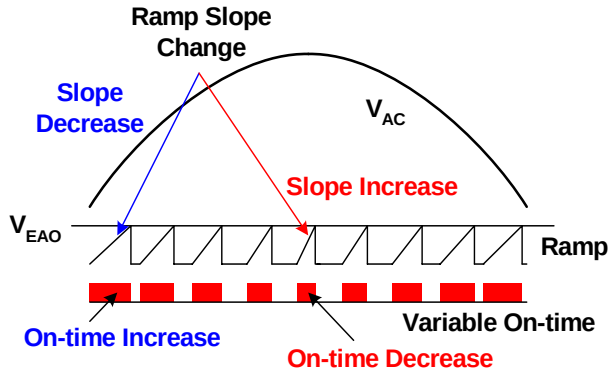


Figure 20. On-Time Variation According to V_{AC}

3) Start-up Circuit Design

To start up the FAN7530, the start-up current must be supplied through a start-up resistor. The resistor value is calculated by Equations 26 and 27. The start-up capacitor must supply IC operating current before the auxiliary winding supplies IC operating current, maintaining V_{CC} voltage higher than the UVLO voltage. The start-up capacitor is determined by Equation 28.

$$R_{ST} \le \frac{V_{in(peak\_min)} - V_{th(st)max}}{I_{ST\,max}} \quad (26)$$

$$P_{R_{ST}} = \frac{V_{in(rms\_max)}^2}{R_{ST}} \le 1W \quad (27)$$

$$C_{ST} \ge \frac{I_{dcc}}{2\pi \cdot f_{ac} \cdot HY_{(ST)min}} \quad (28)$$

4) Current Sense Resistor Design

The CS pin voltage is highest when the AC line voltage is lowest and the output power is maximum. The current sense resistor is determined by Equations 29 and 31, limiting the power loss of the resistor to under 1W.

$$R_{sense} < \frac{0.8V}{I_{L(peak\_max)}} = 0.8V \frac{\eta \cdot V_{in(peak\_min)}}{4 \cdot V_o \cdot I_{o(max)}} \quad (29)$$

$$P_{R_{sense}} = 2 \cdot \left(\frac{V_o \cdot I_{o(max)}}{\eta \cdot V_{in(peak\_min)}} \right)^2 \cdot R_{sense} < 1W \quad (30)$$

$$R_{sense} < \frac{1}{2} \cdot \left(\frac{\eta \cdot V_{in(peak\_min)}}{V_o \cdot I_{o(max)}} \right)^2 \quad (31)$$

4. Design Example

A 100W converter is used here to illustrate the design procedure using a design spreadsheet. Enter the system parameters in the file to get the designed parameters. The system parameters are as follows:

- Maximum output power 100W
- Input voltage range 90Vrms~264Vrms
- Output voltage 392V
- AC line frequency 60Hz
- PFC efficiency 90%
- Minimum switching frequency 37kHz
- Input displacement factor (IDF) 0.98
- Input capacitor ripple voltage 24V
- Output voltage ripple 8V

4.1 Inductor Design

The boost inductor is determined by Equation 6. Calculate it at both the lowest voltage and the highest voltage of the AC line and choose the lower value. The calculated value in this example is 403µH. To get the calculated inductor value, EI30 core is used and the primary winding is 44 turns. The air gap is 0.6mm at both legs of the EI core. The auxiliary winding number, determined by Equation 7, is five; but if more windings are used, the number is six.

4.2 Input Capacitor Design

The minimum input capacitance is determined by the input voltage ripple specification. The calculated minimum input capacitor value is 0.33µF. The maximum input capacitance is restricted by the IDF. The calculated value is 0.77µF. The selected value is 0.63µF (sum of all the capacitors connected to the input side, C1, C2, C3, C4, and C5).

4.3 Output Capacitor Design

The minimum output capacitor is determined by Equation 14 and the calculated value is 85µF. The selected value for the capacitor is 100µF.

4.4 MOSFET and Diode Selection

By calculating Equations 15-19, a 500V/13A MOSFET FQPF13N50C is selected, and a 600V/1A diode BYV26C is selected by the result of Equations 20-21.

4.5 Output Voltage Sense Resistor and Feedback Loop Design

The upper output voltage sense resistor is chosen to be 2MΩ and the bottom output voltage sense resistor is 12.6kΩ. The error amplifier compensation capacitance must be larger than 0.1µF, as calculated by Equation 23. Therefore, 0.22µF capacitor is used.

4.6 Zero Current Detection Resistor Design

The calculated value is 3.1kΩ and the selected value is 20kΩ. A 47pF ceramic capacitor is connected between the ZCD pin and the ground to increase the delay time for the MOSFET minimum voltage turn-on.

4.7 Start-up Circuit Design

The maximum start-up resistor is 1.63MΩ and the minimum is 140kΩ, as determined by Equations 26-27. The selection is 330kΩ. The V_{CC} capacitance must be larger than 7µF, calculated by Equation 28, so the selected value is 47µF.

4.8 Current Sense Resistor Design

The maximum current sense resistance is 0.23Ω as a result of Equation 31 and the selected value is 0.2Ω.

4.9 MOT Resistor Design

The MOT resistor is determined to get the maximum on-time when the AC line voltage is lowest and the output power is maximum. The calculated value is 20.44kΩ and the maximum on-time is 12.26µs. To improve THD performance, a 33kΩ resistor is used for the MOT resistor and a 370kΩ resistor is connected between the MOT pin and the auxiliary winding. The maximum on-time is determined by Equation 32 and the MOT resistor is determined by Equation 33.

$$MOT = \frac{2 \cdot L \cdot P_o}{\eta \cdot V_{in(rms\_min)}^2} \cdot 10^{-6} \quad (32)$$

$$R_{MOT} > \frac{MOT}{600} \times 10^{12} \quad (33)$$

4.10 MOSFET Gate Drive Resistor Design

As shown in Figure 21, noise voltage can be added to the internal ramp signal during MOSFET turn-on. Because of this noise, the AC line current waveform can be distorted if the error amplifier output voltage is close to 1V. It is recommended to use higher resistor for MOSFET turn-on if there is waveform distortion and use a turn-off diode to speed up the turn-off process.

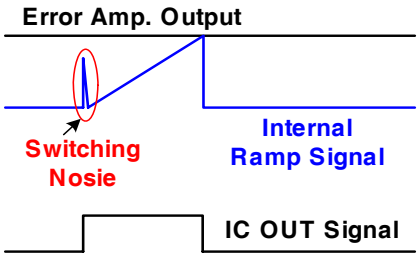


Figure 21. Turn-on Noise on Internal Ramp Signal

Figure 22 shows the designed application circuit diagram and Table 2 shows the 100W demo board components list.

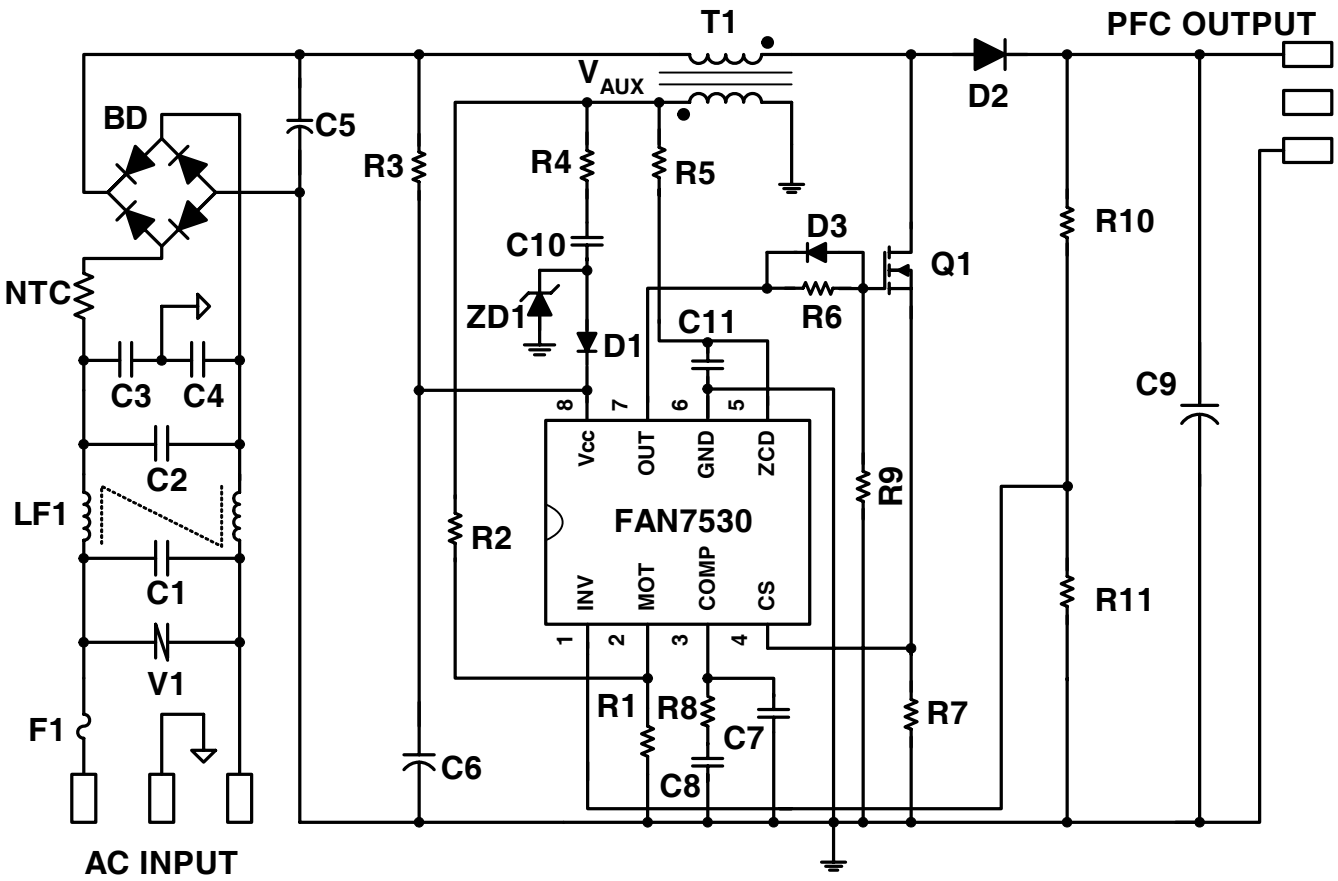


Figure 22. Application Circuit Schematic

Table 2. 100W Demo Board Part List

PART#	VALUE	NOTE	PART#	VALUE	NOTE
Fuse			Capacitor		
F1	250V/3A		C1	150nF/275V_{AC}	Box Capacitor
TNR			C2	470nF/275V_{AC}	Box Capacitor
V1	471	470V	C3,C4	2.2nF/3kV	Ceramic Capacitor
NTC			C6	22μF/25V	Electrolytic Capacitor
RT1	10D-9		C7	47nF/50V	Ceramic Capacitor
Resistor			C8	220nF	MLCC
R1	42kΩ	1/4W	C9	100μF/450V	Electrolytic Capacitor
R2	370kΩ	1/4W	C10	12nF/100V	Film Capacitor
R3	330kΩ	1/2W	C11	47pF/50V	Ceramic Capacitor
R4	150Ω	1/2W	Diode		
R5	20kΩ	1/4W	BD	KBL06	Fairchild
R6	100Ω	1/4W	D1	1N4148	Fairchild
R7	0.2Ω	1/2W	D2	BYV26C	600V/1A
R8	10kΩ	1/4W	D3	SB140	Fairchild
R9	10kΩ	1/4W	ZD1	1N4746	Fairchild
R10	2MΩ	1/4W	Inductor		
R11	12.6kΩ	1/4W	T1	400μH(44T:6T)	EI3026
IC			Primary: 0.2ϕ*10, from Pin 5 to Pin 3		
IC1	FAN7530		Secondary: 0.2ϕ, from Pin 2 to Pin 4		
Line Filter			MOSFET		
LF1	38mH	Wire 0.45mm	Q1	FQPF13N50C	500V/13A

Table 3. Performance Data

		90V_{AC}	**110V_{AC}**	**220V_{AC}**	**264V_{AC}**
100W	PF	0.999	0.998	0.991	0.985
	THD	3.97%	4.43%	5.25%	5.47%
	Efficiency	90.3%	92.7%	94.7%	95.2%
50W	PF	0.998	0.997	0.974	0.956
	THD	4.81%	5.28%	6.74%	7.67%
	Efficiency	90.1%	90.8%	91.7%	92.5%

Table 4. 200W Demo Board Part List (600µH, Wide Input Range Application)

PART#	VALUE	NOTE	PART#	VALUE	NOTE
Fuse			Capacitor		
F1	250V/5A		C1	470nF/275V_{AC}	Box Capacitor
TNR			C2	470nF/275V_{AC}	Box Capacitor
V1	471	470V	C3,C4	2.2nF/3kV	Ceramic Capacitor
NTC			C6	47µF/25V	Electrolytic Capacitor
RT1	10D-9		C7	47nF/50V	Ceramic Capacitor
Resistor			C8	220nF	MLCC
R1	37kΩ	1/4W	C9	220µF/450V	Electrolytic Capacitor
R2	250kΩ	1/4W	C10	12nF/100V	Film Capacitor
R3	330kΩ	1/2W	C11	47pF/50V	Ceramic Capacitor
R4	150Ω	1/2W	Diode		
R5	20kΩ	1/4W	BD	KBU8K	Fairchild
R6	100Ω	1/4W	D1	1N4148	Fairchild
R7	0.1Ω	1W	D2	SUF30J	600V/3A
R8	10kΩ	1/4W	D3	SB140	Fairchild
R9	10kΩ	1/4W	ZD1	1N4746	Fairchild
R10	2MΩ	1/4W	Inductor		
R11	12.6kΩ	1/4W	T1	200µH(30T:3T)	PQ3230
IC			Primary: 0.1ϕ*100, from Pin 5 to Pin 3		
IC1	FAN7530		Secondary: 0.2ϕ, from Pin 2 to Pin 4		
Line Filter			MOSFET		
LF1	22mH	Wire 0.7mm	Q1	FDPF20N50	Fairchild

Table 5. Performance Data

		85V_{AC}	**115V_{AC}**	**230V_{AC}**	**265V_{AC}**
200W	PF	0.999	0.998	0.993	0.990
	THD	3.8%	4.3%	6.5%	6.5%
	Efficiency	91.8%	94.8%	96.9%	97.3%
150W	PF	0.999	0.998	0.990	0.985
	THD	4.7%	5.2%	7.0%	6.9%
	Efficiency	93.3%	95.5%	96.9%	97.0%
100W	PF	0.997	0.996	0.981	0.971
	THD	6.5%	7.4%	9.0%	8.5%
	Efficiency	94.3%	95.3%	96.2%	96.0%

Table 6. 300W Wide Input Range Application Part List

PART#	VALUE	NOTE	PART#	VALUE	NOTE
Fuse			Capacitor		
F1	250V/5A		C1	680nF/275V_{AC}	Box Capacitor
TNR			C2	680nF/275V_{AC}	Box Capacitor
V1	471	470V	C3,C4	2.2nF/3kV	Ceramic Capacitor
NTC			C6	47μF/25V	Electrolytic Capacitor
RT1	6D-22		C7	33nF/50V	Ceramic Capacitor
Resistor			C8	220nF	MLCC
R1	60kΩ	1/4W	C9	33μF/450V	Electrolytic Capacitor
R2	330kΩ	1/4W	C10	12nF/100V	Film Capacitor
R3	330kΩ	1/2W	C11	9pF/50V	Ceramic Capacitor
R4	100Ω	1/2W	Diode		
R5	20kΩ	1/4W	BD	KBU8J	Fairchild
R6	100Ω	1/4W	D1	1N4148	Fairchild
R7	0.06Ω	1W	D2	SUF30J	600V/3A
R8	10kΩ	1/4W	D3	SB140	Fairchild
R9	10kΩ	1/4W	ZD1	1N4746	Fairchild
R10	2MΩ	1/4W	Inductor		
R11	12.6kΩ	1/4W	T1	200μH(36T:3T)	PQ3535
IC			Primary: 0.1ϕ, *100, from Pin 5 to Pin 3		
IC1	FAN7530		Secondary: 0.2ϕ, from Pin 2 to Pin 4		
Line Filter			MOSFET		
LF1	40mH	Wire 1mm	Q1	FQA28N50	Fairchild

Table 7. Performance Data

		85V_{AC}	**115V_{AC}**	**230V_{AC}**	**265V_{AC}**
300W	PF	0.999	0.998	0.993	0.988
	THD	4.5%	4.7%	6.4%	6.5%
	Efficiency	91.4%	94.5%	97.4%	97.7%
225W	PF	0.999	0.998	0.989	0.982
	THD	3.9%	4.7%	6.1%	6.2%
	Efficiency	92.8%	95.1%	97.4%	97.7%
150W	PF	0.998	0.997	0.978	0.963
	THD	4.8%	5.8%	7.4%	7.4%
	Efficiency	94.0%	95.7%	97.0%	97.3%
75W	PF	0.994	0.989	0.929	0.885
	THD	9.3%	10.8%	11.2%	12.0%
	Efficiency	94.8%	95.9%	95.3%	95.2%

Nomenclature

C_{comp}: compensation capacitance

C_{IN}: input capacitance

C_{OUT}: output capacitance

C_{ST}: start-up capacitance

f_{ac}: AC line frequency

$f_{sw(max)}$: maximum switching frequency

$f_{sw(min)}$: minimum switching frequency

f_{sw}: switching frequency

$HY_{(ST)\ min}$: minimum UVLO hysteresis

I_D: boost diode current

I_{Davg}: diode average current

I_{Drms}: diode RMS current

$I_{in\ (peak)}$: input current peak value

$I_{in\ (peak\_max)}$: maximum of the input current peak value

$I_{in\ (rms)}$: input current RMS value

I_{in} (t): input current

I_L (t): inductor current

$I_{L(peak)}$ (t): inductor current peak value during one switching cycle

$I_{L(peak)}$: inductor current peak value during one AC line cycle

$I_{L(peak\_max)}$: maximum inductor current peak value

$I_{O\ (max)}$: maximum output current

I_O: output current

I_{Qrms}: MOSFET RMS current

I_{STmax}: maximum start-up supply current

L: boost inductance

N_{aux}: auxiliary winding turn number

N_P: boost inductor turn number

P_{in}: input power

$P_{O(max)}$: maximum output power

P_O: output power

R_{sense}: current sense resistance

R_{ST}: start-up resistance

R_{zcd}: zero current detection resistance

t_f: MOSFET current falling time

t_{off}: switch off time

t_{on}: switch on time

T_S: switching period

$V_{in\ (peak)}$: input voltage peak value

$V_{in\ (peak\_low)}$: input voltage peak value at low line

$V_{in\ (peak\_max)}$: maximum input voltage peak value

$V_{in\ (peak\_min)}$: minimum input voltage peak value

$V_{in\ (rms)}$: input voltage RMS value

$V_{in\ (rms\_max)}$: maximum input voltage RMS value

$V_{in\ (rms\_min)}$: minimum input voltage RMS value

V_{in} (t): input voltage

V_O or V_{OUT}: output voltage

$\Delta V_{in\ (max)}$: maximum input voltage ripple

$\Delta V_{O\ (max)}$: maximum output voltage ripple

η: converter efficiency

ω: AC line angular frequency