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1. Overview

The M16C/29 group of single-chip microcomputers is built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core and is packaged in a 64-pin and 80-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. They also contain a CAN module, makes it suitable for control of cars and LAN system of FA. In addition, they contain a multiplier and a DMAC, also making it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

1.1 Applications

Automotive body, safety & audio, LAN system of FA, etc.

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

1.2 Performance Outline

Table 1.2.1 lists performance outline of M16C/29 group 80-pin device.

Table 1.2.2 lists performance outline of M16C/29 group 64-pin device.

Table 1.2.1. Performance outline of M16C/29 group (80-pin device)

Item		Performance
CPU	Number of basic instructions	91 instructions
	Shortest instruction excution time	50 ns (f(BCLK)= 20MHz, Vcc= 3.0V to 5.5V) (Normal-ver./T-ver.) 100 ns (f(BCLK)= 10MHz, Vcc= 2.7V to 5.5V) (Normal-ver.) 50 ns (f(BCLK)= 20MHz, Vcc= 4.2V to 5.5V -40 to 105°C) (V-ver.) 62.5 ns (f(BCLK)= 16MHz, Vcc= 4.2V to 5.5V -40 to 125°C) (V-ver.)
	Operation mode	Single chip mode
	Address space	1M bytes
	Memory capacity	ROM/RAM : See the product list
Peripheral function	port	Input/Output : 71 lines
	Multifunction timer	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer TimerS (Input Capture/Output Compare) : 16bit base timer x 1 channel (Input/Output x 8 channels)
	Serial I/O	2 channels (UART0, UART1) UART, clock synchronous 1 channel (UART2) UART, clock synchronous, I2C bus1, or IEbus2 2 channels (SI/O3, SI/O4) Clock synchronous 1 channel (Multi-Master I2C bus1)
	A/D converter	10 bits x 27 channels
	DMAC	2 channels
	CRC calcuration circuit	2 polynomial (CRC-CCITT and CRC-16) with MSB/LSB selectable
	CAN module	1 channel 2.0B BOSCH compliant
	Watchdog timer	15 bits x 1 (with prescaler)
	Interrupt	28 internal and 8 external sources, 4 software sources, 7 levels
	Clock generation circuit	4 circuits • Main clock } (These circuits contain a built-in feedback resistor and external ceramic/quartz oscillator) • Sub-clock } • On-chip oscillator(main-clock oscillation stop detect function) • PLL frequency synthesizer
	Low voltage detection circuit	Available (Normal-ver.) Not available (T-ver./V-ver.)
Electrical Characteristics	Power supply voltage	Vcc=3.0V to 5.5V (f(BCLK)=20MHz) (Normal-ver.) Vcc=2.7V to 5.5V (f(BCLK)=10MHz)
		Vcc=3.0V to 5.5V (T-ver.)
		Vcc=4.2V to 5.5V (V-ver.)
	Power consumption	18mA (Vcc=5V, f(BCLK)=20MHz) 25 µA (Vcc=5V, f(BCLK)=f(XCIN)=32KHz on RAM) 1.8 µA (Vcc=5V, f(BCLK)=f(XCIN)=32KHz, in wait mode) 0.8 µA (Vcc=5V, when stop mode)
Flash memory	Program/erase voltage	2.7V to 5.5V (Normal-ver.) 3.0V to 5.5V (T-ver.) 4.2V to 5.5V (V-ver.)
	Number of program/erase	100 times (Block A ,Block B : 10,000 times (option3))
Operating ambient temperature		-20 to 85°C / -40 to 85°C (option3) (Normal-ver.)
		-40 to 85°C (T-ver.) -40 to 125°C (V-ver.)
Package		80-pin plastic mold QFP

Notes:
1. I2C bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. If you desire this option, please so specify.

Table 1.2.2. Performance outline of M16C/29 group (64-pin device)

Item		Performance
CPU	Number of basic instructions	91 instructions
	Shortest instruction excution time	50 ns (f(BCLK)= 20MHz, Vcc= 3.0V to 5.5V) (Normal-ver./T-ver.) 100 ns (f(BCLK)= 10MHz, Vcc= 2.7V to 5.5V) (Normal-ver.) 50 ns (f(BCLK)= 20MHz, Vcc= 4.2V to 5.5V -40 to 105°C) (V-ver.) 62.5 ns (f(BCLK)= 16MHz, Vcc= 4.2V to 5.5V -40 to 125°C) (V-ver.)
	Operation mode	Single chip mode
	Address space	1M bytes
	Memory capacity	ROM/RAM : See the product list
Peripheral function	port	Input/Output : 55 lines
	Multifunction timer	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer TimerS (Input Capture/Output Compare) : 16bit base timer x 1 channel (Input/Output x 8 channels)
	Serial I/O	2 channels (UART0, UART1) UART, clock synchronous 1 channel (UART2) UART, clock synchronous, I2C bus1, or IEbus2 1 channel (SI/O3) Clock synchronous 1 channel (Multi-Master I2C bus1)
	A/D converter	10 bits x 16 channels
	DMAC	2 channels
	CRC calcuration circuit	2 polynomial (CRC-CCITT and CRC-16) with MSB/LSB selectable
	CAN module	1 channel 2.0B BOSCH compliant
	Watchdog timer	15 bits x 1 (with prescaler)
	Interrupt	28 internal and 8 external sources, 4 software sources, 7 levels
	Clock generation circuit	4 circuits • Main clock, • Sub-clock (These circuits contain a built-in feedback resistor and external ceramic/quartz oscillator) • On-chip oscillator(main-clock oscillation stop detect function) • PLL frequency synthesizer
	Low voltage detection circuit	Available (Normal-ver.) Not available (T-ver./V-ver.)
Electrical Characteristics	Power supply voltage	Vcc=3.0V to 5.5V (f(BCLK)=20MHz) (Normal-ver.) Vcc=2.7V to 5.5V (f(BCLK)=10MHz)
		Vcc=3.0V to 5.5V (T-ver.)
		Vcc=4.2V to 5.5V (V-ver.)
	Power consumption	18mA (Vcc=5V, f(BCLK)=20MHz) 25 µA (Vcc=5V, f(BCLK)=f(XCIN)=32KHz on RAM) 1.8 µA (Vcc=5V, f(BCLK)=f(XCIN)=32KHz, in wait mode) 0.8 µA (Vcc=5V, when stop mode)
Flash memory	Program/erase voltage	2.7V to 5.5V (Normal-ver.) 3.0V to 5.5V (T-ver.) 4.2V to 5.5V (V-ver.)
	Number of program/erase	100 times (Block A ,Block B : 10,000 times (option3))
Operating ambient temperature		-20 to 85°C / -40 to 85°C (option3) (Normal-ver.)
		-40 to 85°C (T-ver.) -40 to 125°C (V-ver.)
Package		64-pin plastic mold QFP

Notes:
1. I2C bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. If you desire this option, please so specify.

1.3 Block Diagram

Figure 1.3.1 is a block diagram of the M16C/29 group, 80-pin device.

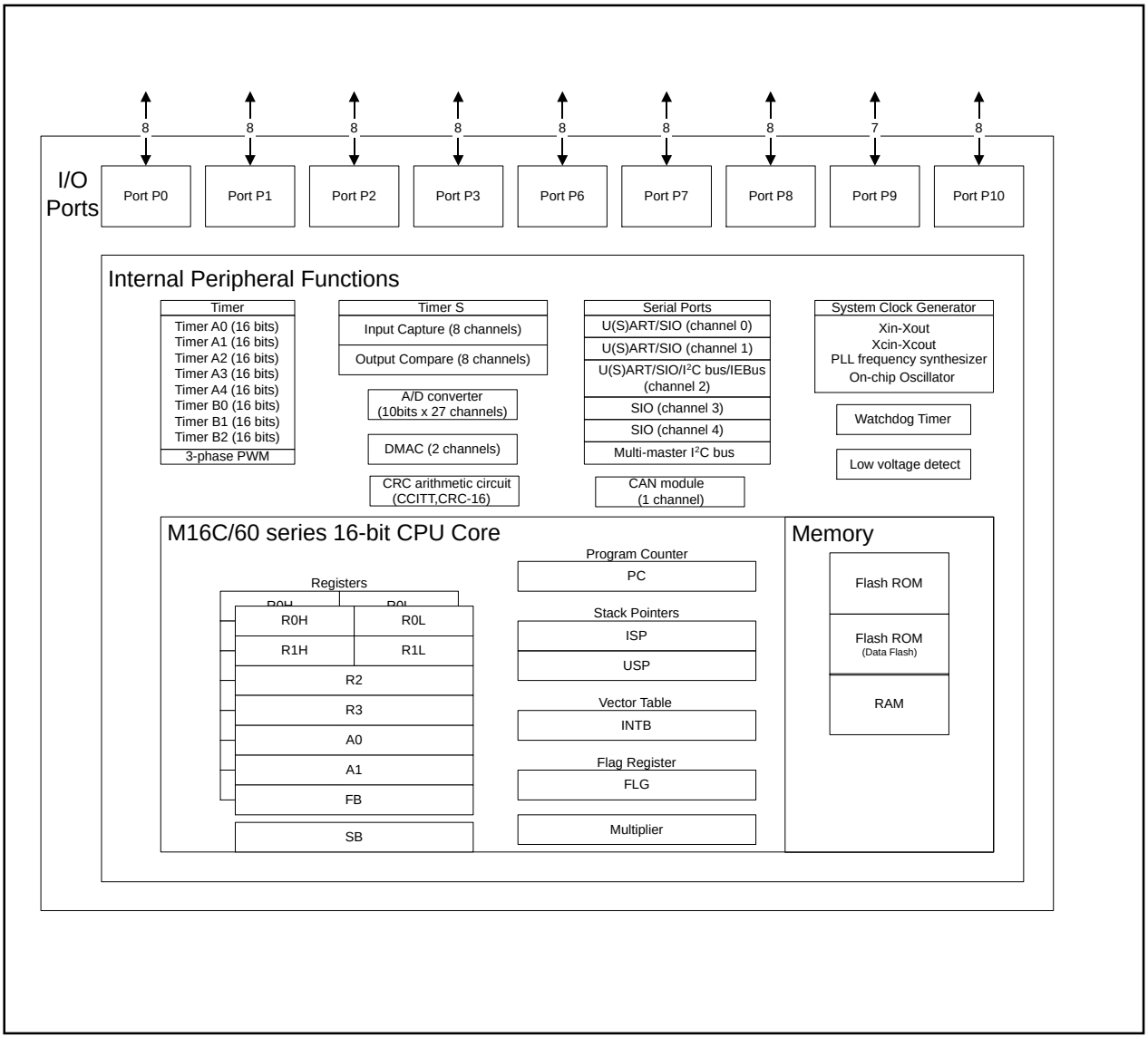


Figure 1.3.1. M16C/28 Group, 80-pin Block Diagram

Figure 1.3.2 is a block diagram of the M16C/29 group, 64-pin device.

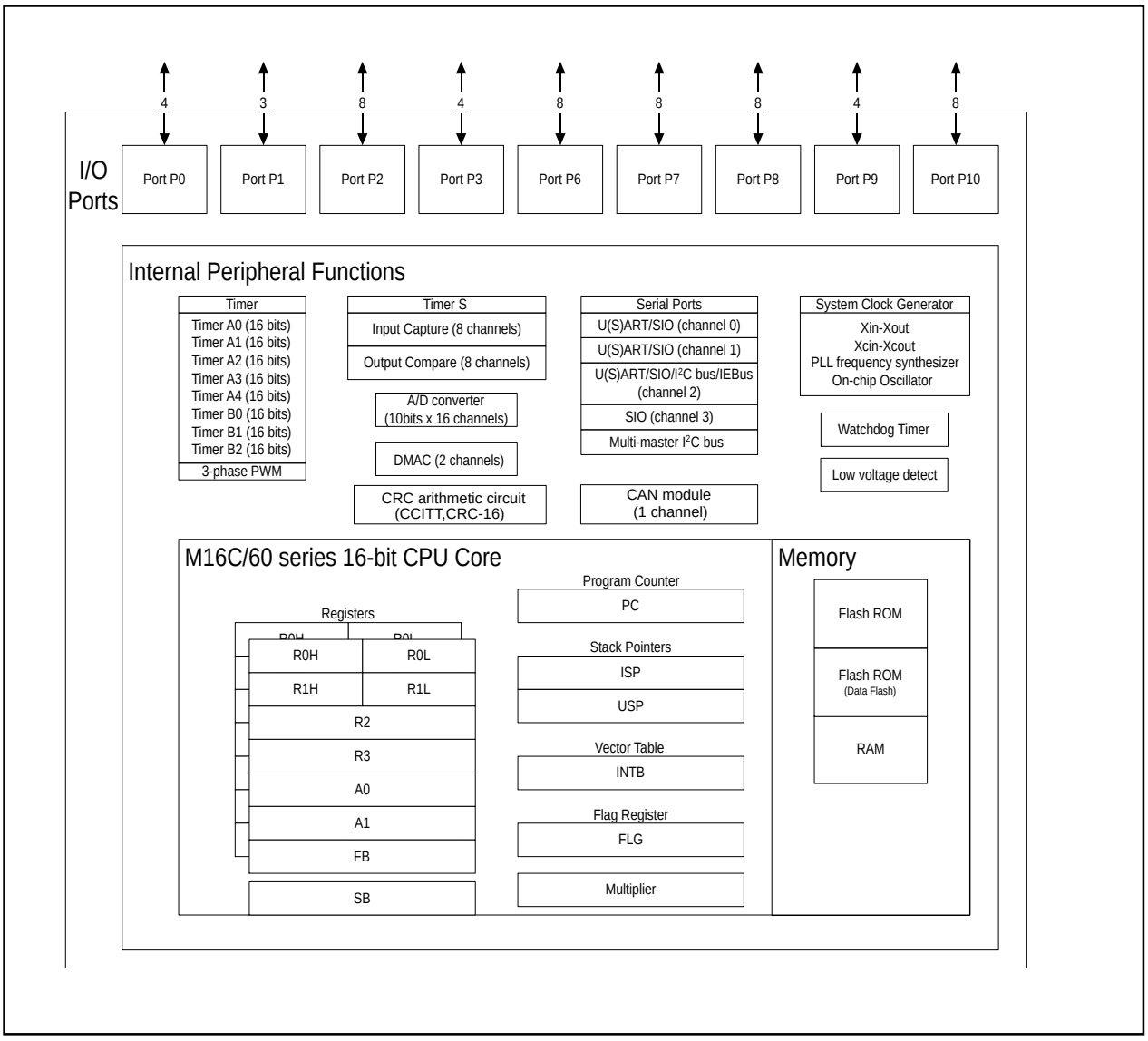


Figure 1.3.2. M16C/28 Group, 64-pin Block Diagram

1.4 Product List

Tables 1.4.1 to 1.4.3 list the M16C/29 group products and Figure 1.4.1 shows the type numbers, memory sizes and packages.

Table 1.4.1. Product List (1) -Normal-ver. **As of Jun 2004**

Type No.		ROM capacity	RAM capacity	Package type	Remarks
M30290F8HP	(P)	64K + 4K byte	4K byte	80P6Q-A	Flash ROM Version
M30290FAHP	(D)	96K + 4K byte	8K byte		
M30290FCHP	(D)	128K + 4K byte	12K byte		
M30291F8HP	(P)	64K + 4K byte	4K byte	64P6Q-A	
M30291FAHP	(D)	96K + 4K byte	8K byte		
M30291FCHP	(D)	128K + 4K byte	12K byte		
M30290M8-XXXHP	(P)	64K byte	4K byte	80P6Q-A	Mask ROM Version
M30290MA-XXXHP	(P)	96K byte	8K byte		
M30290MC-XXXHP	(P)	128K byte	12K byte		
M30291M8-XXXHP	(P)	64K byte	4K byte	64P6Q-A	
M30291MA-XXXHP	(P)	96K byte	8K byte		
M30291MC-XXXHP	(P)	128K byte	12K byte		

(P) : under planning (D) : under development

Table 1.4.2. Product List (2) -T-ver. **As of Jun 2004**

Type No.		ROM capacity	RAM capacity	Package type	Remarks
M30290F8THP	(P)	64K + 4K byte	4K byte	80P6Q-A	Flash ROM Version
M30290FATHP	(D)	96K + 4K byte	8K byte		
M30290FCTHP	(D)	128K + 4K byte	12K byte		
M30291F8THP	(P)	64K + 4K byte	4K byte	64P6Q-A	
M30291FATHP	(D)	96K + 4K byte	8K byte		
M30291FCTHP	(D)	128K + 4K byte	12K byte		
M30290M8T-XXXHP	(P)	64K byte	4K byte	80P6Q-A	Mask ROM Version
M30290MAT-XXXHP	(P)	96K byte	8K byte		
M30290MCT-XXXHP	(P)	128K byte	12K byte		
M30291M8T-XXXHP	(P)	64K byte	4K byte	64P6Q-A	
M30291MAT-XXXHP	(P)	96K byte	8K byte		
M30291MCT-XXXHP	(P)	128K byte	12K byte		

(P) : under planning (D) : under development

NOTES: Specification of T-ver. partly varies from the one of Normal-ver.

Table 1.4.3. Product List (3) -V-ver. **As of Jun 2004**

Type No.		ROM capacity	RAM capacity	Package type	Remarks
M30290F8VHP	(P)	64K + 4K byte	4K byte	80P6Q-A	Flash ROM Version
M30290FAVHP	(D)	96K + 4K byte	8K byte		
M30290FCVHP	(D)	128K + 4K byte	12K byte		
M30291F8VHP	(P)	64K + 4K byte	4K byte	64P6Q-A	
M30291FAVHP	(D)	96K + 4K byte	8K byte		
M30291FCVHP	(D)	128K + 4K byte	12K byte		
M30290M8V-XXXHP	(P)	64K byte	4K byte	80P6Q-A	Mask ROM Version
M30290MAV-XXXHP	(P)	96K byte	8K byte		
M30290MCV-XXXHP	(P)	128K byte	12K byte		
M30291M8V-XXXHP	(P)	64K byte	4K byte	64P6Q-A	
M30291MAV-XXXHP	(P)	96K byte	8K byte		
M30291MCV-XXXHP	(P)	128K byte	12K byte		

(P) : under planning (D) : under development

NOTES: Specification of V-ver. partly varies from the one of Normal-ver.

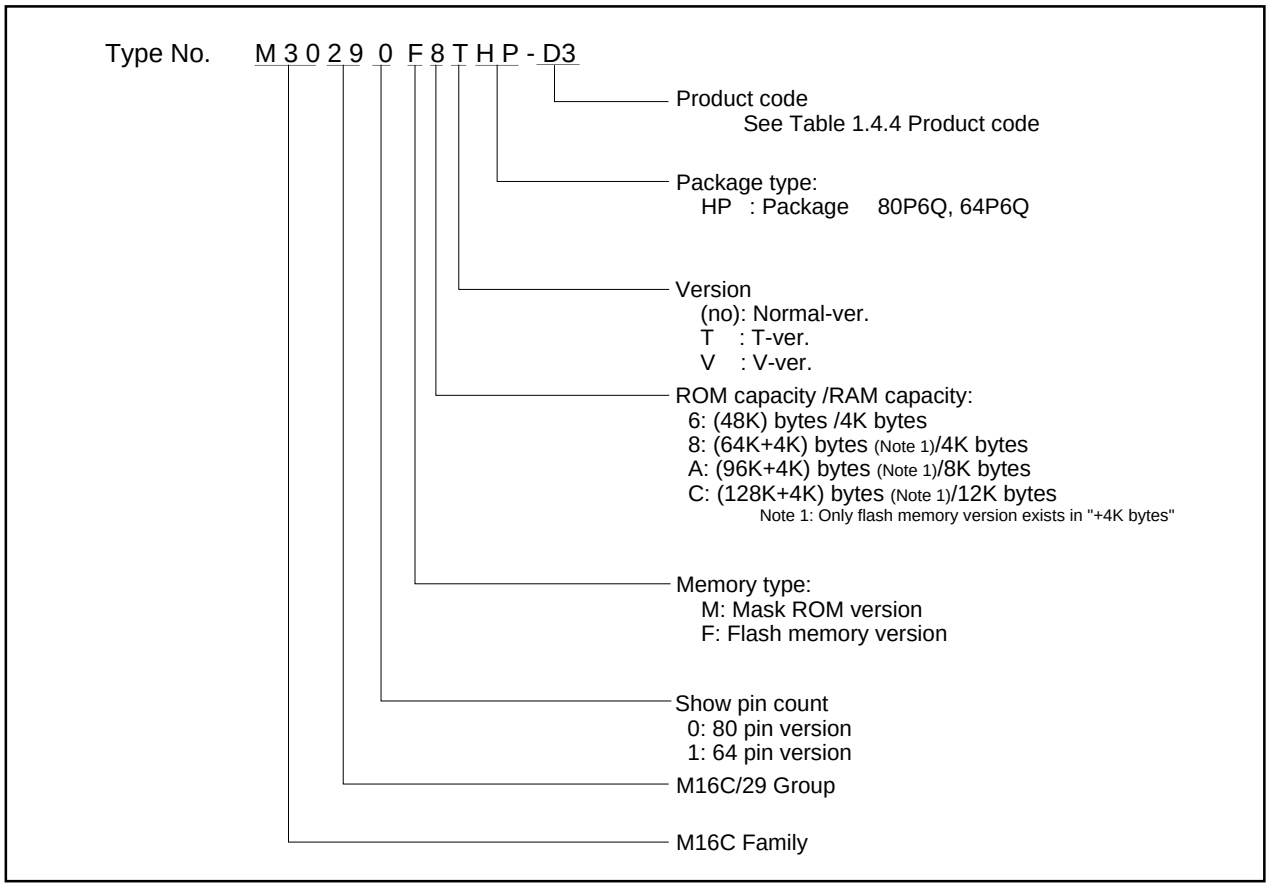


Figure 1.4.1. Type No., Memory Size, and Package

Table 1.4.4. Product code (Flash ROM Version, Normal-ver.)

Product Code	Package	Internal ROM Block (0, 1, 2, 3)		Internal ROM Block (A, B)		Microcomputer operating temperature
		E/W cycles	Temperature range	E/W cycles	Temperature range	
D3	non-LEAD free	100	0°C to 60°C	100	0°C to 60°C	-40°C to 85°C
D5						-20°C to 85°C
D7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
D9					-20°C to 85°C	-20°C to 85°C
U3	LEAD free	100		100	0°C to 60°C	-40°C to 85°C
U5						-20°C to 85°C
U7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
U9					-20°C to 85°C	-20°C to 85°C

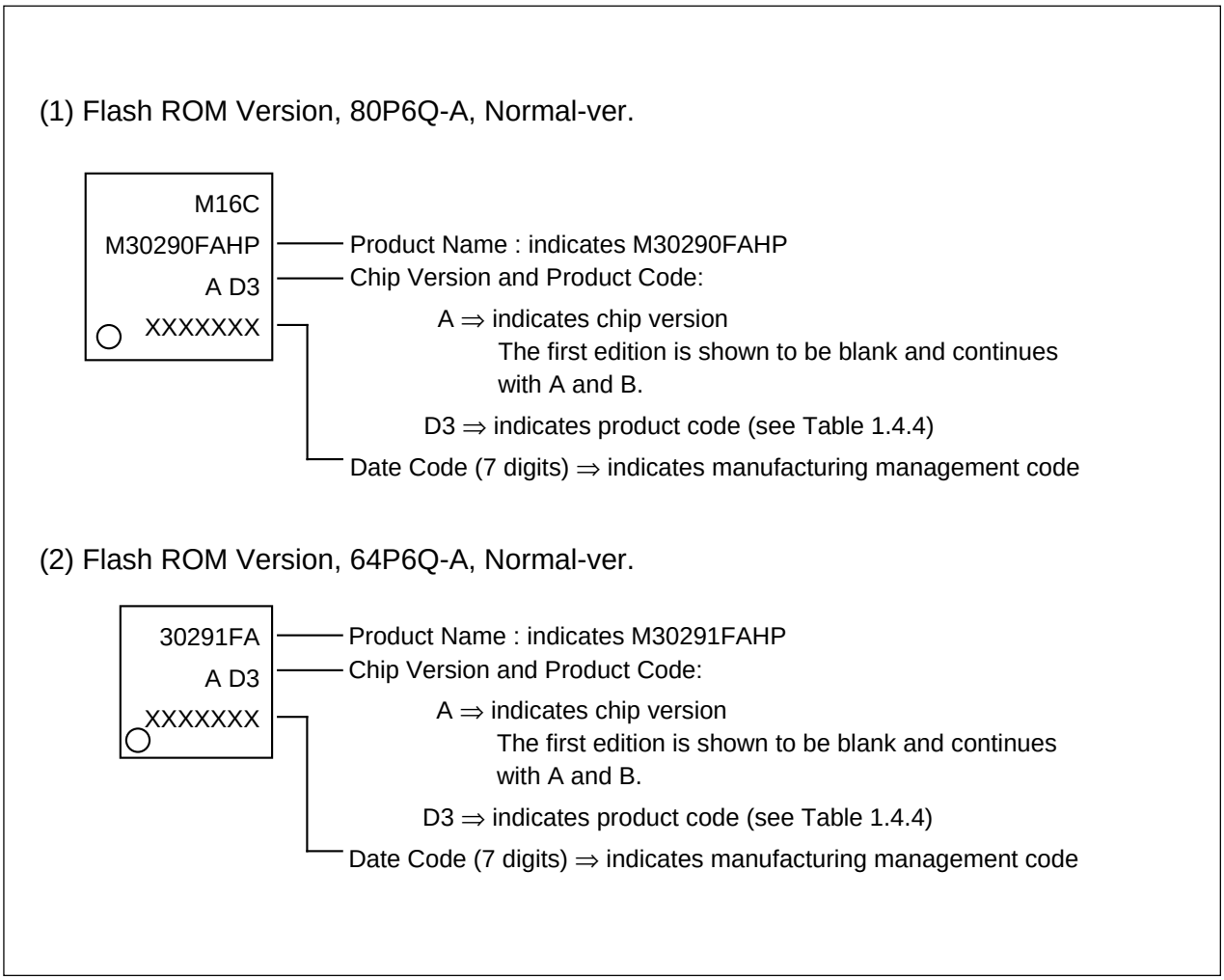


Figure 1.4.2. Marking (Top View)

1.5 Pin Configuration

Figures 1.5.1 and 1.5.2 show the pin configurations (top view).

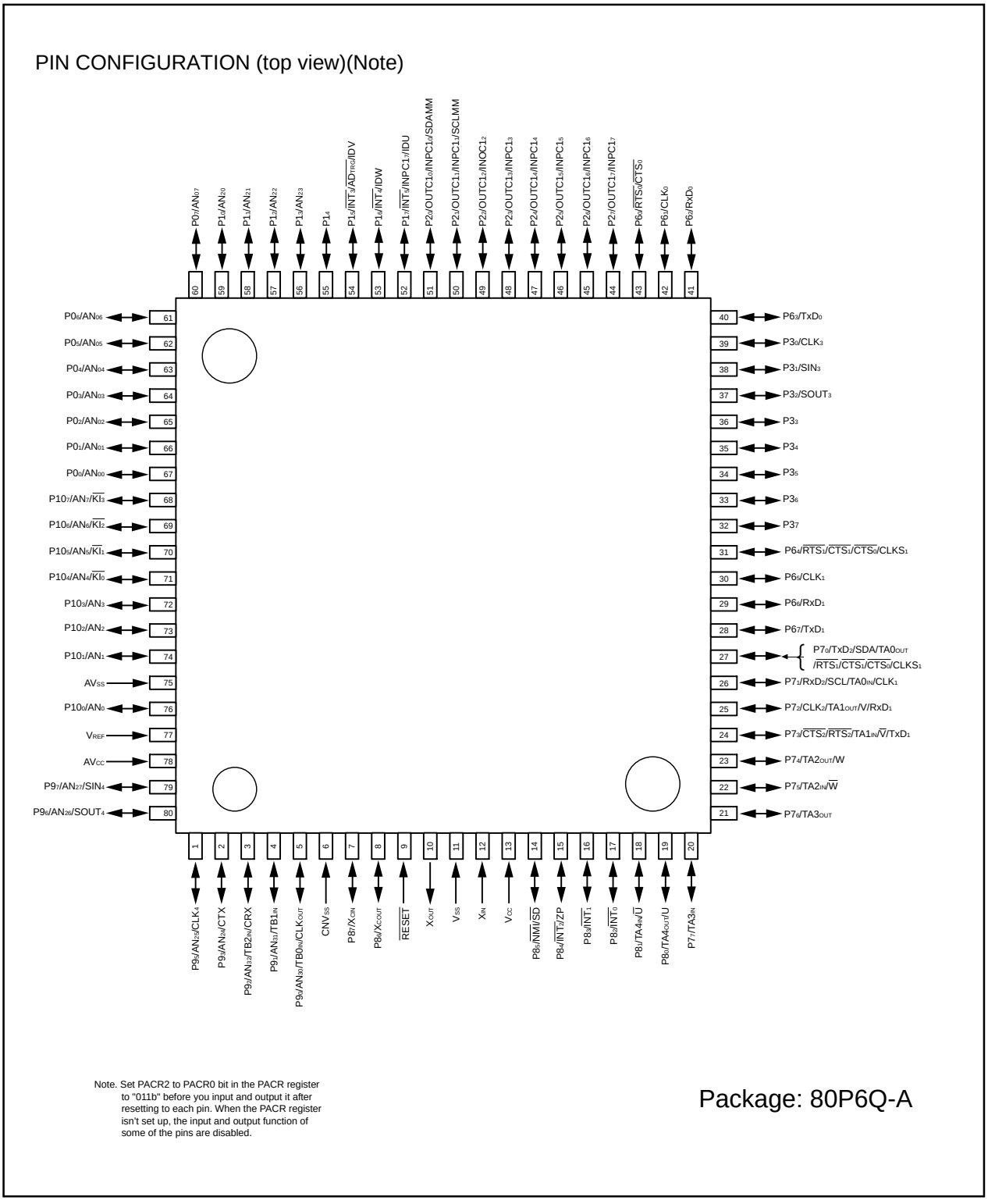
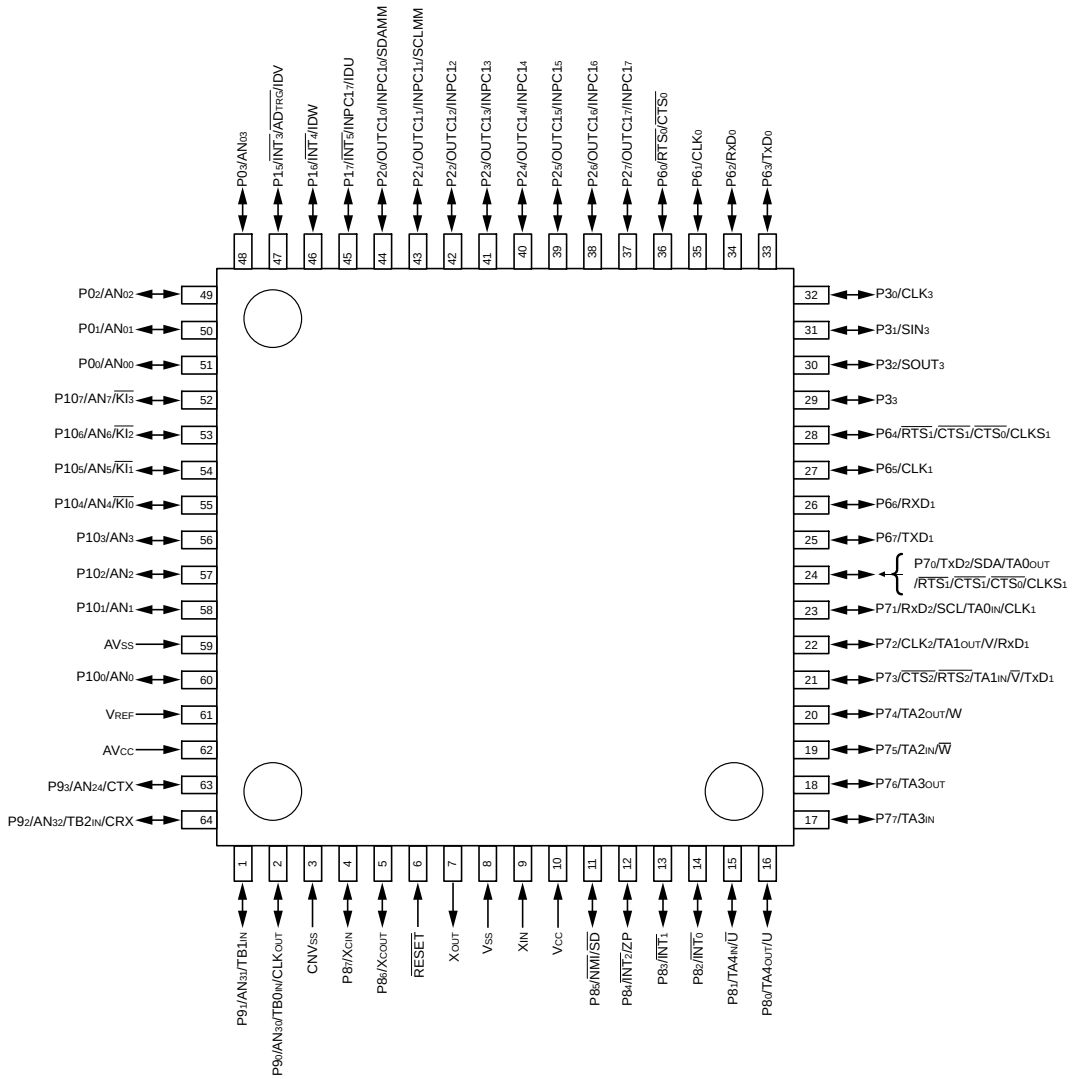


Figure 1.5.1. Pin Configuration (Top View) of M16C/29 Group, 80-pin Package

PIN CONFIGURATION (top view)(Note)



Note. Set PACR2 to PACR0 bit in the PACR register to "010b" before you input and output it afer resetting to each pin. When the PACR register isn't set up, the input and output function of some of the pins are disabled.

Package: 64P6Q-A

Figure 1.5.2. Pin Configuration (Top View) of M16C/29 Group, 64-pin Package

1.6 Pin Description

Table 1.6.1 and 1.6.2 describes the available pins.

Table 1.6.1 Pin Description(1)

Pin Name	Signal name	I/O type	Function
VCC,VSS	Power supply input		Apply 0V to the Vss pin, and the following voltage to the Vcc pin. 2.7 to 5.5V (Normal-ver.) 3.0 to 5.5V (T-ver.) 4.2 to 5.5V (V-ver.)
CNVSS	CNVSS	Input	Connect this pin to Vss.
$\overline{\text{RESET}}$	Reset input	Input	"L" on this input resets the microcomputer.
XIN XOUT	Clock input Clock output	Input Output	These pins are provided for the main clock generating circuit input/ output. Connect a ceramic resonator or crystal between the XIN and the XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open. If XIN is not used (for external oscillator or external clock) connect XIN pin to VCC and leave XOUT pin open.
AVCC	Analog power supply input		This pin is a power supply input for the A/D converter. Connect this pin to VCC.
AVSS	Analog power supply input		This pin is a power supply input for the A/D converter. Connect this pin to VSS.
VREF	Reference Voltage input	Input	This pin is a reference voltage input for the A/D converter.
P00~P07	I/O port P0	Input/Output	This is an 8-bit CMOS I/O port. It has an input/output port direction register that allows the user to set each pin for input or output individually. When used for input, a pull-up register option can be selected for the entire group of four pins. Software can also select this port to function as A/D converter input pins. P04 to P07 is not in 64 pin version.
P10~P17	I/O port P1	Input/Output	This is an 8-bit I/O port equivalent to P0. Additional software selectable secondary functions are: 1) P10 to P13 can act as A/D converter input pins; 2) P15 to P17 can be configured as external interrupt pins; 3) P15 to P17 can be configured as position-data-retain function input pins, and; 4) P15 can input a trigger for the A/D converter. P10 to P14 is not in 64 pin version.
P20~P27	I/O port P2	Input/Output	This is an 8-bit I/O port equivalent to P0. Software can alse select this port to perform as I/O for the Timer S (all pins), and MultiMaster I^2C Bus (P20 to P21 only).
P30~P37	I/O port P3	Input/Output	This is an 8-bit I/O port equivalent to P0. P30 to P32 also function as SIO3 I/O, as selected by software. P34 to P37 is not in 64 pin version.
P60~P67	I/O port P6	Input/Output	This is an 8-bit I/O port equivalent to P0. Pins in this port also function as UART0 and UART1 I/O, as selected by software.

Table 1.6.2 Pin Description(2)

Pin Name	Signal name	I/O type	Function
P7$_0$~P7$_7$	I/O port P7	Input/Output	This is an 8-bit I/O port equivalent to P0. P7 can also function as I/O for timer A0 to A3, as selected by software. Additional programming options are: P7$_0$ to P7$_3$ can assume UART1 or UART2 I/O capabilities, and P7$_2$ to P7$_5$ can function as output pins for the three-phase motor control timer.
P8$_0$~P8$_7$	I/O port P8	Input/Output	This is an 8-bit I/O port equivalent to P0. Additional software selectable secondary functions are: 1) P8$_0$ and P8$_1$ can act as either I/O for Timer A4, as output pins for the three-phase motor control timer; 2) P8$_2$ to P8$_4$ can be configured as external interrupt pins. P8$_4$ can be used for Timer A Zphase function; 3) P8$_5$ can be used as $\overline{\text{NMI}}$/$\overline{\text{SD}}$. P8$_5$ can not be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to P8$_5$ after setting the direction register for P8$_5$ to "0" when the three-phase motor control is enabled, and; 4) P8$_6$ to P8$_7$ can serve as I/O pins for the subclock generation circuit. In this latter case, a quartz oscillator must be connected between P8$_6$ (XCOUT pin) and P8$_7$ (XCIN pin).
P9$_0$~P9$_3$, P9$_5$~P9$_7$	I/O port P9	Input/Output	This is an 7-bit I/O port equivalent to P0. Additional software selectable scondary functions are: 1) P9$_0$ to P9$_2$ can act as Timer B0 to B2 input pins; 2) P9$_0$ to P9$_2$ can act as A/D converter input pins; 3) P9$_0$ outputs a no division, divide-by-8 or divide-by-32 clock of XIN or a clock of the same frequency as XCIN as selected by program; 4) P9$_2$ and P9$_3$ can function as I/O pins fpr the CAN module; 5) P9$_3$, P9$_5$ to P9$_7$ can act as A/D converter input pins, and; 6) P9$_6$ to P9$_7$ can assume SI/O4 I/O. P9$_5$ to P9$_7$ is not in 64 pin version.
P10$_0$~P10$_7$	I/O port P10	Input/Output	This is an 8-bit I/O port equivalent to P0. This port can also function as A/D converter input pins, as selected by software. Furthermore, P10$_4$ to P10$_7$ can also function as input pins for the key input interrupt function.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

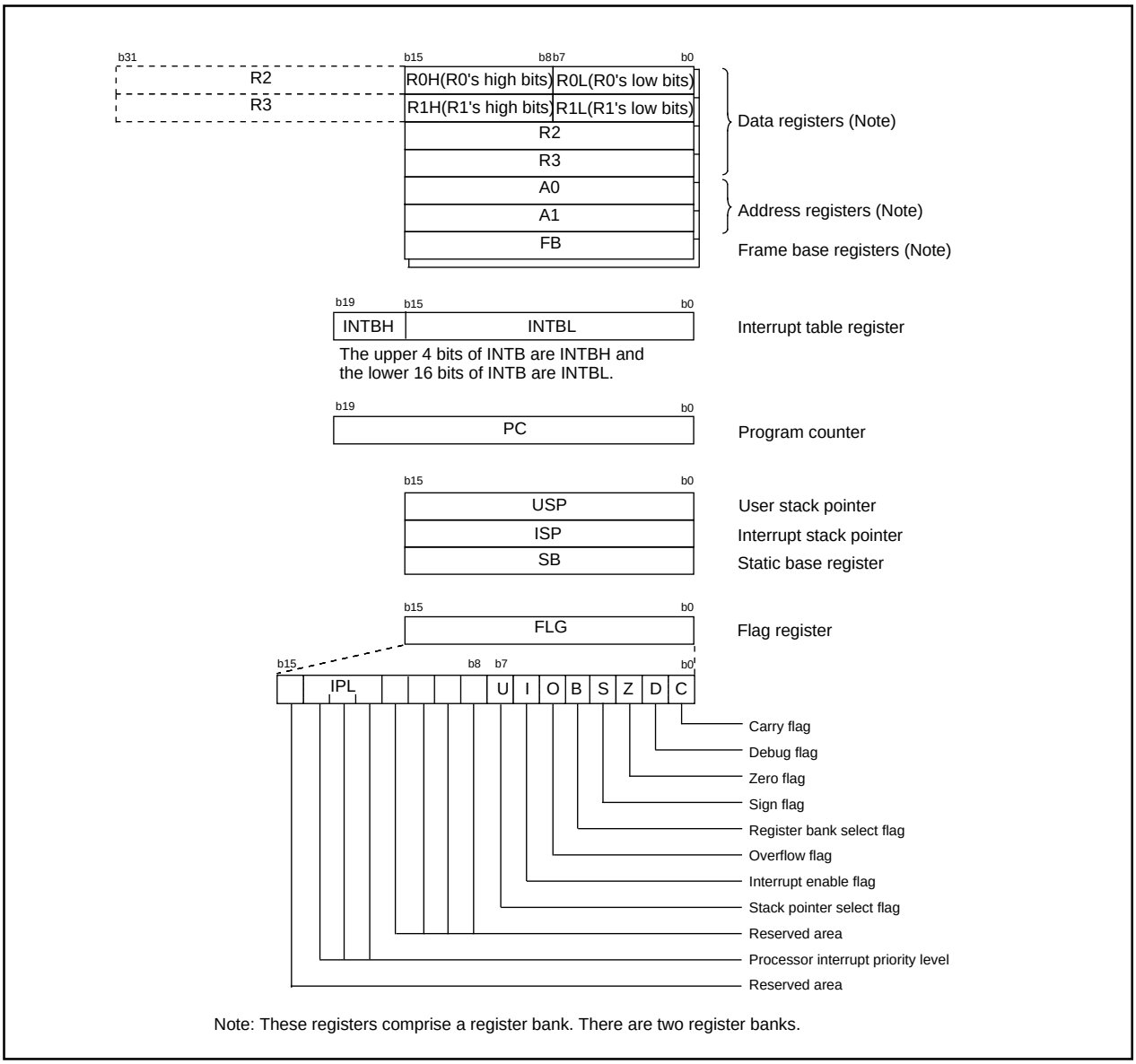


Figure 2.1. Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to “0”.

2.8.3 Zero Flag (Z Flag)

This flag is set to “1” when an arithmetic operation resulted in 0; otherwise, it is “0”.

2.8.4 Sign Flag (S Flag)

This flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, it is “0”.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is “0” ; register bank 1 is selected when this flag is “1”.

2.8.6 Overflow Flag (O Flag)

This flag is set to “1” when the operation resulted in an overflow; otherwise, it is “0”.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is “0”, and are enabled when the I flag is “1”.

The I flag is cleared to “0” when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is “0”; USP is selected when the U flag is “1”.

The U flag is cleared to “0” when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map of the M16C/29 group. The linear address space of 1M bytes extends from address 00000_{16} to $FFFFF_{16}$. From $FFFFF_{16}$ down is ROM. For example, in the M30290F8HP,there are 64 Kbytes of internal ROM from $F0000_{16}$ to $FFFFF_{16}$.

The vector table for fixed interrupts, such as Reset and NMI, is mapped from $FFFDC_{16}$ to $FFFFF_{16}$. The starting address of the interrupt routine is stored here.

The address of the vector table for timer interrupts,etc.,can be set as desired using the interrupt table register(INTB). See the section on interrupts for details.

From 00400_{16} up is RAM. For example, in the M30290FAHP, 8K bytes of internal RAM is mapped to the space from 00400_{16} to $023FF_{16}$. In addition to storing data, the RAM also stores the stack used when calling subroutines and when interrupts are generated.

These devices also contain two blocks of Flash ROM as Data Flash memory to store data. These two blocks of 2K bytes are located from $0F000_{16}$ to $0FFFF_{16}$ on all versions.

The SFR area is mapped from 00000_{16} to $003FF_{16}$. This area accommodates the control registers for peripheral devices such as I/O ports, A/D converter, serial I/O, and timers, etc. Any part of the SFR area that is not occupied is reserved and cannot be used for other purposes.

The special page vector table is allocated to the address from $FFE00_{16}$ to $FFFDB_{16}$. This vector is used by the JMPS or JSRS instruction. For details, refer to the "M16C/60 and M16C/20 Series Software Manual".

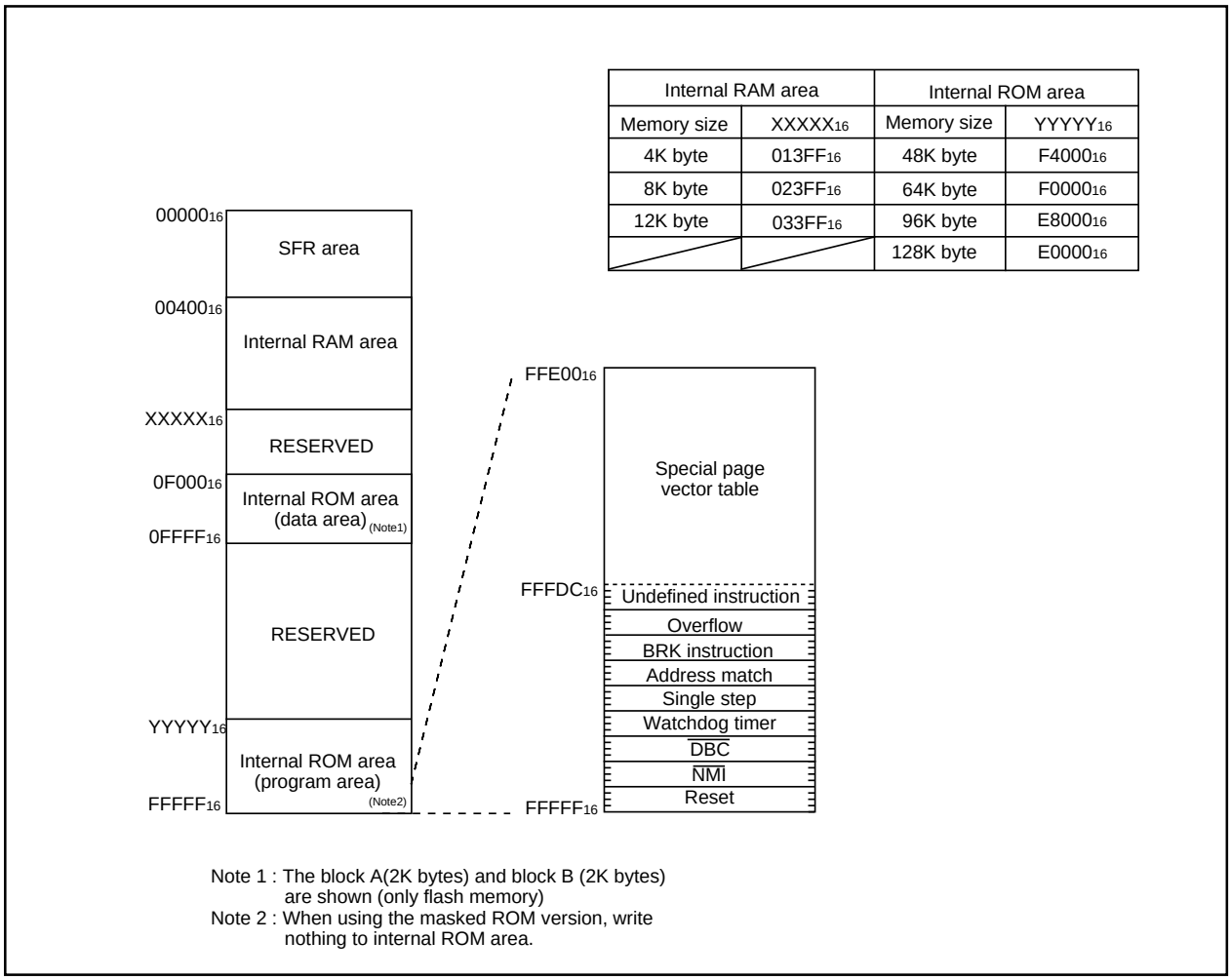


Figure 3.1. Memory Map

4. Special Function Register (SFR) Map

Address	Register		Symbol	After reset
0000₁₆				
0001₁₆				
0002₁₆				
0003₁₆				
0004₁₆	Processor mode register 0		PM0	00₁₆
0005₁₆	Processor mode register 1		PM1	00001000₂
0006₁₆	System clock control register 0		CM0	01001000₂
0007₁₆	System clock control register 1		CM1	00100000₂
0008₁₆				
0009₁₆	Address match interrupt enable register		AIER	XXXXXX00₂
000A₁₆	Protect register		PRCR	XX000000₂
000B₁₆				
000C₁₆	Oscillation stop detection register	(Note 2)	CM2	0X000010₂
000D₁₆				
000E₁₆	Watchdog timer start register		WDTS	??₁₆
000F₁₆	Watchdog timer control register		WDC	00??????₂ (Note3)
0010₁₆	Address match interrupt register 0		RMAD0	00₁₆
0011₁₆				00₁₆
0012₁₆				X0₁₆
0013₁₆				
0014₁₆	Address match interrupt register 1		RMAD1	00₁₆
0015₁₆				00₁₆
0016₁₆				X0₁₆
0017₁₆				
0018₁₆				
0019₁₆	Voltage detection register 1	(Note 4,5)	VCR1	00001000₂
001A₁₆	Voltage detection register 2	(Note 4,5)	VCR2	00₁₆
001B₁₆				
001C₁₆	PLL control register 0		PLC0	0001X010₂
001D₁₆				
001E₁₆	Processor mode register 2		PM2	XXX00000₂
001F₁₆	Voltage down detection interrupt register	(Note 5)	D4INT	00₁₆
0020₁₆	DMA0 source pointer		SAR0	??₁₆
0021₁₆				??₁₆
0022₁₆				X?₁₆
0023₁₆				
0024₁₆	DMA0 destination pointer		DAR0	??₁₆
0025₁₆				??₁₆
0026₁₆				X/16
0027₁₆				
0028₁₆	DMA0 transfer counter		TCR0	??₁₆
0029₁₆				??₁₆
002A₁₆				
002B₁₆				
002C₁₆	DMA0 control register		DM0CON	00000?00₂
002D₁₆				
002E₁₆				
002F₁₆				
0030₁₆	DMA1 source pointer		SAR1	??₁₆
0031₁₆				??₁₆
0032₁₆				X?₁₆
0033₁₆				
0034₁₆	DMA1 destination pointer		DAR1	??₁₆
0035₁₆				??₁₆
0036₁₆				X?₁₆
0037₁₆				
0038₁₆	DMA1 transfer counter		TCR1	??₁₆
0039₁₆				??₁₆
003A₁₆				
003B₁₆				
003C₁₆	DMA1 control register		DM1CON	00000?00₂
003D₁₆				
003E₁₆				
003F₁₆				

Note 1: The blank areas are reserved and cannot be used by users.
Note 2: The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.
Note 3: The WDC5 bit is "0" (cold start) immediately after power-on. It can only be set to "1" in a program.
It is set to "0" when the input voltage at the VCC pin drops to Vdet2 or less while the VC25 bit in the VCR2 register is set to "1" (RAM retention limit detection circuit enable).
Note 4: This register does not change at software reset, watchdog timer reset and oscillation stop detection reset.
Note 5: This registe can not use for T-ver. and V-ver.

X : Nothing is mapped to this bit
? : Undefined

Figure 4.1. SFR Map (1 of 11)

Address	Register	Symbol	After reset
0040₁₆			
0041₁₆	CAN0 wakeup interrupt control register	C01WKIC	XXXX?000₂
0042₁₆	CAN0 successful reception interrupt control register	C0RECIC	XXXX?000₂
0043₁₆	CAN0 successful transmission interrupt control register	C0TRMIC	XXXX?000₂
0044₁₆	INT3 interrupt control register	INT3IC	XX00?000₂
0045₁₆	ICOC 0 interrupt control register	ICOC0IC	XXXX?000₂
0046₁₆	ICOC 1 interrupt control register, I²C-BUS interface interrupt control register 1	ICOC1IC,IICIC	XXXX?000₂
0047₁₆	ICOC base timer interrupt control register, SCL/SDA interrupt control register 2	BTIC,SCLDAIC	XXXX?000₂
0048₁₆	SI/O4 interrupt control register, INT5 interrupt control register	S4IC, INT5IC	XX00?000₂
0049₁₆	SI/O3 interrupt control register, INT4 interrupt control register	S3IC, INT4IC	XX00?000₂
004A₁₆	UART2 Bus collision detection interrupt control register	BCNIC	XXXX?000₂
004B₁₆	DMA0 interrupt control register	DM0IC	XXXX?000₂
004C₁₆	DMA1 interrupt control register	DM1IC	XXXX?000₂
004D₁₆	CAN0 error interrupt control register	C01ERRIC	XXXX?000₂
004E₁₆	A/D conversion interrupt control register, Key input interrupt control register (Note 2)	ADIC, KUPIC	XXXX?000₂
004F₁₆	UART2 transmit interrupt control register	S2TIC	XXXX?000₂
0050₁₆	UART2 receive interrupt control register	S2RIC	XXXX?000₂
0051₁₆	UART0 transmit interrupt control register	S0TIC	XXXX?000₂
0052₁₆	UART0 receive interrupt control register	S0RIC	XXXX?000₂
0053₁₆	UART1 transmit interrupt control register	S1TIC	XXXX?000₂
0054₁₆	UART1 receive interrupt control register	S1RIC	XXXX?000₂
0055₁₆	TimerA0 interrupt control register	TA0IC	XXXX?000₂
0056₁₆	TimerA1 interrupt control register	TA1IC	XXXX?000₂
0057₁₆	TimerA2 interrupt control register	TA2IC	XXXX?000₂
0058₁₆	TimerA3 interrupt control register	TA3IC	XXXX?000₂
0059₁₆	TimerA4 interrupt control register	TA4IC	XXXX?000₂
005A₁₆	TimerB0 interrupt control register	TB0IC	XXXX?000₂
005B₁₆	TimerB1 interrupt control register	TB1IC	XXXX?000₂
005C₁₆	TimerB2 interrupt control register	TB2IC	XXXX?000₂
005D₁₆	INT0 interrupt control register	INT0IC	XX00?000₂
005E₁₆	INT1 interrupt control register	INT1IC	XX00?000₂
005F₁₆	INT2 interrupt control register	INT2IC	XX00?000₂
0060₁₆	CAN0 message box 0: Identifier/DLC		XX??????₂
0061₁₆			XX??????₂
0062₁₆			??₁₆
0063₁₆			X?₁₆
0064₁₆			X?₁₆
0065₁₆			XX??????₂
0066₁₆	CAN0 message box 0 : Data field		??₁₆
0067₁₆			??₁₆
0068₁₆			??₁₆
0069₁₆			??₁₆
006A₁₆			??₁₆
006B₁₆			??₁₆
006C₁₆			??₁₆
006D₁₆			??₁₆
006E₁₆	CAN0 message box 0 : Time stamp		??₁₆
006F₁₆			??₁₆
0070₁₆	CAN0 message box 1 : Identifier/DLC		XX??????₂
0071₁₆			XX??????₂
0072₁₆			??₁₆
0073₁₆			X?₁₆
0074₁₆			X?₁₆
0075₁₆			XX??????₂
0076₁₆	CAN0 message box 1 : Data field		??₁₆
0077₁₆			??₁₆
0078₁₆			??₁₆
0079₁₆			??₁₆
007A₁₆			??₁₆
007B₁₆			??₁₆
007C₁₆			??₁₆
007D₁₆			??₁₆
007E₁₆	CAN0 message box 1 : Time stamp		??₁₆
007F₁₆			??₁₆

Note 1: The blank areas are reserved and cannot be used by users.
Note 2: A/D conversion interrupt control register is effective when the bit1(Interrupt source select register (address 35Eh IFSR2A) is set to "0". Key input interrupt control register is effective when the bit1 is set to "1".
X : Nothing is mapped to this bit
? : Undefined

Figure 4.2. SFR Map (2 of 11)

Address	Register	Symbol	After reset
0080₁₆	CAN0 message box 2: Identifier/DLC		XX??????₂
0081₁₆			XX??????₂
0082₁₆			??₁₆
0083₁₆			X?₁₆
0084₁₆			X?₁₆
0085₁₆			XX??????₂
0086₁₆	CAN0 message box 2 : Data field		??₁₆
0087₁₆			??₁₆
0088₁₆			??₁₆
0089₁₆			??₁₆
008A₁₆			??₁₆
008B₁₆			??₁₆
008C₁₆			??₁₆
008D₁₆			??₁₆
008E₁₆	CAN0 message box 2 : Time stamp		??₁₆
008F₁₆			??₁₆
0090₁₆	CAN0 message box 3 : Identifier/DLC		XX??????₂
0091₁₆			XX??????₂
0092₁₆			??₁₆
0093₁₆			X?₁₆
0094₁₆			X?₁₆
0095₁₆			XX??????₂
0096₁₆	CAN0 message box 3 : Data field		??₁₆
0097₁₆			??₁₆
0098₁₆			??₁₆
0099₁₆			??₁₆
009A₁₆			??₁₆
009B₁₆			??₁₆
009C₁₆			??₁₆
009D₁₆			??₁₆
009E₁₆	CAN0 message box 3 : Time stamp		??₁₆
009F₁₆			??₁₆
00A0₁₆	CAN0 message box 4: Identifier/DLC		XX??????₂
00A1₁₆			XX??????₂
00A2₁₆			??₁₆
00A3₁₆			X?₁₆
00A4₁₆			X?₁₆
00A5₁₆			XX??????₂
00A6₁₆	CAN0 message box 4 : Data field		??₁₆
00A7₁₆			??₁₆
00A8₁₆			??₁₆
00A9₁₆			??₁₆
00AA₁₆			??₁₆
00AB₁₆			??₁₆
00AC₁₆			??₁₆
00AD₁₆			??₁₆
00AE₁₆	CAN0 message box 4 : Time stamp		??₁₆
00AF₁₆			??₁₆
00B0₁₆	CAN0 message box 5 : Identifier/DLC		XX??????₂
00B1₁₆			XX??????₂
00B2₁₆			??₁₆
00B3₁₆			X?₁₆
00B4₁₆			X?₁₆
00B5₁₆			XX??????₂
00B6₁₆	CAN0 message box 5 : Data field		??₁₆
00B7₁₆			??₁₆
00B8₁₆			??₁₆
00B9₁₆			??₁₆
00BA₁₆			??₁₆
00BB₁₆			??₁₆
00BC₁₆			??₁₆
00BD₁₆			??₁₆
00BE₁₆	CAN0 message box 5 : Time stamp		??₁₆
00BF₁₆			??₁₆

Note 1: The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit
? : Undefined

Figure 4.3. SFR Map (3 of 11)

Address	Register	Symbol	After reset
00C0₁₆	CAN0 message box 6: Identifier/DLC		XX??????₂
00C1₁₆			XX??????₂
00C2₁₆			??₁₆
00C3₁₆			X?₁₆
00C4₁₆			X?₁₆
00C5₁₆			XX??????₂
00C6₁₆	CAN0 message box 6 : Data field		??₁₆
00C7₁₆			??₁₆
00C8₁₆			??₁₆
00C9₁₆			??₁₆
00CA₁₆			??₁₆
00CB₁₆			??₁₆
00CC₁₆			??₁₆
00CD₁₆			??₁₆
00CE₁₆	CAN0 message box 6 : Time stamp		??₁₆
00CF₁₆			??₁₆
00D0₁₆	CAN0 message box 7 : Identifier/DLC		XX??????₂
00D1₁₆			XX??????₂
00D2₁₆			??₁₆
00D3₁₆			X?₁₆
00D4₁₆			X?₁₆
00D5₁₆			XX??????₂
00D6₁₆	CAN0 message box 7 : Data field		??₁₆
00D7₁₆			??₁₆
00D8₁₆			??₁₆
00D9₁₆			??₁₆
00DA₁₆			??₁₆
00DB₁₆			??₁₆
00DC₁₆			??₁₆
00DD₁₆			??₁₆
00DE₁₆	CAN0 message box 7 : Time stamp		??₁₆
00DF₁₆			??₁₆
00E0₁₆	CAN0 message box 8: Identifier/DLC		XX??????₂
00E1₁₆			XX??????₂
00E2₁₆			??₁₆
00E3₁₆			X?₁₆
00E4₁₆			X?₁₆
00E5₁₆			XX??????₂
00E6₁₆	CAN0 message box 8: Data field		??₁₆
00E7₁₆			??₁₆
00E8₁₆			??₁₆
00E9₁₆			??₁₆
00EA₁₆			??₁₆
00EB₁₆			??₁₆
00EC₁₆			??₁₆
00ED₁₆			??₁₆
00EE₁₆	CAN0 message box 8 : Time stamp		??₁₆
00EF₁₆			??₁₆
00F0₁₆	CAN0 message box 9 : Identifier/DLC		XX??????₂
00F1₁₆			XX??????₂
00F2₁₆			??₁₆
00F3₁₆			X?₁₆
00F4₁₆			X?₁₆
00F5₁₆			XX??????₂
00F6₁₆	CAN0 message box 9 : Data field		??₁₆
00F7₁₆			??₁₆
00F8₁₆			??₁₆
00F9₁₆			??₁₆
00FA₁₆			??₁₆
00FB₁₆			??₁₆
00FC₁₆			??₁₆
00FD₁₆			??₁₆
00FE₁₆	CAN0 message box 9 : Time stamp		??₁₆
00FF₁₆			??₁₆

Note 1: The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit
? : Undefined

Figure 4.4. SFR Map (4 of 11)

Address	Register	Symbol	After reset
0100$_{16}$	CAN0 message box 10: Identifier/DLC		XX??????$_2$
0101$_{16}$			XX??????$_2$
0102$_{16}$			??$_{16}$
0103$_{16}$			X?$_{16}$
0104$_{16}$			X?$_{16}$
0105$_{16}$			XX??????$_2$
0106$_{16}$	CAN0 message box 10 : Data field		??$_{16}$
0107$_{16}$			??$_{16}$
0108$_{16}$			??$_{16}$
0109$_{16}$			??$_{16}$
010A$_{16}$			??$_{16}$
010B$_{16}$			??$_{16}$
010C$_{16}$			??$_{16}$
010D$_{16}$			??$_{16}$
010E$_{16}$	CAN0 message box 10 : Time stamp		??$_{16}$
010F$_{16}$			??$_{16}$
0110$_{16}$	CAN0 message box 11 : Identifier/DLC		XX??????$_2$
0111$_{16}$			XX??????$_2$
0112$_{16}$			??$_{16}$
0113$_{16}$			X?$_{16}$
0114$_{16}$			X?$_{16}$
0115$_{16}$			XX??????$_2$
0116$_{16}$	CAN0 message box 11 : Data field		??$_{16}$
0117$_{16}$			??$_{16}$
0118$_{16}$			??$_{16}$
0119$_{16}$			??$_{16}$
011A$_{16}$			??$_{16}$
011B$_{16}$			??$_{16}$
011C$_{16}$			??$_{16}$
011D$_{16}$			??$_{16}$
011E$_{16}$	CAN0 message box 11 : Time stamp		??$_{16}$
011F$_{16}$			??$_{16}$
0120$_{16}$	CAN0 message box 12: Identifier/DLC		XX??????$_2$
0121$_{16}$			XX??????$_2$
0122$_{16}$			??$_{16}$
0123$_{16}$			X?$_{16}$
0124$_{16}$			X?$_{16}$
0125$_{16}$			XX??????$_2$
0126$_{16}$	CAN0 message box 12: Data field		??$_{16}$
0127$_{16}$			??$_{16}$
0128$_{16}$			??$_{16}$
0129$_{16}$			??$_{16}$
012A$_{16}$			??$_{16}$
012B$_{16}$			??$_{16}$
012C$_{16}$			??$_{16}$
012D$_{16}$			??$_{16}$
012E$_{16}$	CAN0 message box 12 : Time stamp		??$_{16}$
012F$_{16}$			??$_{16}$
0130$_{16}$	CAN0 message box 13 : Identifier/DLC		XX??????$_2$
0131$_{16}$			XX??????$_2$
0132$_{16}$			??$_{16}$
0133$_{16}$			X?$_{16}$
0134$_{16}$			X?$_{16}$
0135$_{16}$			XX??????$_2$
0136$_{16}$	CAN0 message box 13 : Data field		??$_{16}$
0137$_{16}$			??$_{16}$
0138$_{16}$			??$_{16}$
0139$_{16}$			??$_{16}$
013A$_{16}$			??$_{16}$
013B$_{16}$			??$_{16}$
013C$_{16}$			??$_{16}$
013D$_{16}$			??$_{16}$
013E$_{16}$	CAN0 message box 13 : Time stamp		??$_{16}$
013F$_{16}$			??$_{16}$

Note 1: The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit
? : Undefined

Figure 4.5. SFR Map (5 of 11)

Address	Register	Symbol	After reset
0140₁₆	CAN0 message box 14: Identifier/DLC		XX??????₂
0141₁₆			XX??????₂
0142₁₆			??₁₆
0143₁₆			X?₁₆
0144₁₆			X?₁₆
0145₁₆			XX??????₂
0146₁₆	CAN0 message box 14 : Data field		??₁₆
0147₁₆			??₁₆
0148₁₆			??₁₆
0149₁₆			??₁₆
014A₁₆			??₁₆
014B₁₆			??₁₆
014C₁₆			??₁₆
014D₁₆			??₁₆
014E₁₆	CAN0 message box 14 : Time stamp		??₁₆
014F₁₆			??₁₆
0150₁₆	CAN0 message box 15 : Identifier/DLC		XX??????₂
0151₁₆			XX??????₂
0152₁₆			??₁₆
0153₁₆			X?₁₆
0154₁₆			X?₁₆
0155₁₆			XX??????₂
0156₁₆	CAN0 message box 15 : Data field		??₁₆
0157₁₆			??₁₆
0158₁₆			??₁₆
0159₁₆			??₁₆
015A₁₆			??₁₆
015B₁₆			??₁₆
015C₁₆			??₁₆
015D₁₆			??₁₆
015E₁₆	CAN0 message box 15 : Time stamp		??₁₆
015F₁₆			??₁₆
0160₁₆	CAN0 global mask register	C0GMR	XX??????₂
0161₁₆			XX??????₂
0162₁₆			??₁₆
0163₁₆			X?₁₆
0164₁₆			XX₁₆
0165₁₆			XX??????₂
0166₁₆	CAN0 local mask A register	C0LMAR	XX??????₂
0167₁₆			XX??????₂
0168₁₆			??₁₆
0169₁₆			X?₁₆
016A₁₆			XX₁₆
016B₁₆			XX??????₂
016C₁₆	CAN0 local mask B register	C0LMBR	XX??????₂
016D₁₆			XX??????₂
016E₁₆			??₁₆
016F₁₆			X?₁₆
0170₁₆			XX₁₆
0171₁₆			XX??????₂
≈			≈
01B3₁₆	Flash memory control register 4 (Note 2)	FMR4	0100000X₂
01B4₁₆			
01B5₁₆	Flash memory control register 1 (Note 2)	FMR1	000???0?₂
01B6₁₆			
01B7₁₆	Flash memory control register 0 (Note 2)	FMR0	01₁₆
≈			≈
01FD₁₆			
01FE₁₆			
01FF₁₆			

Note 1: The blank areas are reserved and cannot be used by users.
Note 2: This register is included in the flash memory version.

X :Nothing is mapped to this bit
? : Undefined

Figure 4.6. SFR Map (6 of 11)

Address	Register	Symbol	After reset
0200₁₆	CAN0 message control register 0	C0MCTL0	00₁₆
0201₁₆	CAN0 message control register 1	C0MCTL1	00₁₆
0202₁₆	CAN0 message control register 2	C0MCTL2	00₁₆
0203₁₆	CAN0 message control register 3	C0MCTL3	00₁₆
0204₁₆	CAN0 message control register 4	C0MCTL4	00₁₆
0205₁₆	CAN0 message control register 5	C0MCTL5	00₁₆
0206₁₆	CAN0 message control register 6	C0MCTL6	00₁₆
0207₁₆	CAN0 message control register 7	C0MCTL7	00₁₆
0208₁₆	CAN0 message control register 8	C0MCTL8	00₁₆
0209₁₆	CAN0 message control register 9	C0MCTL9	00₁₆
020A₁₆	CAN0 message control register 10	C0MCTL10	00₁₆
020B₁₆	CAN0 message control register 11	C0MCTL11	00₁₆
020C₁₆	CAN0 message control register 12	C0MCTL12	00₁₆
020D₁₆	CAN0 message control register 13	C0MCTL13	00₁₆
020E₁₆	CAN0 message control register 14	C0MCTL14	00₁₆
020F₁₆	CAN0 message control register 15	C0MCTL15	00₁₆
0210₁₆	CAN0 control register	C0CTLR	X0000001₂
0211₁₆			XX0X0000₂
0212₁₆	CAN0 status register	C0STR	00₁₆
0213₁₆			X0000001₂
0214₁₆	CAN0 slot status register	C0SSTR	00₁₆
0215₁₆			00₁₆
0216₁₆	CAN0 interrupt control register	C0ICR	00₁₆
0217₁₆			00₁₆
0218₁₆	CAN0 extended ID register	C0IDR	00₁₆
0219₁₆			00₁₆
021A₁₆	CAN0 configuration register	C0CONR	??₁₆
021B₁₆			??₁₆
021C₁₆	CAN0 receive error count register	C0RECR	00₁₆
021D₁₆	CAN0 transmit error count register	C0TECR	00₁₆
021E₁₆	CAN0 time stamp register	C0TSR	00₁₆
021F₁₆			00₁₆
≈			≈
0242₁₆	CAN0 acceptance filter support register	C0AFS	??₁₆
0243₁₆			??₁₆
≈			≈
025A₁₆	Three-phase protect control register	TPRC	00₁₆
025B₁₆			
025C₁₆	On-chip oscillator control register	ROCR	00000101₂
025D₁₆	Pin assignment control register	PACR	00₁₆
025E₁₆	Peripheral clock select register	PCLKR	00000011₂
025F₁₆	CAN0 clock select register	CCLKR	00₁₆
≈			≈
02E0₁₆	I^2C0 data-shift register	S00	??₁₆
02E1₁₆			
02E2₁₆	I^2C0 address register	S0D0	00₁₆
02E3₁₆	I^2C0 control register 0	S1D0	00₁₆
02E4₁₆	I^2C0 clock control register	S20	00₁₆
02E5₁₆	I^2C0 start/stop condition control register	S2D0	00011010₂
02E6₁₆	I^2C0 control register 1	S3D0	00110000₂
02E7₁₆	I^2C0 control register 2	S4D0	00₁₆
02E8₁₆	I^2C0 status register	S10	0001000X₂
≈			≈
02FD₁₆			
02FE₁₆			
02FF₁₆			

Note 1: The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit
? : Undefined

Figure 4.7. SFR Map (7 of 11)

Address	Register	Symbol	After reset
0300₁₆	Time measurement, Pulse generation register 0	G1TM0,G1PO0	??₁₆
0301₁₆			??₁₆
0302₁₆	Time measurement, Pulse generation register 1	G1TM1,G1PO1	??₁₆
0303₁₆			??₁₆
0304₁₆	Time measurement, Pulse generation register 2	G1TM2,G1PO2	??₁₆
0305₁₆			??₁₆
0306₁₆	Time measurement, Pulse generation register 3	G1TM3,G1PO3	??₁₆
0307₁₆			??₁₆
0308₁₆	Time measurement, Pulse generation register 4	G1TM4,G1PO4	??₁₆
0309₁₆			??₁₆
030A₁₆	Time measurement, Pulse generation register 5	G1TM5,G1PO5	??₁₆
030B₁₆			??₁₆
030C₁₆	Time measurement, Pulse generation register 6	G1TM6,G1PO6	??₁₆
030D₁₆			??₁₆
030E₁₆	Time measurement, Pulse generation register 7	G1TM7,G1PO7	??₁₆
030F₁₆			??₁₆
0310₁₆	Pulse generation control register 0	G1POCR0	0X00XX00₂
0311₁₆	Pulse generation control register 1	G1POCR1	0X00XX00₂
0312₁₆	Pulse generation control register 2	G1POCR2	0X00XX00₂
0313₁₆	Pulse generation control register 3	G1POCR3	0X00XX00₂
0314₁₆	Pulse generation control register 4	G1POCR4	0X00XX00₂
0315₁₆	Pulse generation control register 5	G1POCR5	0X00XX00₂
0316₁₆	Pulse generation control register 6	G1POCR6	0X00XX00₂
0317₁₆	Pulse generation control register 7	G1POCR7	0X00XX00₂
0318₁₆	Time measurement control register 0	G1TMCR0	00₁₆
0319₁₆	Time measurement control register 1	G1TMCR1	00₁₆
031A₁₆	Time measurement control register 2	G1TMCR2	00₁₆
031B₁₆	Time measurement control register 3	G1TMCR3	00₁₆
031C₁₆	Time measurement control register 4	G1TMCR4	00₁₆
031D₁₆	Time measurement control register 5	G1TMCR5	00₁₆
031E₁₆	Time measurement control register 6	G1TMCR6	00₁₆
031F₁₆	Time measurement control register 7	G1TMCR7	00₁₆
0320₁₆	Base timer register	G1BT	??₁₆
0321₁₆			??₁₆
0322₁₆	Base timer control register 0	G1BCR0	00₁₆
0323₁₆	Base timer control register 1	G1BCR1	00₁₆
0324₁₆	Time measurement prescale register 6	G1TPR6	00₁₆
0325₁₆	Time measurement prescale register 7	G1TPR7	00₁₆
0326₁₆	Function enable register	G1FE	00₁₆
0327₁₆	Function select register	G1FS	00₁₆
0328₁₆	Base timer reset register	G1BTRR	??₁₆
0329₁₆			??₁₆
032A₁₆	Count source division register	G1DV	00₁₆
032B₁₆			
032C₁₆			
032D₁₆			
032E₁₆			
032F₁₆			
0330₁₆	Interrupt request register	G1IR	??₁₆
0331₁₆	Interrupt enable register 0	G1IE0	00₁₆
0332₁₆	Interrupt enable register 1	G1IE1	00₁₆
0333₁₆			
0334₁₆			
0335₁₆			
0336₁₆			
0337₁₆			
0338₁₆			
0339₁₆			
033A₁₆			
033B₁₆			
033C₁₆			
033D₁₆			
033E₁₆	NMI digital debounce register	NDDR	FF₁₆
033F₁₆	Port P17 digital debounce register	P17DDR	FF₁₆

Note 1: The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit
? : Undefined

Figure 4.8. SFR Map (8 of 11)

Address	Register	Symbol	After reset
0340$_{16}$			
0341$_{16}$			
0342$_{16}$	Timer A1-1 register	TA11	??$_{16}$
0343$_{16}$			??$_{16}$
0344$_{16}$	Timer A2-1 register	TA21	??$_{16}$
0345$_{16}$			??$_{16}$
0346$_{16}$	Timer A4-1 register	TA41	??$_{16}$
0347$_{16}$			??$_{16}$
0348$_{16}$	Three phase PWM control register 0	INVC0	00$_{16}$
0349$_{16}$	Three phase PWM control register 1	INVC1	00$_{16}$
034A$_{16}$	Three phase output buffer register 0	IDB0	00$_{16}$
034B$_{16}$	Three phase output buffer register 1	IDB1	00$_{16}$
034C$_{16}$	Dead time timer	DTT	??$_{16}$
034D$_{16}$	Timer B2 Interrupt occurrence frequency set counter	ICTB2	??$_{16}$
034E$_{16}$	Position - data - retain function control register	PDRF	XXXX0000$_2$
034F$_{16}$			
0350$_{16}$			
0351$_{16}$			
0352$_{16}$			
0353$_{16}$			
0354$_{16}$			
0355$_{16}$			
0356$_{16}$			
0357$_{16}$			
0358$_{16}$	Port function control register	PFCR	00111111$_2$
0359$_{16}$			
035A$_{16}$			
035B$_{16}$			
035C$_{16}$			
035D$_{16}$			
035E$_{16}$	Interrupt cause select register 2	IFSR2A	00XXX000$_2$
035F$_{16}$	Interrupt cause select register	IFSR	00$_{16}$
0360$_{16}$	SI/O3 transmit/receive register	S3TRR	??$_{16}$
0361$_{16}$			
0362$_{16}$	SI/O3 control register	S3C	01000000$_2$
0363$_{16}$	SI/O3 bit rate register	S3BRG	??$_{16}$
0364$_{16}$	SI/O4 transmit/receive register	S4TRR	??$_{16}$
0365$_{16}$			
0366$_{16}$	SI/O4 control register	S4C	01000000$_2$
0367$_{16}$	SI/O4 bit rate register	S4BRG	??$_{16}$
0368$_{16}$			
0369$_{16}$			
036A$_{16}$			
036B$_{16}$			
036C$_{16}$			
036D$_{16}$			
036E$_{16}$			
036F$_{16}$			
0370$_{16}$			
0371$_{16}$			
0372$_{16}$			
0373$_{16}$			
0374$_{16}$	UART2 special mode register 4	U2SMR4	00$_{16}$
0375$_{16}$	UART2 special mode register 3	U2SMR3	000X0X0X$_2$
0376$_{16}$	UART2 special mode register 2	U2SMR2	X0000000$_2$
0377$_{16}$	UART2 special mode register	U2SMR	X0000000$_2$
0378$_{16}$	UART2 transmit/receive mode register	U2MR	00$_{16}$
0379$_{16}$	UART2 bit rate register	U2BRG	??$_{16}$
037A$_{16}$	UART2 transmit buffer register	U2TB	????????$_2$
037B$_{16}$			XXXXXXX?$_2$
037C$_{16}$	UART2 transmit/receive control register 0	U2C0	00001000$_2$
037D$_{16}$	UART2 transmit/receive control register 1	U2C1	00000010$_2$
037E$_{16}$	UART2 receive buffer register	U2RB	????????$_2$
037F$_{16}$			?????XX?$_2$

Note 1 :The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit
? : Undefined

Figure 4.9. SFR Map (9 of 11)

Address	Register	Symbol	After reset
0380$_{16}$	Count start flag	TABSR	00$_{16}$
0381$_{16}$	Clock prescaler reset flag	CPSRF	0XXXXXXX$_2$
0382$_{16}$	One-shot start flag	ONSF	00$_{16}$
0383$_{16}$	Trigger select register	TRGSR	00$_{16}$
0384$_{16}$	Up-dowm flag	UDF	00$_{16}$
0385$_{16}$			
0386$_{16}$	Timer A0 register	TA0	??$_{16}$
0387$_{16}$			??$_{16}$
0388$_{16}$	Timer A1 register	TA1	??$_{16}$
0389$_{16}$			??$_{16}$
038A$_{16}$	Timer A2 register	TA2	??$_{16}$
038B$_{16}$			??$_{16}$
038C$_{16}$	Timer A3 register	TA3	??$_{16}$
038D$_{16}$			??$_{16}$
038E$_{16}$	Timer A4 register	TA4	??$_{16}$
038F$_{16}$			??$_{16}$
0390$_{16}$	Timer B0 register	TB0	??$_{16}$
0391$_{16}$			??$_{16}$
0392$_{16}$	Timer B1 register	TB1	??$_{16}$
0393$_{16}$			??$_{16}$
0394$_{16}$	Timer B2 register	TB2	??$_{16}$
0395$_{16}$			??$_{16}$
0396$_{16}$	Timer A0 mode register	TA0MR	00$_{16}$
0397$_{16}$	Timer A1 mode register	TA1MR	00$_{16}$
0398$_{16}$	Timer A2 mode register	TA2MR	00$_{16}$
0399$_{16}$	Timer A3 mode register	TA3MR	00$_{16}$
039A$_{16}$	Timer A4 mode register	TA4MR	00$_{16}$
039B$_{16}$	Timer B0 mode register	TB0MR	00??0000$_2$
039C$_{16}$	Timer B1 mode register	TB1MR	00?X0000$_2$
039D$_{16}$	Timer B2 mode register	TB2MR	00?X0000$_2$
039E$_{16}$	Timer B2 special mode register	TB2SC	X0000000$_2$
039F$_{16}$			
03A0$_{16}$	UART0 transmit/receive mode register	U0MR	00$_{16}$
03A1$_{16}$	UART0 bit rate register	U0BRG	??$_{16}$
03A2$_{16}$	UART0 transmit buffer register	U0TB	????????$_2$
03A3$_{16}$			XXXXXXX?$_2$
03A4$_{16}$	UART0 transmit/receive control register 0	U0C0	00001000$_2$
03A5$_{16}$	UART0 transmit/receive control register 1	U0C1	00000010$_2$
03A6$_{16}$	UART0 receive buffer register	U0RB	????????$_2$
03A7$_{16}$			?????XX?$_2$
03A8$_{16}$	UART1 transmit/receive mode register	U1MR	00$_{16}$
03A9$_{16}$	UART1 bit rate register	U1BRG	??$_{16}$
03AA$_{16}$	UART1 transmit buffer register	U1TB	????????$_2$
03AB$_{16}$			XXXXXXX?$_2$
03AC$_{16}$	UART1 transmit/receive control register 0	U1C0	00001000$_2$
03AD$_{16}$	UART1 transmit/receive control register 1	U1C1	00000010$_2$
03AE$_{16}$	UART1 receive buffer register	U1RB	????????$_2$
03AF$_{16}$			?????XX?$_2$
03B0$_{16}$	UART transmit/receive control register 2	UCON	X0000000$_2$
03B1$_{16}$			
03B2$_{16}$			
03B3$_{16}$			
03B4$_{16}$	CRC snoop address register	CRCSAR	??$_{16}$
03B5$_{16}$			00XXXX??$_2$
03B6$_{16}$	CRC mode register	CRCMR	0XXXXXX0$_2$
03B7$_{16}$			
03B8$_{16}$	DMA0 request cause select register	DM0SL	00$_{16}$
03B9$_{16}$			
03BA$_{16}$	DMA1 request cause select register	DM1SL	00$_{16}$
03BB$_{16}$			
03BC$_{16}$	CRC data register	CRCD	??$_{16}$
03BD$_{16}$			??$_{16}$
03BE$_{16}$	CRC input register	CRCIN	??$_{16}$
03BF$_{16}$			

Note 1: The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit
? : Undefined

Figure 4.10. SFR Map (10 of 11)

Address	Register	Symbol	After reset
03C0$_{16}$	A/D register 0	AD0	????????$_2$
03C1$_{16}$			XXXXXX??$_2$
03C2$_{16}$	A/D register 1	AD1	????????$_2$
03C3$_{16}$			XXXXXX??$_2$
03C4$_{16}$	A/D register 2	AD2	????????$_2$
03C5$_{16}$			XXXXXX??$_2$
03C6$_{16}$	A/D register 3	AD3	????????$_2$
03C7$_{16}$			XXXXXX??$_2$
03C8$_{16}$	A/D register 4	AD4	????????$_2$
03C9$_{16}$			XXXXXX??$_2$
03CA$_{16}$	A/D register 5	AD5	????????$_2$
03CB$_{16}$			XXXXXX??$_2$
03CC$_{16}$	A/D register 6	AD6	????????$_2$
03CD$_{16}$			XXXXXX??$_2$
03CE$_{16}$	A/D register 7	AD7	????????$_2$
03CF$_{16}$			XXXXXX??$_2$
03D0$_{16}$			
03D1$_{16}$			
03D2$_{16}$	A/D trigger control register	ADTRGCON	XXXX0000$_2$
03D3$_{16}$	A/D status register 0	ADSTAT0	00000X00$_2$
03D4$_{16}$	A/D control register 2	ADCON2	00$_{16}$
03D5$_{16}$			
03D6$_{16}$	A/D control register 0	ADCON0	00000???$_2$
03D7$_{16}$	A/D control register 1	ADCON1	00$_{16}$
03D8$_{16}$			
03D9$_{16}$			
03DA$_{16}$			
03DB$_{16}$			
03DC$_{16}$			
03DD$_{16}$			
03DE$_{16}$			
03DF$_{16}$			
03E0$_{16}$	Port P0 register	P0	??$_{16}$
03E1$_{16}$	Port P1 register	P1	??$_{16}$
03E2$_{16}$	Port P0 direction register	PD0	00$_{16}$
03E3$_{16}$	Port P1 direction register	PD1	00$_{16}$
03E4$_{16}$	Port P2 register	P2	??$_{16}$
03E5$_{16}$	Port P3 register	P3	??$_{16}$
03E6$_{16}$	Port P2 direction register	PD2	00$_{16}$
03E7$_{16}$	Port P3 direction register	PD3	00$_{16}$
03E8$_{16}$			
03E9$_{16}$			
03EA$_{16}$			
03EB$_{16}$			
03EC$_{16}$	Port P6 register	P6	??$_{16}$
03ED$_{16}$	Port P7 register	P7	??$_{16}$
03EE$_{16}$	Port P6 direction register	PD6	00$_{16}$
03EF$_{16}$	Port P7 direction register	PD7	00$_{16}$
03F0$_{16}$	Port P8 register	P8	??$_{16}$
03F1$_{16}$	Port P9 register	P9	???X????$_2$
03F2$_{16}$	Port P8 direction register	PD8	00$_{16}$
03F3$_{16}$	Port P9 direction register	PD9	000X0000$_2$
03F4$_{16}$	Port P10 register	P10	??$_{16}$
03F5$_{16}$			
03F6$_{16}$	Port P10 direction register	PD10	00$_{16}$
03F7$_{16}$			
03F8$_{16}$			
03F9$_{16}$			
03FA$_{16}$			
03FB$_{16}$			
03FC$_{16}$	Pull-up control register 0	PUR0	00$_{16}$
03FD$_{16}$	Pull-up control register 1	PUR1	00$_{16}$
03FE$_{16}$	Pull-up control register 2	PUR2	00$_{16}$
03FF$_{16}$	Port control register	PCR	00$_{16}$

Note 1: The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit
? : Undefined

Figure 4.11. SFR Map (11 of 11)

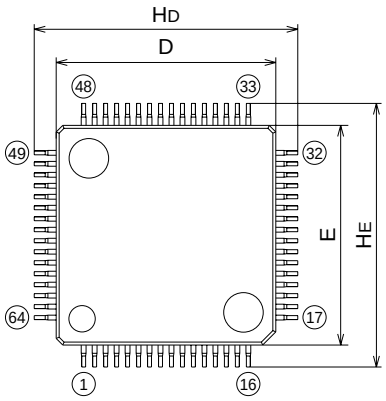
5. Package

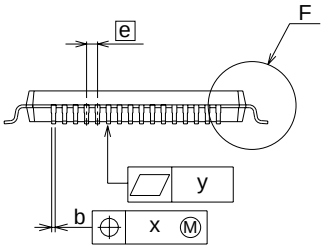
64P6Q-A

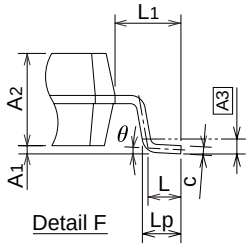
Recommended

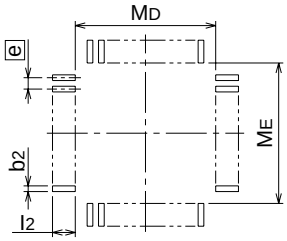
Plastic 64pin 10×10mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP64-P-1010-0.5	–		Cu Alloy









Recommended Mount Pad

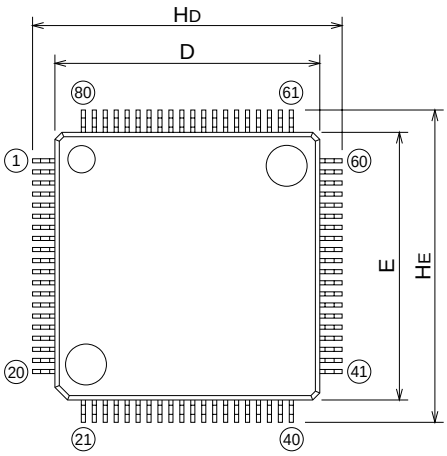
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	9.9	10.0	10.1
E	9.9	10.0	10.1
e	–	0.5	–
HD	11.8	12.0	12.2
HE	11.8	12.0	12.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	10°
b2	–	0.225	–
l2	1.0	–	–
MD	–	10.4	–
ME	–	10.4	–

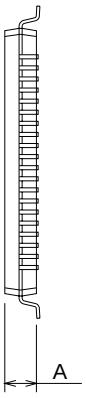
80P6Q-A

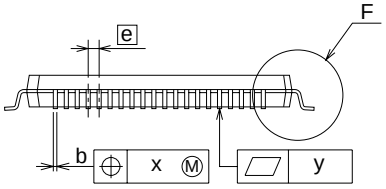
Recommended

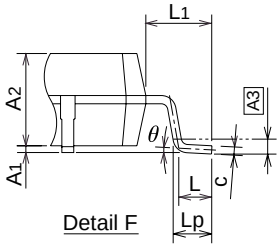
Plastic 80pin 12×12mm body LQFP

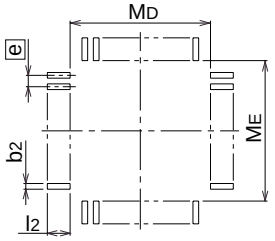
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP80-P-1212-0.5	–	0.47	Cu Alloy











Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	11.9	12.0	12.1
E	11.9	12.0	12.1
e	–	0.5	–
HD	13.8	14.0	14.2
HE	13.8	14.0	14.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	10°
b2	–	0.225	–
l2	0.9	–	–
MD	–	12.4	–
ME	–	12.4	–

6. Functional differences

6.1 Functional differences between Normal-ver. and T-ver./V-ver. of M16C/29 group

Item	Detailed Item	M16C/29(Normal-ver.)	M16C/29(T-ver./V-ver.)
Reset	Voltage Detection Circuit (Function of 0019_{16}, $001A_{16}$, $001F_{16}$)	Available (Power supply detection register 1, Power supply detection register 2, Power supply down detection interrupt register)	Not available (Reserved register)

Note. Refer to Hardware Manual about detail and electrical characteristics.

6.2 Functional differences between M16C/28 group and M16C/29 group (Normal-ver.)

Item	Detailed Item	M16C/28(Normal-ver.)	M16C/29(Normal-ver.)
Clock	Clock Output Function	Not available (reserved bit)	Available (Clock output function select bit)
Protect	PRC0 bit function	Enable wrtite to CM0, CM1, CM2, POCR, PLC0, PCLKR registers	Enable write to CM0, CM1, CM2, POCR, PLC0, PCLKR, CCLKR registers
Interrupt	IFSR20 bit of IFSR2A register	Must be set to "1"	Must be set to "0"
	b1 bit of IFSR2A register	Nothing is assigned (When write, set to "0")	Interrupt request cause select bit (0:A/D conversion 1:Key input)
	b2 bit of IFSR2A register	Nothing is assigned (When write, set to "0")	Interrupt request cause select bit (0:CAN0 wakeup/error)
	Interrupr source of software interrupt number 13	Key input interrupt	CAN0 error
	Interrupr source of software interrupt number 14	A/D conversion interrupt	A/D conversion/Key input interrupt
Three-Phase Motor Control Timer	Three-phase/Port Output Switch Function (0358_{16})	Not available (Nothing is assigned)	Available (Port function control register)
A/D Conversion	Analog Input pins	24 channels (AN_{30} to AN_{32} not available)	27 channels (AN_{30} to AN_{32} available)
	Delayed trigger mode 0	The product of the first edition and version A do not available	Available
	Delayed trigger mode 1	The product of the first edition and version A do not available	Available
CAN Module	2.0B BOSCH compliant	Not available (Related registers are not assigned)	Available (1channel)
CRC Calculation	CRC-CCITT and CRC-16	Not available (Related registers are not assigned)	Available (1 curcuit)
Pin Function	2 pin (80 pin version) 62 pin (64 pin version)	$P9_3/AN_{24}$	$P9_3/AN_{24}/CTX$
	3 pin (80 pin version) 64 pin (64 pin version)	$P9_2/TB_{2IN}$	$P9_2/AN_{32}/TB_{2IN}/CRX$
	4 pin (80 pin version) 1 pin (64 pin version)	$P9_1/TB_{1IN}$	$P9_1/AN_{31}/TB_{1IN}$
	5 pin (80 pin version) 2 pin (64 pin version)	$P9_0/TB_{0IN}$	$P9_0/AN_{30}/TB_{0IN}/CLK_{OUT}$

Note. Refer to Hardware Manual about detail and electrical characteristics.

6.3 Functional differences between M16C/28 group and M16C/29 group (T-ver./V-ver.)

Item	Detailed Item	M16C/28(T-ver./V-ver.)	M16C/29(T-ver./V-ver.)
Protect	PRC0 bit function	Enable wrtite to CM0, CM1, CM2, POCR, PLC0, PCLKR registers	Enable write to CM0, CM1, CM2, POCR, PLC0, PCLKR, CCLKR registers
Interrupt	IFSR20 bit of IFSR2A register	Must be set to "1"	Must be set to "0"
	b1 bit of IFSR2A register	Nothing is assigned (When write, set to "0")	Interrupt request cause select bit (0:A/D conversion 1:Key input)
	b2 bit of IFSR2A register	Nothing is assigned (When write, set to "0")	Interrupt request cause select bit (0:CAN0 wakeup/error)
	Interrupr source of software interrupt number 13	Key input interrupt	CAN0 error
	Interrupr source of software interrupt number 14	A/D conversion interrupt	A/D conversion/Key input interrupt
CAN Module	2.0B BOSCH compliant	Not available (Related registers are not assigned)	Available (1channel)
Pin Function	2 pin (80 pin version) 62 pin (64 pin version)	P9$_3$/AN$_{24}$	P9$_3$/AN$_{24}$/CTX
	3 pin (80 pin version) 64 pin (64 pin version)	P9$_2$/TB$_{2IN}$	P9$_2$/AN$_{32}$/TB$_{2IN}$/CRX

Note. Refer to Hardware Manual about detail and electrical characteristics.

REVISION HISTORY	M16C/29 Short Sheet

Rev.	Date	Description	
		Page	Summary
0.20	Apri/ 10/ 04		First edition
0.30	Jun/15/04	2,3	Table 1.2.1 and 1.2.2 are partly revised.
		4,5	Figure 1.3.1 and 1.3.2 are integrated descriptions.
		7	Table 1.4.4 is added.
		8	Figure 1.4.2 is added.
		11,12	Table 1.6.1 and 1.6.2 are integrated descriptions.
		14	Note 2 in Figure 3.1 is added.
		15	The Chapter ”3. Memory” and Figure 3.1 are integrated descriptions.
		16	Figure 4.1 is partly revised.
		17,18	Figure 4.2 and 4.3 are integrated descriptions.
		22	Figure 4.7 is integrated descriptions.
		23	Figure 4.8 is partly revised.
		26	Figure 4.11 is integrated descriptions.
		27	64P6Q-A package is revised.
		28 to 30	The Chapter “6. Functional differences” is added.

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