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A TDK Group Company

SSI 32C9022
SCSI Combo Controller
48 Mbit/s; dual bit NRZ interface

Preliminary Data

January 1995

DESCRIPTION

The SSI 32C9022 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build a SCSI disk drive. The circuitry of the SSI 32C9022 includes a complete SCSI target interface, an advanced buffer manager, a high performance disk formatter and an 88-bit Reed-Solomon ECC with fast "on-the-fly" hardware correction. The SSI 32C9022 provides maximum performance while minimizing micro controller intervention.

The SSI 32C9022 provides a dual bit and single bit NRZ interface to the ENDEC. Both Interfaces allow an effective transfer rate of up to 48 megabits per second on the disk interface. The dual bit Interface utilizes two parallel NRZ data signals and a clock rate of 24 MHz. The reduction of overall clock rates between the SSI 32C9022 and the ENDEC can be of great benefit to the designer.

The SSI 32C9022 can sustain concurrent transfers of up to 48 megabits per second transfer rate to the disk and 10 megabytes per second across the SCSI bus.

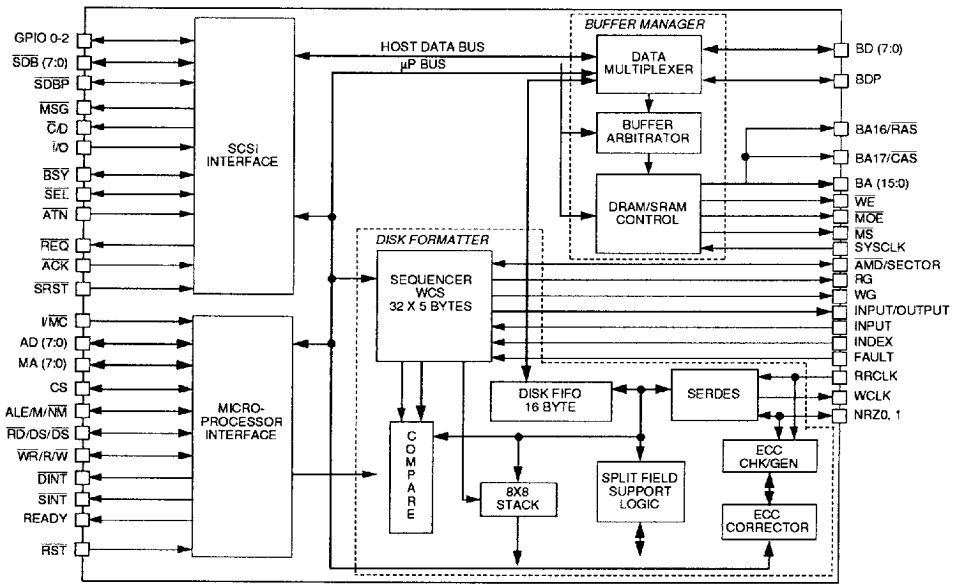
(continued)

FEATURES

- **SCSI Bus Interface**
  - **Full SCSI-2 Compatibility**
  - **Direct bus interface logic with on-chip 48 mA drivers**
  - **Synchronous transfer rates up to 10 megabytes per second**
  - **Asynchronous transfer rates up to 5 megabytes per second**
  - **Parity generation and checking**
  - **Auto Command Mode (ACM) SCSI state machine performs high level SCSI sequences without microprocessor intervention**
  - **Four level ACM command FIFO supports automatic execution of multiple ACM commands**
  - **Hardware support for automatic handling of SCSI-2 command queuing**
  - **Automatic SCSI CDB size determination**
  - **Automatic SCSI Disconnect and Reconnect**
  - **Sixteen byte data FIFO between SCSI channel and Buffer Manager**

(continued)

BLOCK DIAGRAM



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DESCRIPTION (continued)

In addition, on-the-fly error corrections and microcontroller accesses to the buffer memory will not degrade the throughput during transfers.

The SSI 32C9022 is one of a family of Silicon Systems' single chip disk controllers which support a wide range of device interfaces. The SSI 32C9020 is similar to the SSI 32C9022, but is contained in a 100-pin package, giving up some features for size. Other family members support AT and PCMCIA interfaces. All members are based on a common architecture allowing major portions of firmware to be reused. The Silicon Systems' chip family is illustrated in the hierarchy chart shown in Figure 1.

The high level of integration within the SSI 32C9022 represents a major reduction in parts count. When the SSI 32C9022 SCSI Controller is combined with the SSI 32R2110 Read/Write device, the SSI 32P4782 Combination Read Channel, the SSI 32D4680 Time Base Generator, the SSI 32H4631 Servo and Motor Speed Controller, an appropriate microcontroller and memory, a complete, cost efficient, high performance intelligent drive solution is created.

FEATURES (continued)

- Buffer Manager
  - Direct support of DRAM or SRAM
    - SRAM throughput to 20 megabytes per second
    - SRAM size up to 256k bytes
    - DRAM throughput to 17.78 megabytes per second
    - DRAM size up to 1 megabyte
  - Programmable memory timing
  - Buffer RAM segmentation with flexible segment sizes from 256 bytes to 1 megabyte
  - Dedicated host, disk and microprocessor address pointers
  - Internal buffer protection circuit provides buffer integrity
- Disk Formatter
  - Dual bit or serial NRZ interface
  - Effective data rates to 80 megabits/s
  - Automatic multi-sector transfer
  - Header or microprocessor based split data field support
  - Advanced sequencer organized in 32 x 5 bytes
  - 88-bit Reed Solomon ECC with "on-the-fly" fast hardware correction circuitry
  - Capable of correcting up to four 10-bit symbols in error

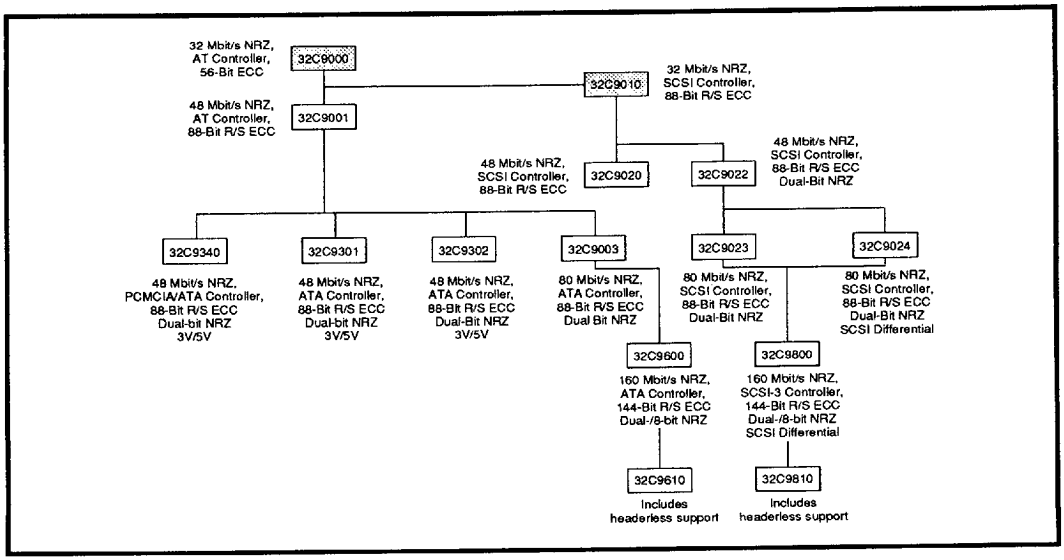

FIGURE 1: Silicon Systems' Single Chip Controller Hierarchy

  - Guaranteed to correct one 31-bit burst or two 11-bit bursts
  - Hardware on-the-fly correction of an 11-bit single burst error within a half sector time
  - Detects up to one 51-bit burst or three 11-bit bursts
- Microprocessor Interface
  - Supports both multiplexed or non-multiplexed microprocessors
  - Separate or combined host and disk interrupts
  - Programmable wait state insertion
- Other Features
  - Internal Power Down modes
  - Available in 128-pin QFP

FUNCTIONAL DESCRIPTION

The SSI 32C9022 contains the following four major functional blocks:

Microcontroller Interface
SCSI Interface
Disk Formatter
Buffer Manager

The microprocessor interface allows the local microprocessor access to all of the SSI 32C9022 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers can control all activities of the SSI 32C9022. The microprocessor can elect to perform SCSI and/or disk operations directly, or it can enable the advanced features of the SSI 32C9022 which can perform all typical operations automatically.

The SCSI Interface block handles all SCSI activities. The SCSI interface includes 48 mA drivers allowing for direct connection of the SSI 32C9022 to the SCSI bus. The SCSI interface logic includes Auto Command Mode (ACM) logic, an advanced state machine capable of handling a variety of complex SCSI sequences without microprocessor intervention. The microprocessor can queue up to four ACM commands into the ACM Command FIFO to create even more sophisticated command sequences. The SCSI block interfaces directly with the buffer manager via an internal speed matching FIFO. This FIFO, plus the bandwidth capabilities of the buffer manager guarantee sustained full speed transfers across the SCSI bus. The high level of automation of the ACM minimizes SCSI bus overhead. The net result is maximized performance with minimum SCSI bus bandwidth utilization.

The disk formatter performs the serialization and deserialization of data. If provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the disk formatter is an advanced programmable sequencer which is flexible enough to interface to a wide variety of read/write channels. The sequencer can contain 31 instructions, each of which is 5 bytes (40 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The flexible disk interface can be configured through a wide range of capabilities. This allows the SSI 32C9022 to interface with nearly any read/write channel and allows the user of the SSI 32C9022 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9022 controller and the SSI 32D4782 Combination Read Channel, you are guaranteed a problem free interface.

Within the disk formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 32-bit ECC for headers and an 88-bit Reed Solomon code for data. If the checker detects an error in an 88-bit Reed Solomon data field, the syndrome information is transferred into the corrector. The corrector performs the necessary operations to determine if the error was correctable and interfaces directly with the buffer controller to perform the correction automatically. The corrector performs its correction within one half of a sector time. This guarantees that the corrector will always be available to correct the next sector if necessary.

As its name implies, the buffer manager manages the data buffer of the controller. The buffer manager can support either SRAM or DRAM. When configured to operate with DRAM, the buffer manager automatically performs necessary refresh cycles. The buffer manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. The buffer manager interfaces with the buffer memory, the SCSI Interface block, the data path of the disk formatter block, the ECC corrector and the microprocessor. If more than one of these devices requires access to the buffer memory, the buffer manager arbitrates the requests automatically. The buffer manager of the SSI 32C9022 can sustain SCSI operations at the rate of 10 megabytes per second, disk formatter operations at 48 megabits per second (6 megabytes per second) and still have sufficient bandwidth left to handle on-the-fly ECC corrections and microprocessor accesses without degrading performance on any of the interfaces.

PIN DESCRIPTION

The following convention is used in the pin description:

(I) denotes an input
(O) denotes an output
(Z) denotes a tri-state output
(OD) denotes an open drain output

GENERAL

NAME	TYPE	DESCRIPTION
VDD	–	POWER SUPPLY PIN
GND	–	GROUND

HOST INTERFACE

$\overline{SDBP}$	I/O	SCSI DATA BUS PARITY. Odd parity bit for the SCSI data bus.
$\overline{SDB}(7:0)$	I/O	SCSI DATA BUS BITS 7-0.
$\overline{ATN}$	I	ATTENTION. This active low signal is used by the initiator to request a message out phase.
$\overline{BSY}$	I/O	BUSY. This active low signal is used to indicate when the bus is active.
$\overline{ACK}$	I	ACKNOWLEDGE. This active low signal is used in the handshake protocol to indicate the completion of a data byte transfer.
$\overline{SRST}$	I	SCSI RESET. This active low signal is used to reset the SCSI controller.
$\overline{MSG}$	O	MESSAGE. This active low signal is used to indicate a message phase.
$\overline{SEL}$	I/O	SELECT. This active low signal is used to indicate either a selection or reselection phase.
C/$\overline{D}$	O	COMMAND/DATA. This signal is used to indicate either a command or data phase.
$\overline{REQ}$	O	REQUEST. This active low signal is used in the handshake protocol to initiate a data byte transfer.
I/$\overline{O}$	I/O	INPUT/OUTPUT. This signal is used to indicate the direction of data transfer.
GPIO(2:0)	I/O	INPUT/OUTPUT. These pins are used to indicate the SCSI ID of the target device. The pins can be programmed as outputs for test purposes only.

DISK INTERFACE

INDEX	I	INDEX. Input for index pulse received from the drive.
INPUT/ OUTPUT	I/O	DISK SEQUENCER INPUT/OUTPUT. A general purpose control (output) and status (input) pin configured by the Output Enable Bit of Register 71H, bit 7. At power-on, this pin is an input. As an input, it can be used to synchronize the disk sequencer to an external event. As an output, it is controlled by bit 2 of the Control Field of the disk sequencer.
INPUT	I	INPUT. This pin can be used to synchronize the disk to an external event.

DISK INTERFACE (continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{AMD}}$/ SECTOR	I	ADDRESS MARK DETECT/SECTOR. This pin is used in the hard sector mode as the sector input. A pulse on this pin indicates a sector mark is found. In the soft sector mode, a low-level input indicates an address mark was detected. The device powers up in soft sector default mode.
RG	O	READ GATE. During disk data read, this pin is asserted. Active high.
WG	O	WRITE GATE. During disk data write, this pin is asserted. Active high.
RRCLK	I	READ/REFERENCE CLOCK. This is a clock signal generated from an external data synchronizer. This clock is used to synchronize the input NRZ data and clock the disk formatter of the chip.
WCLK	O	WRITE CLOCK. This signal clocks the NRZ data out in the dual NRZ interface mode.
NRZ1	I/O	NON RETURN TO ZERO 1. In dual NRZ mode, this signal is the most significant bit read data input from the disk drive when the read gate signal is asserted; it is the most significant bit write data output to the disk drive when the write gate signal is asserted. In single NRZ mode, this signal is not used and should be grounded. NRZ1 is the leading bit of the bit pair. In Write mode, the MSB of the data bytes always appears on NRZ1.
NRZ0	I/O	NON RETURN TO ZERO. In dual NRZ mode, this signal is the least significant bit read data input from the disk drive when the read gate signal is asserted; it is the least significant bit write data output to the disk drive when the write gate signal is asserted. In single NRZ mode, this signal is used to transfer NRZ data to/from the read channel chip.
FAULT	I	FAULT. This input when asserted indicates to the chip that a fault has occurred with the disk. The disk sequencer will stop and both RG and WG pins will be deasserted.

MICROPROCESSOR INTERFACE

$\overline{\text{RST}}$	I	RESET. An asserted low input generates a component reset that holds the internal registers at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals are set to the high-Z state during the assertion of this signal.
ALE/M/$\overline{\text{NM}}$	I	ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high or left floating after reset, the microprocessor interface is configured as non-multiplexed. When driven low, then the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs.
CS	I	CHIP SELECT. Active high signal, when asserted, the internal registers of the SSI 32C9022 can be accessed.
$\overline{\text{WR}}$/R/$\overline{\text{W}}$	I	WRITE STROBE/READ/WRITE. In the Intel bus mode, when an active low signal is present with CS signal high, the data is written to the internal registers. In the Motorola bus mode, this signal acts as the R/$\overline{\text{W}}$ signal.

MICROPROCESSOR INTERFACE (continued)

NAME	TYPE	DESCRIPTION
$\overline{RD}$/DS/$\overline{DS}$	I	READ STROBE/DATA STROBE. When the Intel bus control interface is selected (the I/$\overline{MC}$ is high), this signal acts as the $\overline{RD}$ signal. When the read strobe signal is asserted low and the CS signal is asserted high, the data from the specified register will be driven to the AD signals. When the Motorola bus control interface is selected (the I/$\overline{MC}$ is low) this signal acts as the data strobe signal. A high on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a read operation. A low on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a write operation. Note when non-multiplexed Motorola bus configuration is chosen, the data strobe is an active low input.
$\overline{DINT}$	O,OD,Z	DISK INTERRUPT. An active low signal indicates the controller is requesting microprocessor service from the disk side. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-Z state. Register 4F bit 3 enables the pull-up.
$\overline{SINT}$	O,OD,Z	SCSI INTERRUPT. This signal is generated by the SCSI controller and is an interrupt line to the microprocessor. It is programmable for either a push-pull or open drain output circuit. This signal powers up in the high-Z state. The interrupt is sourced from the SCSI Interrupt Register. Register 4F bit 3 enables the pull-up. This signal is also programmable to be either an active high or low interrupt.
AD(7:0)	I/O	ADDRESS/DATA BUS. When configured in the Intel mode, these lines are multiplexed, bidirectional microprocessor register address and data lines. When configured in the Motorola mode, these lines are bidirectional data lines.
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS: These signals are nonmultiplexed address input or latched address output lines.
READY	O	READY: When this signal is deasserted low, the microprocessor shall insert wait states to allow time for the chip to respond.
I/$\overline{MC}$	I	INTEL/MOTOROLA: This signal selects the microprocessor interface to be used. When this signal is asserted high, it selects the Intel bus control interface. When this signal is deasserted low, it selects the Motorola bus control interface. This signal has an internal pull-up to allow the default selection of the Intel bus control interface.

BUFFER MANAGER INTERFACE

BA(15:0)	O	BUFFER MEMORY ADDRESS LINES 15 through 0. Active high, for direct connection to a Static or Dynamic RAM address lines.
BA16/$\overline{RAS}$	O	BUFFER MEMORY ADDRESS 16: In SRAM mode, for direct connection to a Static RAM address line 16. ROW ADDRESS STROBE: In DRAM mode, for direct connection to a Dynamic RAM Row Address Strobe signal.
BA17/$\overline{CAS}$	O	BUFFER MEMORY ADDRESS 17: In SRAM mode, for direct connection to a Static RAM address line 17. ROW ADDRESS STROBE: In DRAM mode, active low, for direct connection to a Dynamic RAM Column Address Strobe signal.

BUFFER MANAGER INTERFACE

NAME	TYPE	DESCRIPTION
BD(7:0)	I/O	BUFFER MEMORY DATA BUS. 7 through 0. Active high, buffer data bus that connects directly to the buffer RAM data lines.
BDP	I/O	BUFFER MEMORY DATA PARITY. This signal provides odd parity for the buffer memory data bus during transfers to/from the buffer memory to the buffer RAM.
$\overline{MOE}$	O	MEMORY OUTPUT ENABLE. In SRAM mode this signal is asserted low when every buffer memory access is active. In DRAM mode this signal is asserted low only for buffer memory read operation.
$\overline{MS}$	O	MEMORY SELECT. An active low signal indicates external memory is selected.
$\overline{WE}$	O	WRITE ENABLE. Active low, write enable for the buffer RAM.
SYSCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address bits, write enable $\overline{WE}$, and memory output enable $\overline{MOE}$.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

PARAMETER	RATING
Power Supply Voltage, VCC	7V
Ambient Temperature	0 to 70°C
Storage Temperature	-65 to 150°C
Power Dissipation	750 mW
Input, Output pins	-0.5 to VCC+0.5V

ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Power Supply Voltage	VCC		4.50		5.50	V
Supply Current	ICC	Ta = 25°C Outputs Unloaded			50	mA
Supply Current	ICCS				250	µA
Input Low Voltage	VIL		-0.5		0.8	V
Input High Voltage	V0IH		2.0		VCC+0.5	V
Output Low Voltage	VOL	All pins except SCSI interface, IOL = 2 mA			0.4	V
Output Low Voltage	VOL	SCSI interface pins, IOL = 48 mA			0.5	V
Output High Voltage	VOH	IOH = -400 µA			2.4	V
Input Leakage Current	IL	0 < VIN < VCC	-10		10	µA
Input Capacitance	CIN				10	pF
Output Capacitance	COUT				10	pF

MICROPROCESSOR INTERFACE TIMING
Multiplexed Interface Timing Parameters (Figures 2-5)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
ALE width	Ta		20			ns
Address valid to MA(7:0) valid	Tma				30	ns
$\overline{RD}$ width	Tr		80			ns
Address valid to ALE ↓	As		5			ns
ALE ↓ to address invalid	Ah		10			ns
CS valid to $\overline{RD}$ ↓ or DS ↑	Cs		20			ns
$\overline{RD}$ ↑ or DS ↓ to CS ↓	Ch		0			ns
$\overline{RD}$ ↓ or DS ↑ to read data valid	Tda				60	ns
DS width	Tds		80			ns
$\overline{RD}$ ↑ or DS ↓ to read data invalid	Tdh		0		25	ns
R/$\overline{W}$ valid to DS ↑	Tsrw		20			ns
DS ↓ to R/$\overline{W}$ invalid	Thrw		20			ns
$\overline{RD}$ ↓ to READY ↓ (Intel) or DS ↑ to READY ↓ (Motorola)	Tdrdy				30	ns
Write data valid to $\overline{WR}$ ↑ or DS ↓	Wds		40			ns
$\overline{WR}$ ↑ or DS ↓ to write data invalid	Wdh		10			ns

Note: ↑ indicates rising edge ↓ indicates falling edge

Non-Multiplexed Bus Interface Timings (Figure 6)

MA(7:0) valid to DS ↓	Tmas		5			ns
DS ↑ to MA(7:0) invalid	Tmah		5			ns
CS valid to DS ↓	Cs		20			ns
DS ↑ to CS ↓	Ch		0			ns
DS ↑ to read data valid	Tda				60	ns
DS width	Tds		80			ns
DS ↑ to read data invalid	Tdh		0		25	ns
R/$\overline{W}$ valid to DS ↓	Tsrw		20			ns
DS ↑ to R/$\overline{W}$ invalid	Thrw		20			ns
DS ↑ to READY ↓ (Motorola)	Tdrdy				30	ns
Write data valid to $\overline{WR}$ ↑ or DS ↓	Wds		40			ns
$\overline{WR}$ ↑ or DS ↓ to write data invalid	Wdh		10			ns

Note 1: ↑ indicates rising edge ↓ indicates falling edge
Note 2:Loading capacitor = 30 pF

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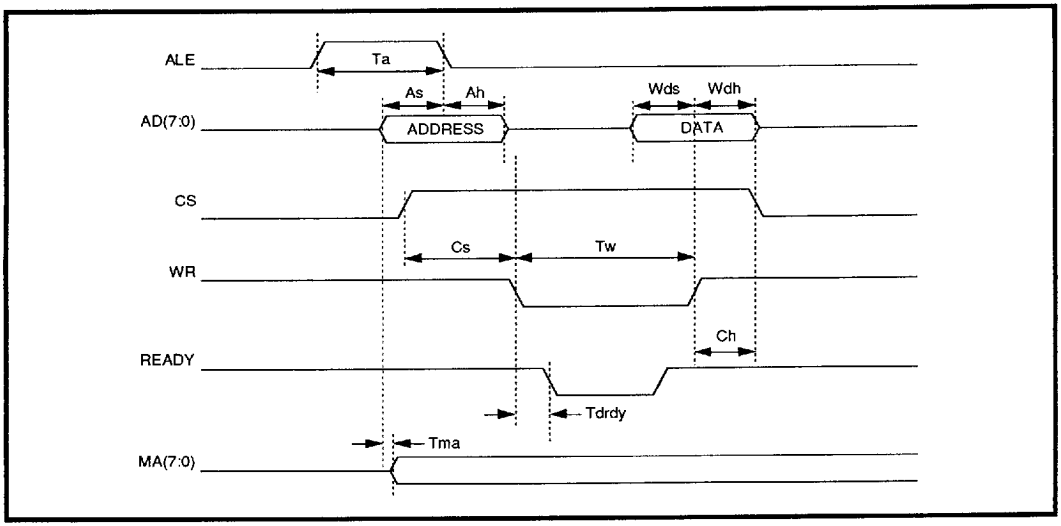

FIGURE 2: Intel Register Multiplexed Read Timing

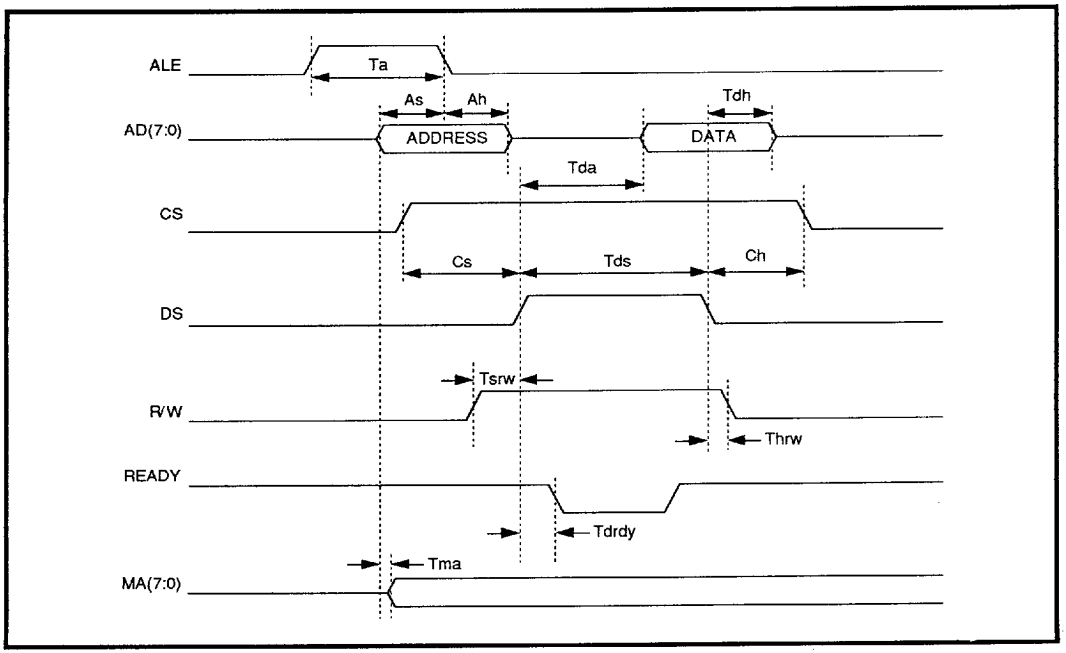

FIGURE 3: Motorola Register Multiplexed Read Timing

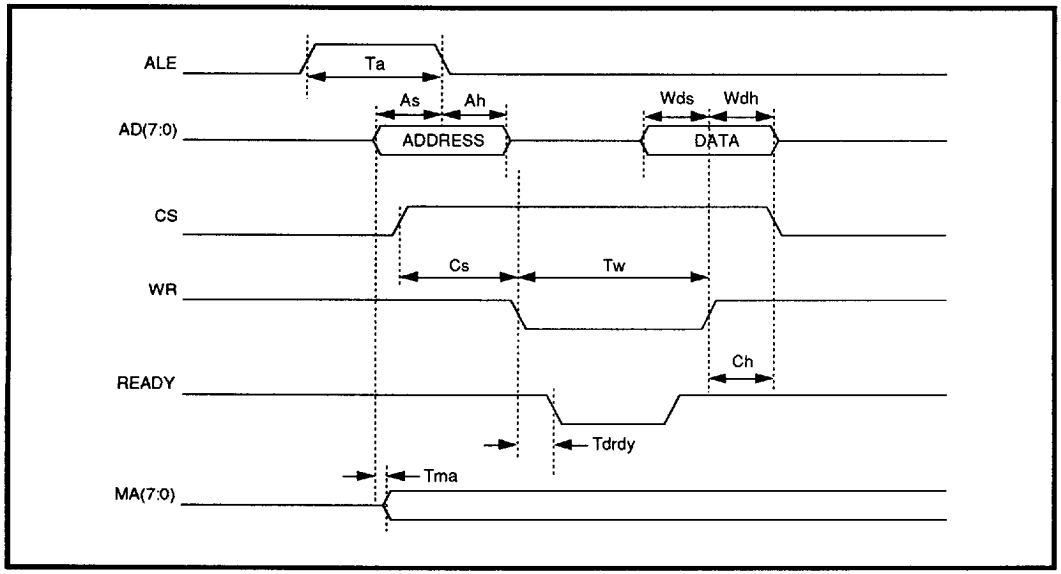

FIGURE 4: Intel Register Multiplexed Write Timing

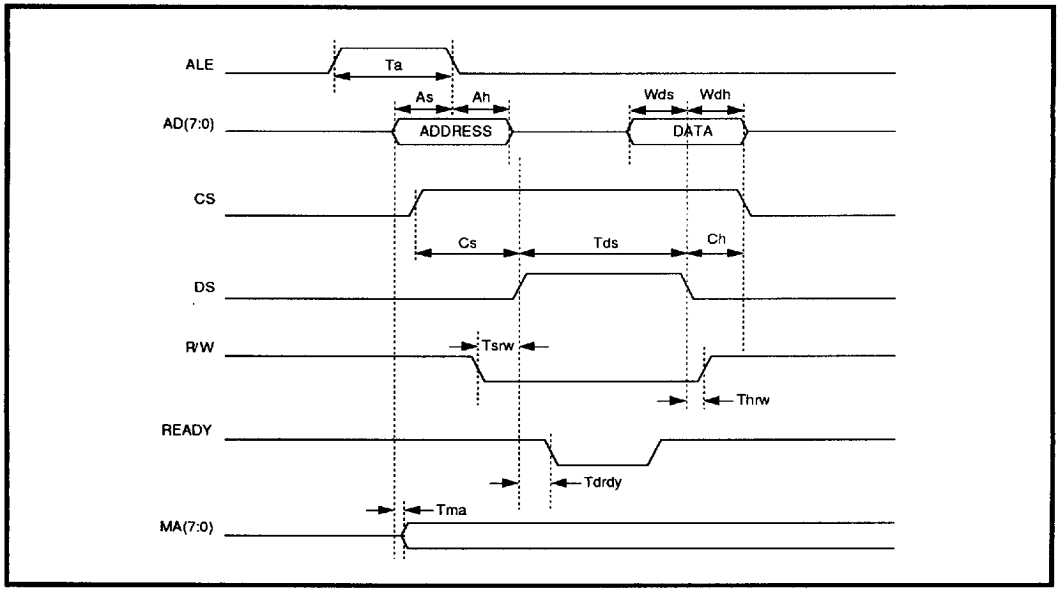

FIGURE 5: Motorola Register Multiplexed Write Timing

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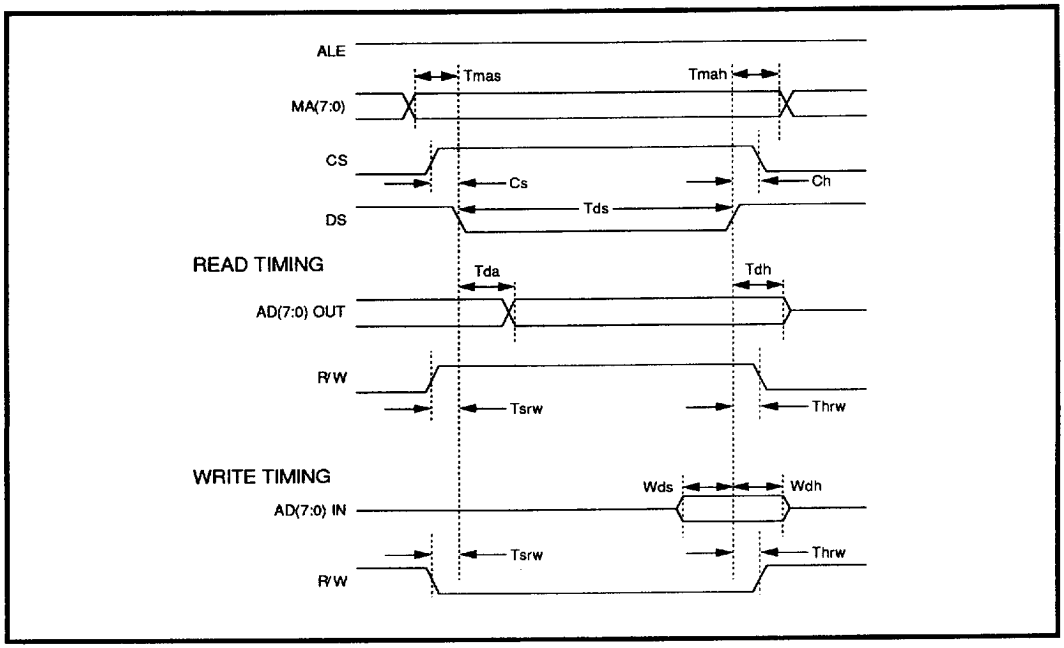

FIGURE 6: Non-Multiplexed Bus Timing Diagrams

ELECTRICAL SPECIFICATIONS (continued)

Disk Interface Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Dual bit interface RRCLK period	Td		40			ns
Single bit interface RRCLK period	Ts		20.8			ns
Dual bit interface RRCLK high/low time	Td/2		16			ns
Single bit interface RRCLK high/low time	Ts/2		8.5			ns
RRCLK rise/fall time	Tr, Tf				3	ns
NRZ in valid to RRCLK ↑	Dis		3			ns
RRCLK ↑ to NRZ in invalid	Dih		3			ns
$\overline{AMD}$ valid to RRCLK ↑	As		3			ns
RRCLK ↓ to WCLK ↓	Tckd				8	ns
RRCLK ↓ to NRZ out valid	Dvr				18	ns
WCLK ↓ to NRZ out valid	Dv				±2	ns

Note: ↑ indicates rising edge ↓ indicates falling edge
Loading capacitor = 10 pF

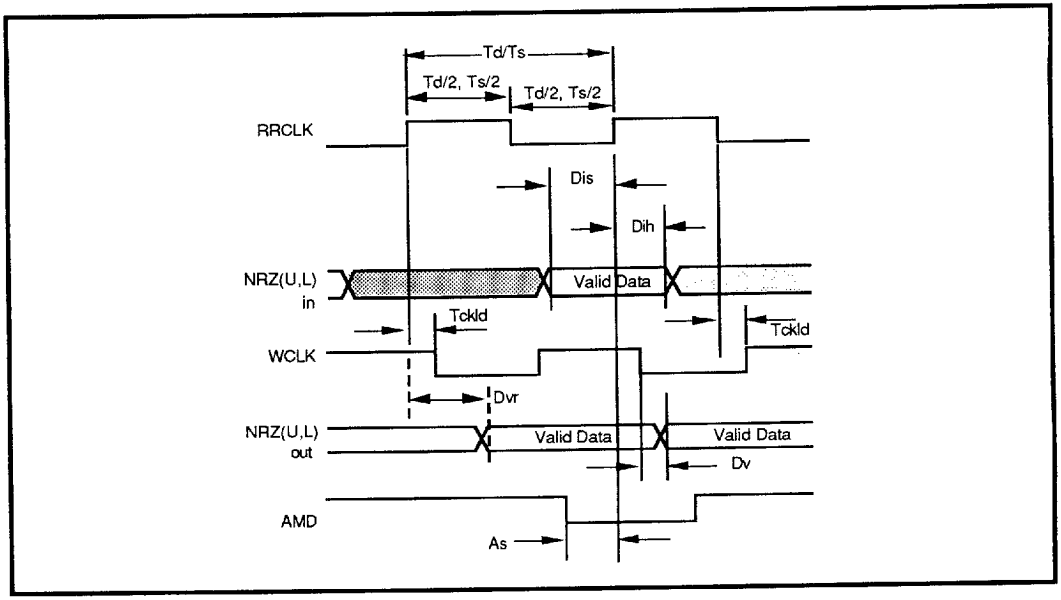

FIGURE 7: Disk Interface Timing

ELECTRICAL SPECIFICATIONS (continued)

BUFFER MEMORY READ/WRITE TIMING PARAMETERS (Figures 8 through 13)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
SYSCLK period	T		25			ns
SYSCLK ↑ to address valid (Note 1)	Tav				18	ns
SYSCLK ↑ to $\overline{MOE}$↓ (Note 1)	Tmv				18	ns
SYSCLK ↑ to $\overline{MOE}$↑ (Note 1)	Tmh				18	ns
SYSCLK ↑ to $\overline{WE}$↓ (Note 1)	Twv				18	ns
SYSCLK ↑ to $\overline{WE}$↑ (Note 1)	Twh				18	ns
SYSCLK ↑ to data out valid (Note 1)	Tdov				18	ns
SYSCLK ↑ to data out invalid (Note 1)	Tdoh				18	ns
Data in valid to MOE ↑ (SRAM)	Tdis		5			ns
Data in valid to $\overline{CAS}$ ↑ (DRAM)						
$\overline{MOE}$ ↑ to data in valid (SRAM)	Tdih		0			ns
$\overline{CAS}$ ↑ to data in valid (DRAM)						
SYSCLK ↑ to $\overline{RAS}$↓ (Note 1)	Trv				18	ns
SYSCLK ↑ to $\overline{RAS}$↑ (Note 1)	Trh				18	ns
SYSCLK ↑ to row address valid (Note 1)	Trav				18	ns
SYSCLK ↑ to row address invalid (Note 1)	Trah				18	ns
SYSCLK ↑ to $\overline{CAS}$↓ (Note 1)	Tcv				18	ns
SYSCLK ↑ to $\overline{CAS}$↑ (Note 1)	Tch				18	ns
SYSCLK ↑ to column address valid (Note 1)	Tcav				18	ns
SYSCLK ↑ to column address invalid	Tcah		0			ns

BUFFER MEMORY READ/WRITE FUNCTIONAL PARAMETERS (Figures 8 through 13) (continued)

PARAMETER		CONDITIONS	MIN	UNIT
Trwl	$\overline{RAS}\downarrow$ to $\overline{RAS}\uparrow$	Notes 2, 3	((RWL + 3)•T)	ns
Trwh	$\overline{RAS}\uparrow$ to $\overline{RAS}\downarrow$	Notes 2, 4	((RWH + 1)•T)	ns
Tcwl	$\overline{CAS}\downarrow$ to $\overline{CAS}\uparrow$	Note 2	((CWL + 1)•T)	ns
Tcwl	$\overline{CAS}\uparrow$ to $\overline{CAS}\downarrow$	Notes 2, 5	((CWL + 1)•T)	ns

Note: Loading capacitance = 30 pF

Note 1: The measured delay for any of the signal indicated by this note will not vary from the measured delay of any other signal indicated by this note by more than ±2 ns.

Note 2: RWL, RWH, CWL and CWH are fields in the Buffer Manager Timing Control Register (54H). Each is a two bit field which can contain a value of 0, 1, 2, or 3. These values determine the minimum number of SYSCLK periods (T) for the associated signal width.

Note 3: The minimum width value of Trwl will be generated for refresh cycles and for any buffer memory access cycle except when multiple page mode accesses are performed. When multiple page mode accesses are performed, the width of the $\overline{RAS}$ low pulse is extended until the end of the last $\overline{CAS}$ low cycle.

Note 4: The minimum value of Trwh will be generated whenever the Buffer Manager determines that a buffer request is pending at the completion of the current memory cycle and a page mode access can not be used either because page mode operation is not enabled or the needed location is not within the current page.

Note 5: The minimum value of Tcwh will be generated only between consecutive page mode accesses.

Note 6: $\overline{MS}$ will rise only if the Buffer Manager determines that no additional requests for buffer access are pending. If the Buffer Manager determines that another access is to be Made, $\overline{MS}$ is kept low between the accesses for improved speed.

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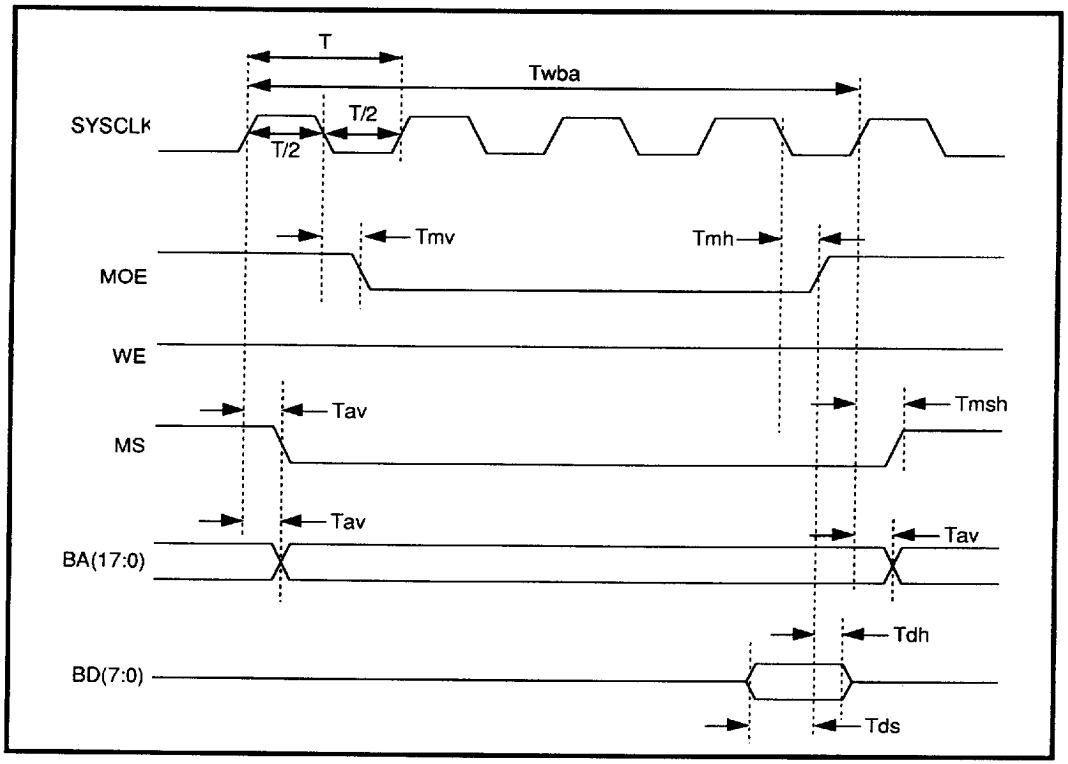

Note: Twba is a functional parameter that gives the duration of one RAM data buffer access cycle in SYSCLK periods. The value is programmed in bits 1-0 of register 54H. These examples show Twba = 4T.

FIGURE 8: SRAM Read Timing

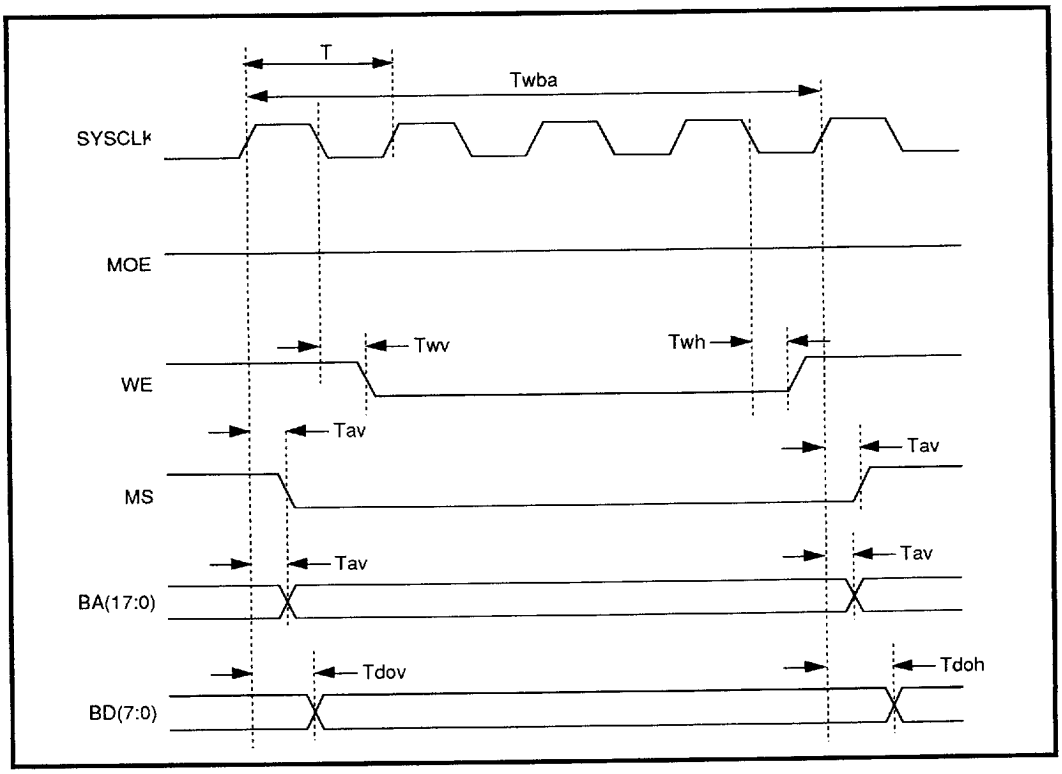

FIGURE 9: SRAM Write Timing

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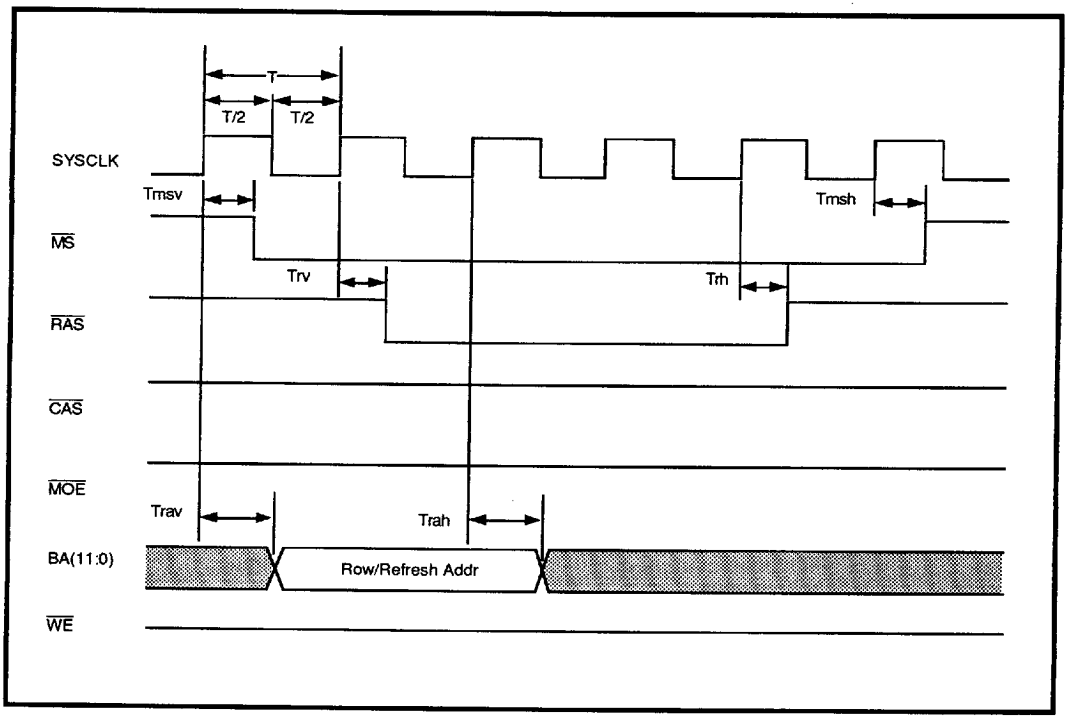

FIGURE 10: DRAM Timing, Refresh Cycle (Shown with WRL = 0)

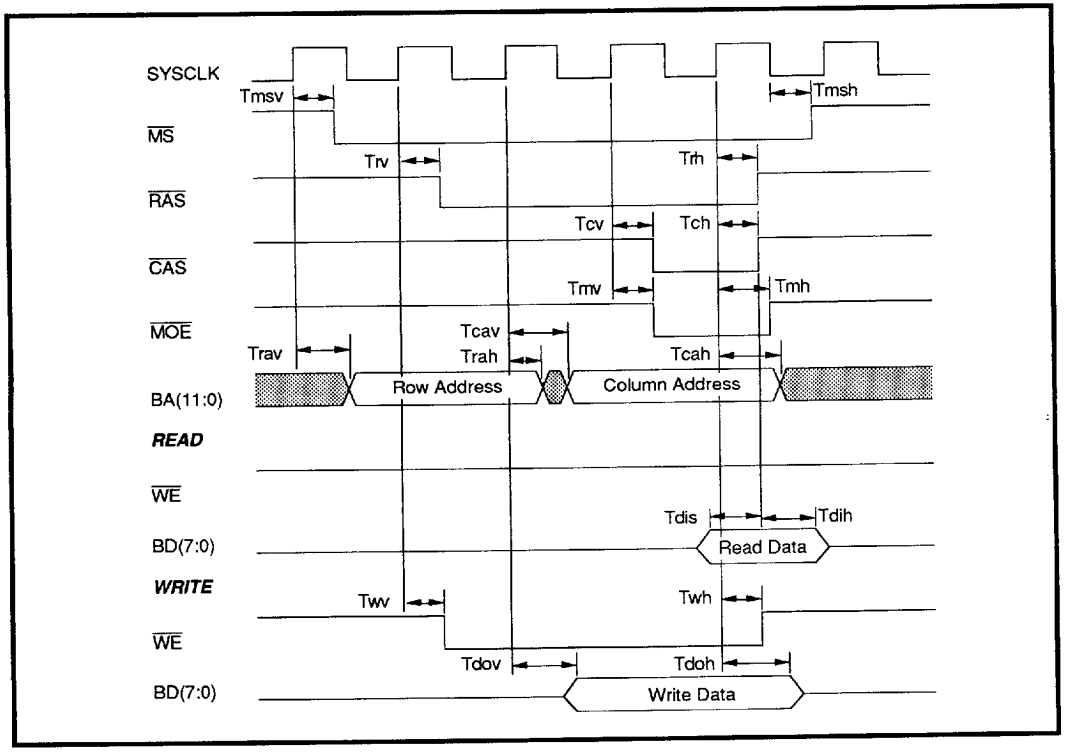

FIGURE 11: DRAM Timing, Standard Cycle (Shown with RWL = 0 and CWL = 0)

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ELECTRICAL SPECIFICATIONS (continued)

SCSI Asynchronous Timing Parameters

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Data Setup to $\overline{ACK}\downarrow$	Tods	SCSI Output Phase	5			ns
Data Hold from $\overline{ACK}\downarrow$	Todh	SCSI Output Phase	12			ns
$\overline{ACK}\downarrow$ to $\overline{REQ}\uparrow$	Talrh				49	ns
Data Setup to $\overline{REQ}\downarrow$	Tids	SCSI Input Phase	80			ns
Data Hold from $\overline{ACK}\downarrow$	Tidh	SCSI Input Phase	29			ns

Note: All timing parameters are measured with 200 pf load, two SCSI terminator loads, $\overline{ACK}$ filter turned off.

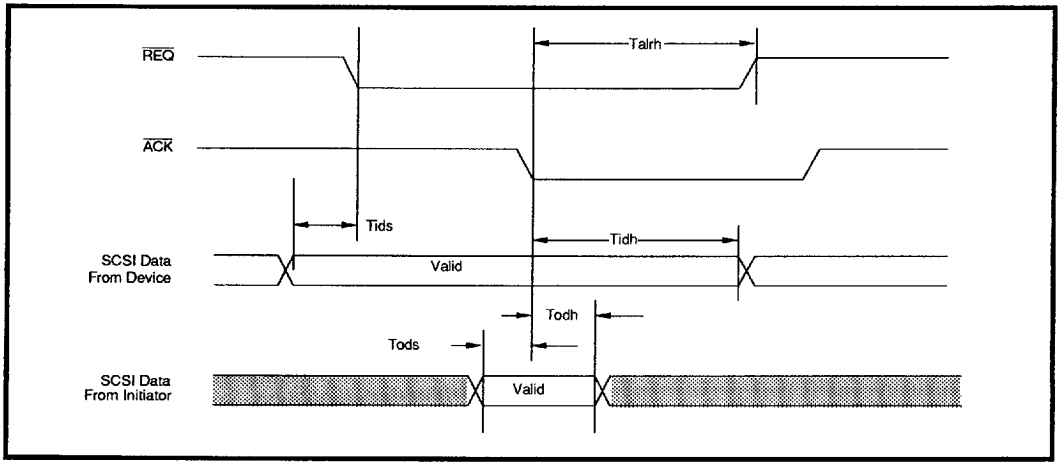


FIGURE 14: SCSI Asynchronous Timing

SCSI Synchronous Timing Parameters

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
$\overline{REQ}$ Assertion Time	Trh		37		48	ns
$\overline{REQ}$ Deassertion Time	Trl		63		52	ns
Setup time SCSI Data to $\overline{REQ}\downarrow$	Tids	Write to SCSI bus	43			ns
Hold time $\overline{REQ}\downarrow$ to SCSI Data invalid	Tidh	Write to bus	43			ns
Minimum $\overline{ACK}$ Assertion Width Required	Tal		10			ns
Data Setup to $\overline{ACK}\downarrow$	Tods	Read from the SCSI bus	5			ns
Data Hold from $\overline{ACK}\downarrow$	Todh	Read from the SCSI bus	12			ns

Note: All timing parameters are measured with 200 pf load, two SCSI terminator loads, $\overline{ACK}$ filter turned off.

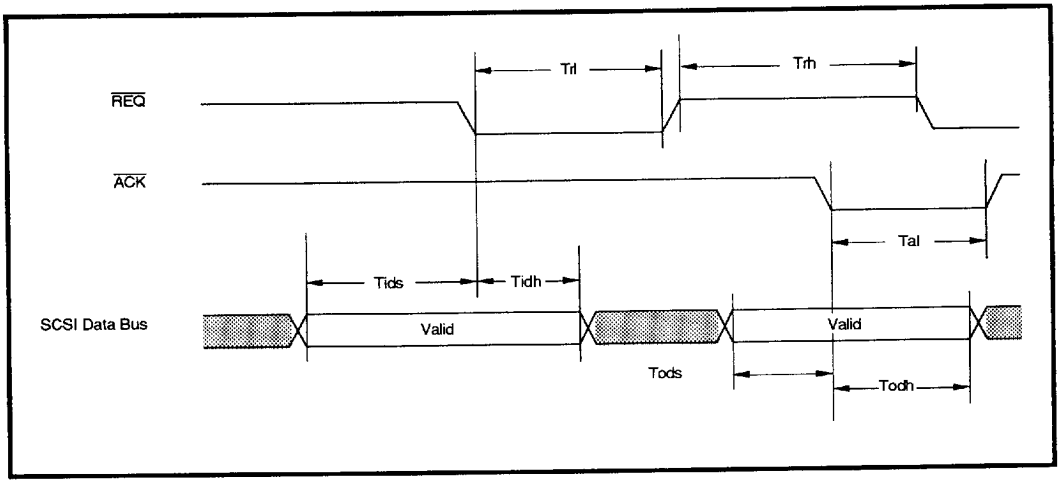


FIGURE 15: SCSI Synchronous Timing

ELECTRICAL SPECIFICATIONS (continued)

Synchronous Data In/Out Phase

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Synchronous Transfer Period	Txtrp*	(see note)				ns
SYSFREQ high to $\overline{REQ}$ low	Tsrl				50	ns
SYSFREQ high to $\overline{REQ}$ high	Tsrh				60	ns
SYSFREQ high to data out valid	Tdov				40	ns
Data setup to $\overline{ACK}$ low	Tdsu		55			ns
Data hold from $\overline{ACK}$ low	Tdh		40			ns

Note: Txtrp is the Synchronous Transfer Period as defined by the Synchronous Control Register (Reg: 43H). SYSFREQ is a function of the BUFCLK and is determined by the prescale value as defined by the Clock Control Register (Reg: 49H).

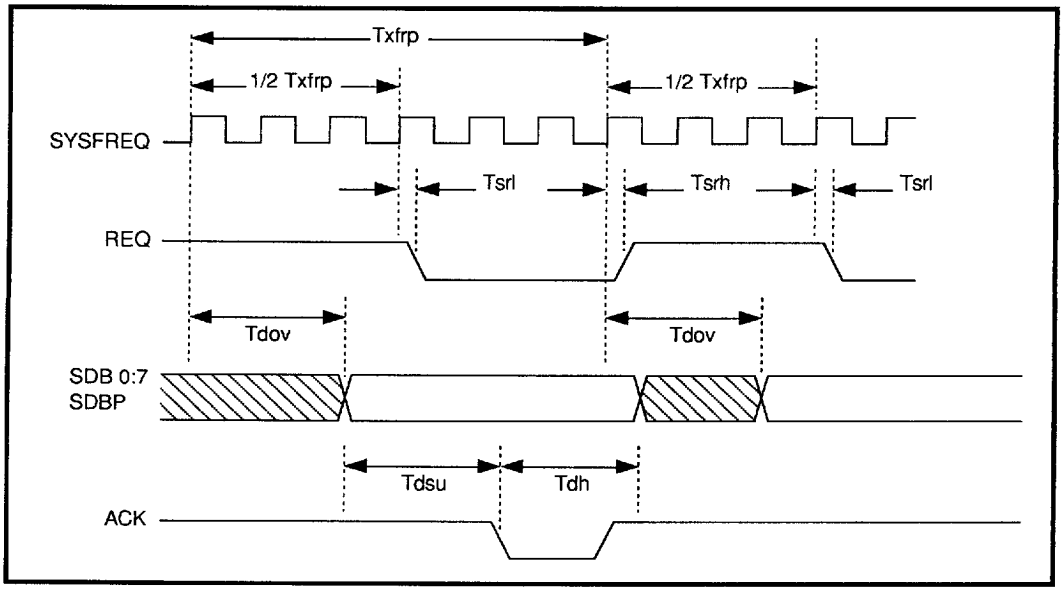


FIGURE 16: Even Number of SYSFREQ Cycles/SCSI Transfer Period

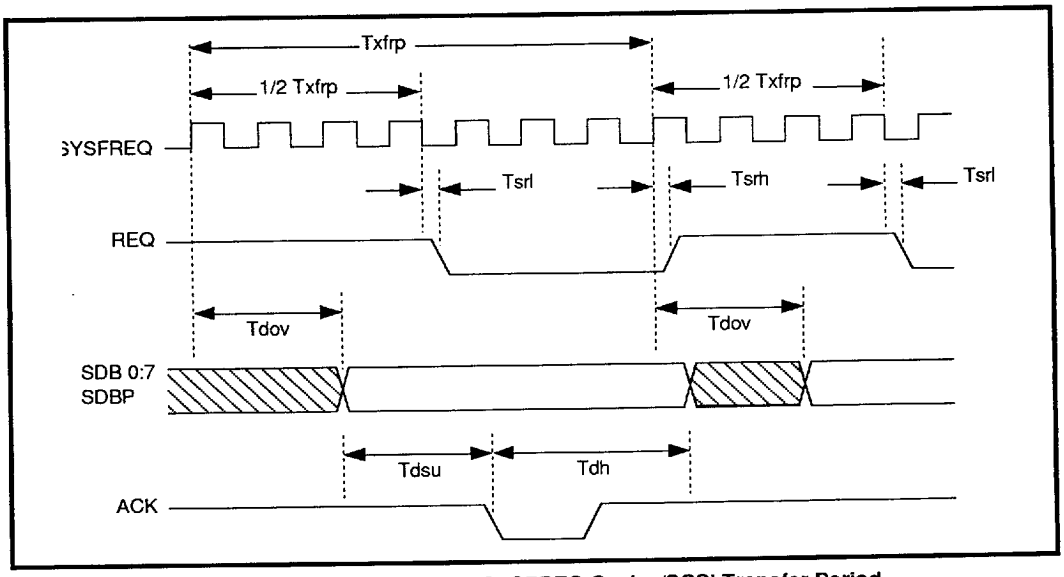


FIGURE 17: Odd Number of SYSFREQ Cycles/SCSI Transfer Period

Wait for Selection

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Bus Settle Delay (400 ns) Tbsd to the assertion of $\overline{BSY}$		3T + 90		4T + 90	ns

Note: T is the SCSI Clock Period (SCP) as defined in Register 49H (CLKCTL).

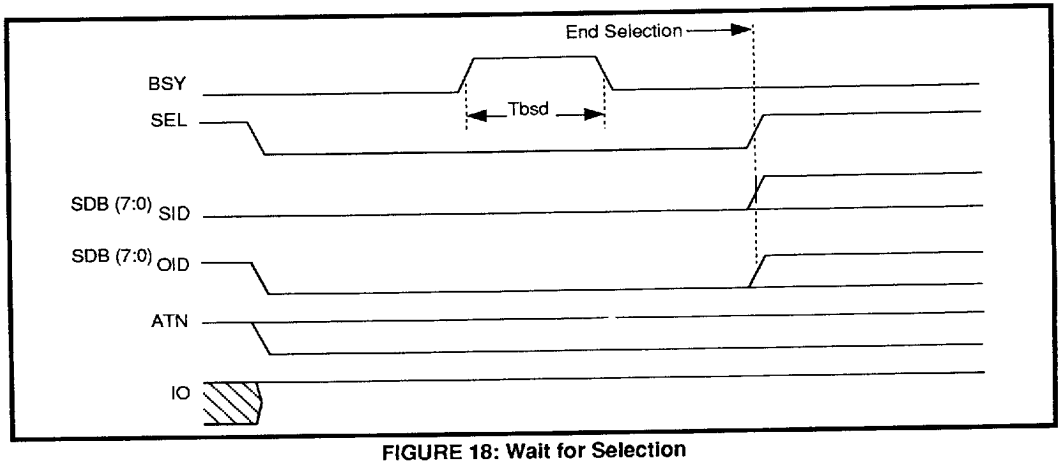


FIGURE 18: Wait for Selection

ELECTRICAL SPECIFICATIONS (continued)

Arbitration

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Bus Settle Delay (400 ns) + Bus Free Delay (800 ns) to the assertion of BSY and $\overline{SDB}_{OID}$ Tbfsd		6T + 110		7T + 110	ns
Arbitration Delay (2.4 µsec) to the assertion of $\overline{SEL}$ (win) or deassertion of $\overline{BSY}$ and $\overline{SDB}_{OID}$ (lost) Tad		-		13T + 100	ns
Bus Clear Delay (800 ns)+ Bus Settle Delay (400 ns) to end of Arbitration Phase Tbcsd		-		6T + 100	ns

Note: T is the SCSI Clock Period (SCP) as defined in Register 61H (CLKCTL).

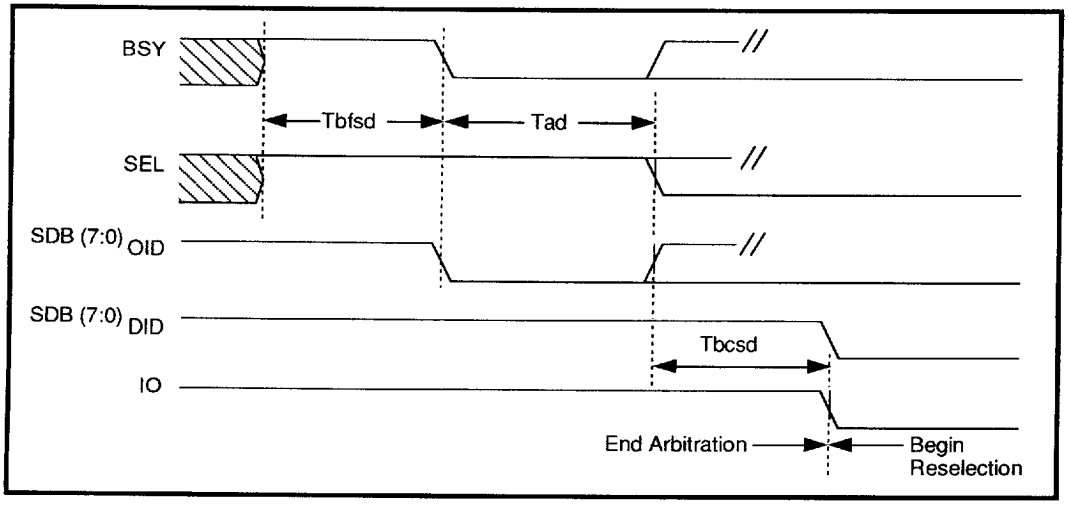


FIGURE 19: Arbitration

Reselection

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Bus Clear Delay (800 ns) + Tbcsd Bus Settle Delay (400 ns) to end of Arbitration Phase		-		6T + 100	ns
Two Deskew Delays Tdskd1 (90 ns) to the deassertion of $\overline{BSY}$		-		160	ns
Bus Settle Delay (400 ns) Tbsd to the assertion of $\overline{BSY}$		-		2T + 40	ns
Two Deskew Delays (90 ns) Tdskd2 to the deassertion of SEL, $\overline{SDB}_{OID}$, and $\overline{SDB}_{DID}$		1T +70		2T + 70	ns

Note: T is the SCSI Clock Period (SCP) as defined in Register 61H (CLKCTL).

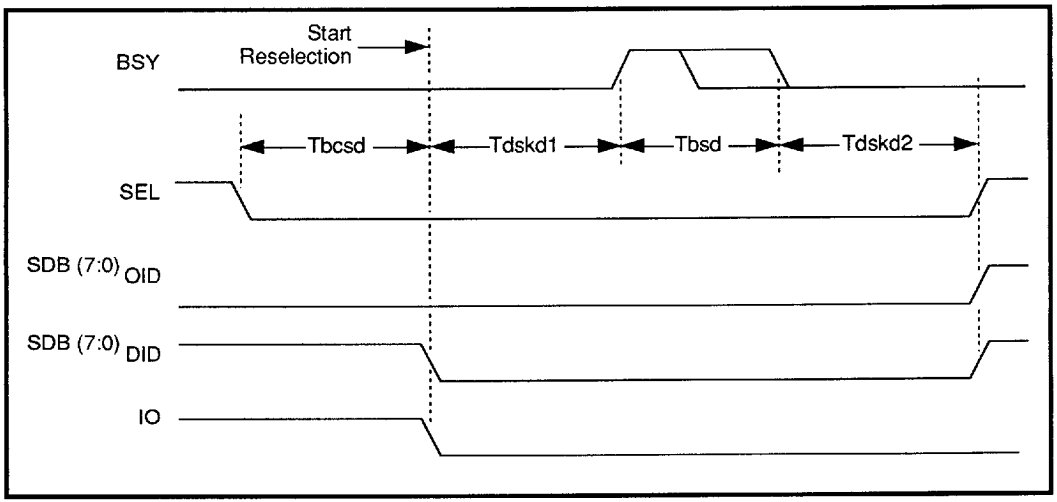
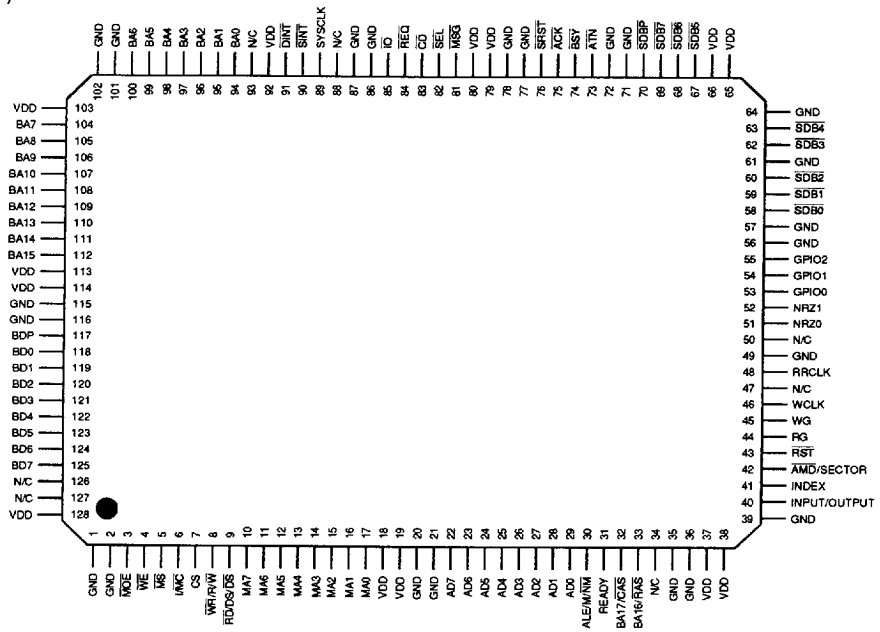


FIGURE 20: Reselection

SSI 32C9022
SCSI Combo Controller
48 Mbit/s; dual bit NRZ interface

PACKAGE PIN DESIGNATIONS

(Top View)



128-Lead QFP, TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
128-Lead TQFP	SSI 32C9022-CGT	SSI 32C9022-CGT
128-Lead QFP	SSI 32C9022-CG	SSI 32C9022-CG

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX: (714) 573-6914

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