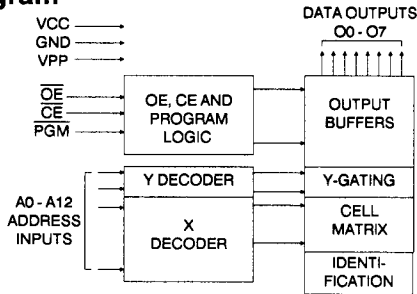## Features

- **Bipolar Speed in JEDEC Standard EPROM Pinout**
    Read Access Time - 45ns
    600 mil DIP or LCC packages
- **Low Power CMOS Operation**
    100 μA max. Standby
    75 mA max. Active at 10 MHz
- **High Output Drive Capability**
- **High Reliability Latch-Up Resistant CMOS Technology**
- **Fast Programming - 4ms/byte (typical)**
- **Two-line Control**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Full Military, Commercial and Industrial Temperature Ranges**

64K (8K x 8) High Speed UV Erasable CMOS EPROM
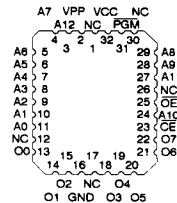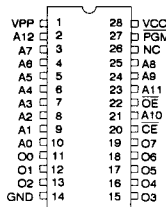
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Block Diagram

Description

The AT27HC64/64L chip family is a high-speed, low-power 65,536 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM), organized 8K x 8. The AT27HC64 is suited for very high speed applications, while the AT27HC64L features low Vcc Standby Current. Both require only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 45ns on the AT27HC64, making this part compatible with high performance systems. Power consumption is typically only 40mA in Active Mode on both parts and less than 20μA in Standby on the AT27HC64L.

Atmel's 1.5 micron, high speed CMOS technology provides optimum speed, low-power and high noise immunity. The high speed CMOS process is an extension of Atmel's high quality and highly manufacturable floating poly EPROM technology.

The AT27HC64/64L come in an industry standard JEDEC-approved 28-lead 64K EPROM pinout. The devices feature a two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention. Both parts are available in either 28-pin 600 mil DIP or 32-pad LCC packages.

Pin Configurations

Pin Name	Function
A0-A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect
O0-O7	Outputs

Description (Continued)

With a storage capacity of 8K bytes, Atmel's 27HC64/64L allow firmware to be stored reliably and to be accessed at bipolar PROM speeds. The AT27HC64/64L have exceptional output drive capability - source 4mA and sink 16mA per output.

The AT27HC64/64L have additional features to ensure high quality and efficient production use. The fast programming algorithm reduces the time required to program the chip and guarantees reliable programming. The Integrated Product Identification Code electronically identifies the device and manufacturing origin. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27HC64/64L is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using $12,000\,\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of $15W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias ....-55°C to +125°C

Storage Temperature ....-65°C to +150°C

Voltage on Any Pin with
Respect to Ground ....-2.0V to +7.0V[1]

Voltage on A9 with
Respect to Ground ....-2.0V to +14.0V[1]

V_{PP} Supply Voltage with
Respect to Ground ....-2.0V to +14.0V[1]

Integrated UV Erase Dose................ 7258 w∙sec/cm²

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is $V_{CC}+0.75V$ dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	Ai	V_{CC}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	$X^{(1)}$	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	X	V_{CC}	V_{CC}	High Z
Fast Program[2]	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	High Z
Product Identification[4]	V_{IL}	V_{IL}	V_{IH}	A9 = V_H [3] A0 = V_{IH} or V_{IL} A1-A12 = V_{IL}	V_{CC}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. $V_H = 12.0 \pm 0.5V$.

4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27HC64	AT27HC64 / AT27HC64L		
		-55	-70	-90	-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C[1]	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Notes: 1. AT27HC64 only.

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition			Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = -0.1V$ to $V_{CC} + 1V$				10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = -0.1V$ to $V_{CC} + 0.1V$				10	μA
I_{PP} [2]	V_{PP} [1] Read/Standby Current	$V_{PP} = 3.8$ to $V_{CC} + 0.3V$				20	μA
I_{SB1}/I_{SB2}	V_{CC} [1] Standby Current	I_{SB1} (CMOS) $\overline{CE} = V_{CC}$-0.3 to $V_{CC} + 1.0V$	AT27HC64L Com.			0.1/2	mA
			Ind.,Mil.			0.2/3	mA
		I_{SB2} (TTL) $\overline{CE} = 2.0$ to $V_{CC} + 1.0V$	AT27HC64 Com.			35/35	mA
			Ind.,Mil.			40/40	mA
I_{CC}	V_{CC} Active Current	$f = 10MHz, I_{OUT} = 0mA,$ $\overline{CE} = V_{IL}$	Com.			75	mA
			Ind.,Mil.			90	mA
V_{IL}	Input Low Voltage				-0.6	0.8	V
V_{IH}	Input High Voltage				2.0	$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 16mA$				.45	V
V_{OH}	Output High Voltage	$I_{OH} = -100\mu A$			V_{CC}-0.3		V
		$I_{OH} = -2.5mA$			3.5		V
		$I_{OH} = -4.0mA$			2.4		V
V_{PP}	V_{PP} Read Voltage	$V_{CC} = 5 \pm 0.5V$			3.8	5.5	V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.   2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT27HC64		AT27HC64 / AT27HC64L						
				-45		-55		-70		-90		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} [4]	Address to Output Delay	$\overline{CE} = \overline{OE}$ $= V_{IL}$	Com.,Ind.		45		55		70		90	ns
			Mil.				55[1]		70		90	ns
t_{CE} [3]	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$			45		55		70		90	ns
t_{OE} [3,4]	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$			25		30		35		40	ns
t_{DF} [2,5]	$\overline{OE}$ or $\overline{CE}$ High to Output Float	$\overline{CE} = V_{IL}$			25		30		35		40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE} = \overline{OE}$ $= V_{IL}$		0		0		0		0		ns

Notes: 1. AT27HC64 only.   2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]
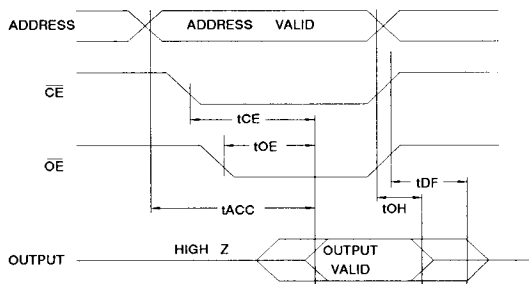
Notes:
1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.
   $C_L = 30pF$, add 10ns for $C_L = 100pF$.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first. t_{DF} is measured at $V_{OH}-0.5V$ or $V_{OL}+0.5V$ with $C_L=5pF$.
3. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels

t_R, $t_F < 5ns$ (10% to 90%)
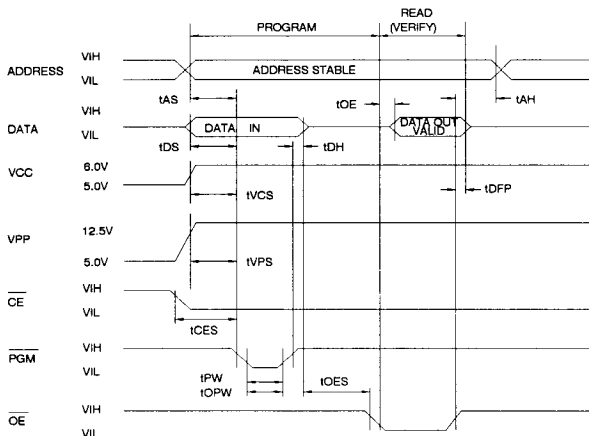
Output Test Load
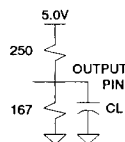
Note: $C_L=30pF$ including jig capacitance.

Pin Capacitance (f = 1MHz   T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	$V_{IN} = 0V$
C_{OUT}	8	12	pF	$V_{OUT} = 0V$

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]

Notes:
1. The Input Timing Reference is 0.0V for V_{IL} and 3.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27HC64/64L a $0.1\mu F$ capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

$T_A = 25 \pm 5^\circ C$, $V_{CC} = 6.0 \pm 0.25V$, $V_{PP} = 12.5 \pm 0.5V$

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		10	μA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	$I_{OL} = 16mA$		.4	V
V_{OH}	Output High Volt.	$I_{OH} = -4.0mA$	2.4		V
I_{CC2}	Vcc Supply Current (Program and Verify)			80	mA
I_{PP2}	Vpp Supply Current	$\overline{CE} = V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

$T_A = 25 \pm 5^\circ C$, $V_{CC} = 6.0 \pm 0.25V$, $V_{PP} = 12.5 \pm 0.5V$

Symbol	Parameter	Test Conditions* (see Note 1)	Min	Max	Units
t_{AS}	Address Setup Time		2		μS
t_{CES}	$\overline{CE}$ Setup Time		2		μS
t_{OES}	$\overline{OE}$ Setup Time		2		μS
t_{DS}	Data Setup Time		2		μS
t_{AH}	Address Hold Time		0		μS
t_{DH}	Data Hold Time		2		μS
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	Vpp Setup Time		2		μS
t_{VCS}	Vcc Setup Time		2		μS
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	(Note 3)	0.95	1.05	ms
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	(Note 4)	2.85	78.75	ms
t_{OE}	Data Valid from $\overline{OE}$			70	ns

*A.C. Conditions of Test:
Input Rise and Fall Times (10% to 90%) 5ns
Input Pulse Levels ....0.0V to 3.0V
Input Timing Reference Level 1.5V
Output Timing Reference Level 1.5V

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Initial Program Pulse width tolerance is 1msec±5%.
4. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.

Atmel's 27HC64/L Integrated Product Identification Code:

Codes	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	1	1F
Device Type	1	1	0	0	1	0	0	0	1	91

(The "Pins" header spans columns A0 through O0.)

Fast Programming Algorithm

Two $\overline{PGM}$ pulse widths are used to program; initial and over-program. Ai are set to address the desired byte. V_{CC} is raised to 6.0V. The first $\overline{PGM}$ pulse is 1ms. The programmed byte is then verified. If the byte programmed successfully, then an overprogram $\overline{PGM}$ pulse is applied for 3ms. If the byte fails to program after the first 1ms pulse, then up to 25 successive 1ms pulses are applied with a verification after each pulse. When the byte passes verification, the overprogram pulse width is 3X (times) the number of 1ms pulses required earlier (75ms max).

If the part fails to verify after 25 1ms pulses have been applied, it is considered as failed. After the first byte is programmed, the Ai are set to the next address repeating the algorithm until all required addresses are programmed. Then V_{CC} is lowered to 5.0V. All bytes subsequently are read to compare with the original data to determine if the device passes or fails.
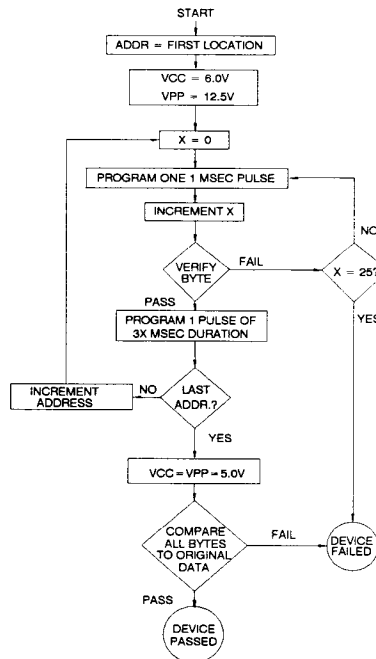
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Ordering Information

tACC (ns)	ICC (mA) Active	ICC (mA) Standby	Ordering Code	Package	Operation Range
45	75	35	AT27HC64-45DC AT27HC64-45LC	28DW6 32LW	Commercial (0°C to 70°C)
45	90	40	AT27HC64-45DI AT27HC64-45LI	28DW6 32LW	Industrial (-40°C to 85°C)
55	75	35	AT27HC64-55DC AT27HC64-55LC AT27HC64-55PC	28DW6 32LW 28P6	Commercial (0°C to 70°C)
55	90	40	AT27HC64-55DI AT27HC64-55LI AT27HC64-55PI	28DW6 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC64-55DM AT27HC64-55LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27HC64-55DM/883 AT27HC64-55LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	75	35	AT27HC64-70DC AT27HC64-70LC AT27HC64-70PC	28DW6 32LW 28P6	Commercial (0°C to 70°C)
70	90	40	AT27HC64-70DI AT27HC64-70LI AT27HC64-70PI	28DW6 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC64-70DM AT27HC64-70LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27HC64-70DM/883 AT27HC64-70LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	75	35	AT27HC64-90DC AT27HC64-90LC AT27HC64-90PC	28DW6 32LW 28P6	Commercial (0°C to 70°C)
90	90	40	AT27HC64-90DI AT27HC64-90LI AT27HC64-90PI	28DW6 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC64-90DM AT27HC64-90LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27HC64-90DM/883 AT27HC64-90LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

AT27HC64/L

Ordering Information

tACC (ns)	ICC (mA) Active	ICC (mA) Standby	Ordering Code	Package	Operation Range
55	75	0.1	AT27HC64L-55DC AT27HC64L-55LC	28DW6 32LW	Commercial (0°C to 70°C)
55	90	0.2	AT27HC64L-55DI AT27HC64L-55LI	28DW6 32LW	Industrial (-40°C to 85°C)
70	75	0.1	AT27HC64L-70DC AT27HC64L-70LC AT27HC64L-70PC	28DW6 32LW 28P6	Commercial (0°C to 70°C)
70	90	0.2	AT27HC64L-70DI AT27HC64L-70LI AT27HC64L-70PI	28DW6 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC64L-70DM AT27HC64L-70LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27HC64L-70DM/883 AT27HC64L-70LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	75	0.1	AT27HC64L-90DC AT27HC64L-90LC AT27HC64L-90PC	28DW6 32LW 28P6	Commercial (0°C to 70°C)
90	90	0.2	AT27HC64L-90DI AT27HC64L-90LI AT27HC64L-90PI	28DW6 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC64L-90DM AT27HC64L-90LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27HC64L-90DM/883 AT27HC64L-90LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	90	0.2	5962-85102 04 YX 5962-85102 04 ZX	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

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Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)