, INC.

27CX256
256K (32K x 8) CMOS High-Speed EPROM

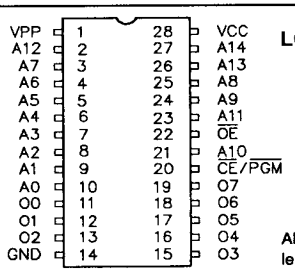
Features

- **Advanced CMOS EPROM Technology**
- **High Performance / Industry's Fastest**
  - — 27CX256C-35 t_{AA} = 35ns max
  - — 27CX256C-45 t_{AA} = 45ns max
  - — 27CX256C-55 t_{AA} = 55ns max
- **Low Power Consumption**
  - — 50mA Max Active
  - — 25mA Max Standby, TTL interface
  - — 1mA Max Standby, CMOS interface
- **TTL-Compatible I/O**
- **Reprogrammability**
  - — Adds convenience, reduces costs
  - — Windowed package for UV erasure
  - — Allows 100% factory testing
- **Programming Support**
  - — Supported by popular programmers
  - — Fast programming algorithm
  - — Auto Select mode feature
- **Packaging**
  - — JEDEC-standard 28-pin Ceramic

General Description

The ICT 27CX256 is a 262,144-bit CMOS high-speed UV-Erasable Programmable Read Only Memory, organized as 32K-bytes of 8 bits each. Available in a JEDEC-standard 28-pin package, the 27CX256 allows pin-compatible upgrades from 32K through 128K-bit EPROMS with minimal or no hardware changes. The 27CX256 is designed using an advanced CMOS EPROM technology which provides ultra-fast access times (35, 45, 55ns max) and a low active power consumption (50mA max). The power consumption is further reduced (1mA max) with its special CMOS standby mode, when pin $\overline{CE}$ is deselected. The high-speed of the 27CX256 makes it ideal for operation with fast 16-bit and 32-bit microprocessors, eliminating the necessity of wait states. The 27CX256's high density allows the storage of operating systems and applications software, freeing the system's RAM for other uses. Popular third party vendor EPROM programmers will support the 27CX256 programming. An Auto Select mode provides for foolproof programmer operation by allowing EPROM programmers to read a special code from the 27CX256 to identify manufacturer and part type.

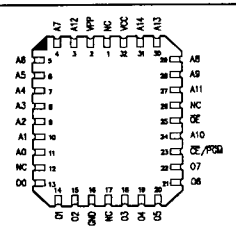
Pin Diagram DIP



Pin Names

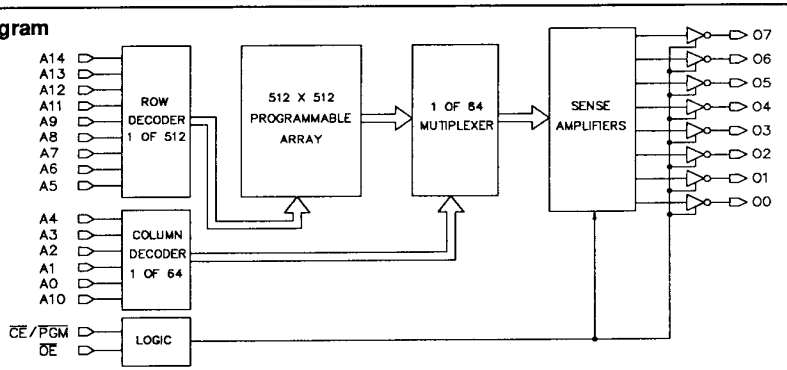
A0–A14	Address Inputs
O0-O7	Data Outputs
$\overline{CE}$/PGM	Chip Enable
$\overline{OE}$	Output Enable
GND	Ground
V_{CC}	Power Supply
V_{PP}	Power Supply (program)

LCC*



Also available in 32-pin rectangular plastic leaded chip carrier

Block Diagram



Functional Description

Erasure Characteristics

The 27CX256 is erased by exposure to an ultraviolet light source. For complete erasure, the recommended minimum integrated dose (UV intensity X exposure time) is 15 Watt-second/cm^2 of ultraviolet light with a wavelength of 2537 Å. For an ultraviolet lamp with a 12mW/cm^2 power rating, the exposure time should be approximately 20 minutes, with the device placed within one inch of the lamp during erasure. Exposing the CMOS EPROM to high-intensity UV light for extended periods may affect device reliability. Also, exposure to fluorescent light or sunlight may erase the EPROM. Therefore, an opaque label or substance should be placed over the package window if the device is used in such an environment.

Programming Mode

After erasure, all bits of the EPROM are set to 1's. Programming of the 27CX256 stores 0's in the selected bit positions. The program mode is entered when a voltage between 12.5V and 13.0V is applied to the VPP pin, while $\overline{CE}$/ $\overline{PGM}$ is held low and $\overline{OE}$ is high.
Programming support is available from third-party manufacturers. For more information on programming support and programming specifications, please contact ICT.

Read Mode

The 27CX256 has two control functions, Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$), which must both be held low for data to be accessed from the EPROM. $\overline{CE}$ is the power control and should be used for device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if the device is selected.
It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the read line from the system control bus. This will assure that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular device.
Assuming the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to the output (t_{CS}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The 27CX256 has two standby modes, a CMOS standby mode (when true CMOS devices are wired) and a TTL standby mode (when TTL level devices are wired). In the CMOS standby mode or power-down mode, the current consumed (I_{CC1}) is less than 1mA. During TTL standby mode the current (I_{CC2}) is less than 25mA, and the outputs O0-O7 are in the high impedance state, independent of $\overline{OE}$ input.

Auto Select Mode

The Auto Select Mode allows the reading out of a two-byte binary code from the EPROM that will identify its manufacturer and part type. This mode is intended for use by programming equipment for the purpose of automatically matching the device being programmed with its corresponding programming algorithm. The two codes identified are the Manufacturer code and the Device code.
These codes are given in the Mode table. All identifiers for manufacturers and devices will exhibit odd parity with the MSB (O7) defined as the parity bit.

Program Inhibit Mode

Multiple 27CX256 devices can be programmed in parallel by wiring all like inputs of the EPROMs except for $\overline{CE}$. Different data can also be programmed into each EPROM while in parallel. Devices with $\overline{CE}$ and $\overline{OE}$ held HIGH are inhibited from being programmed. The chosen device can then be programmed by setting $\overline{CE}$ to a LOW TTL level and applying 12.5V to VPP. (See mode table)

Program Verify Mode

A verify should be performed on the programmed bits of the 27CX256 to determine the correct programming of the EPROM.
This is accomplished by taking $\overline{CE}$ to V_{IH} and $\overline{OE}$ to V_{IL}, and applying 12.5V to VPP.

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	– 0.6 to +7.0	V
V_{IO}	Voltage Applied to All Pins Except A9,VPP	Relative to GND	–0.6 to Vcc+0.6	V
V_{IO2}	Voltage Applied to A9 and V_{PP}	Relative to GND	–0.6 to +13.5	V
T_A	Ambient Temp., Power Applied		–65 to +150	°C
T_{ST}	Storage Temperature		–65 to +150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
T_A	Ambient Temperature	Commercial	0	70	°C
V_{CC}	Supply Voltage (Read)	Commercial	4.5	5.5	V
V_{CCP}	Suppy Voltage (Program)	Commercial	6.0	6.5	V
V_{CCV}	Supply Voltage (Verify)	Commercial	5.0	5.5	V
V_{PP}	Program Voltage	Commercial	12.5	13.0	V

D.C. Electrical Characteristics[1,2]

Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Level		2.0	Vcc+.5	V
V_{IL}	Input LOW Level		–0.3	0.8	V
V_{OH}	Output HIGH Voltage[3]	V_{CC} = Min, I_{OH} = –4.0mA	2.4		V
V_{OL}	Output LOW Voltage[3]	V_{CC} = Min, I_{OL} = 12mA		0.45	V
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	Vout = 0V to V_{CC}		10	µA
I_{CC1}	VCC Standy Current (TTL)	/CE=V_{IH}, /OE=V_{IL}		25	mA
I_{CC2}	VCC Standby Current (CMOS)	/CE=V_{CC}-0.3V to V_{CC}+0.3V		1	mA
I_{CC3}	VCC Active Current	/CE=V_{IL}, /OE=V_{IH}, f=10MHz		50	mA
I_{PP1}	VPP Current During Read	V_{PP} = 5.5V		100	µA

Capacitance

These measurements are periodically sample tested.

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V, @ f = 1MHz		8	pF
C_{OUT}	Output Capacitance			8	pF
C_{IN2}	VPP Input Capacitance			20	pF

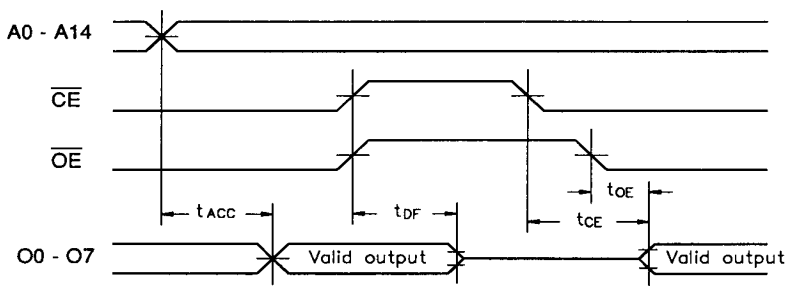
Notes:
1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. It is recommended that V_{PP} be connected directly to V_{CC} except during programming. The supply current will be I_{CC} + I_{PP1}.
3. The 27CX256 provides true CMOS output interface levels. The specifications shown are for a TTL interface.

A.C. Electrical Characteristics

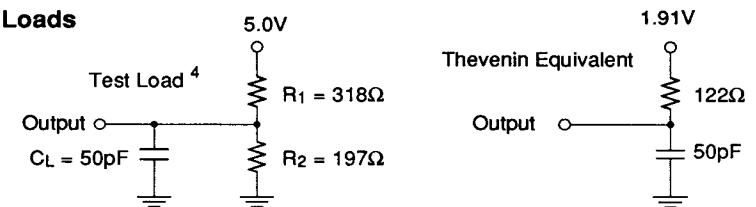
Over the Operating Range [4]

Symbol	Parameter	27CX256-35		27CX256-45		27CX256-55		Unit
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Access Time From Address To Output		35		45		55	ns
t_{CE}	Access Time From Chip Enable To Output		35		45		55	ns
t_{OE}	Access Time From Output Enable To Output[5]		20		20		25	ns
t_{DF}	Chip Disable to High-Z [5,6]		20		20		25	ns

Switching Waveforms



Test Loads



Notes:

4. Test conditions assume: signal transition times of 5 nS or less from the 10% and 90% points; timing reference levels of 1.5V (unless otherwise specified); and test loads shown.
5. t_{CE} and t_{OE} are measured from the input transition to $V_{REF} \pm 0.1V$. t_{DF} is measured from the input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$.
6. C_L includes scope and jig capacitance. t_{DF} is tested with $C_L = 5pF$.

Mode Table

Mode		$\overline{CE}/PGM$	$\overline{OE}$	VPP	VCC	A9	A0	Output
Read		VIL	VIL	VCC	VCC	X	X	DOUT
Standby		VIH	X	VCC	VCC	X	X	HI-Z
Output Disable		VIL	VIH	VCC	VCC	X	X	HI-Z
Program		VIL	VIH	VPP	VCC	X	X	DIN
Program Verify		VIH	VIL	VPP	VCC	X	X	DOUT
Program Inhibit		VIH	VIH	VPP	VCC	X	X	HI-Z
Auto Select	Manufactuer	VIL	VIL	VCC	VCC	VH	VIL	01H
	Device	VIL	VIL	VCC	VCC	VH	VIH	10H

VIL = Input Low Voltage, VIH = Input High Voltage, VH = High Voltage (12.5V), X = VIL or VIH