

SERIES 607 10-TAPS CHIP CARRIER FAST LOGIC DELAY MODULES

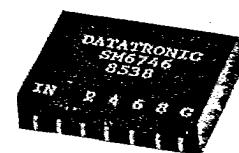
- 30 Pin Chip Carrier • Designed For Surface Mounting • Low Profile
- TTL and DTL Compatible • 10 Equally Spaced Taps

Specifications:

- Supply Voltage : 4.75 to 5.25VDC
- Logic 1 Input Current : 100 μ A Max
- Logic 0 Input Current : -1.6mA Max
- Logic 1 Volt Out : 2.5V Min
- Logic 0 Volt Out : 0.5V Max
- Logic 1 Fan-Out : 25 Max
- Logic 0 Fan-Out : 12.5 Max
- Output Rise Time⁽²⁾ : 2NSEC TYP.
- Operating Temp Range : 0°C to 70°C
- Temperature Coefficient : 100 PPM/°C

Input Test Conditions:

- Input Pulse Voltage : 3.2V
- Input Rise Time : ≤ 2 NS
- Pulse Width : 40% of Total Delay
- Supply Current ICCL* : 50mA
- ICCH* : 15mA



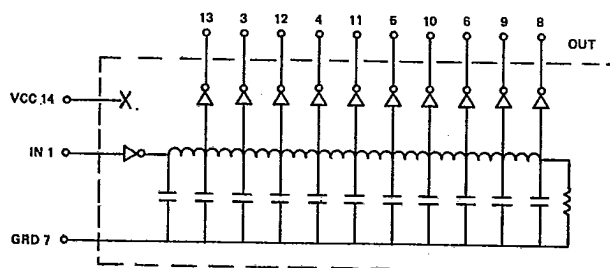
Electrical Specifications at 25°C (Measured with no Loads on Taps)

Part Number	Total Delay Nanosecond (1)	Tap to Tap Delay NSEC (1)
607-10*	9.0 $\pm$ 1.0	1.0 $\pm$ 0.4
607-20*	18.0 $\pm$ 2.0	2.0 $\pm$ 0.5
607-25*	22.5 $\pm$ 2.0	2.5 $\pm$ 0.7
607-50*	45.0 $\pm$ 2.0	5.0 $\pm$ 1.0
607-60	60.0 $\pm$ 3.0	6.0 $\pm$ 1.0
607-70	70.0 $\pm$ 3.5	7.0 $\pm$ 1.0
607-75	75.0 $\pm$ 3.5	7.5 $\pm$ 1.0
607-100	100.0 $\pm$ 5.0	10.0 $\pm$ 2.0
607-125	125.0 $\pm$ 6.0	12.5 $\pm$ 2.0
607-150	150.0 $\pm$ 7.5	15.0 $\pm$ 2.0
607-200	200.0 $\pm$ 10.0	20.0 $\pm$ 2.0
607-250	250.0 $\pm$ 12.5	25.0 $\pm$ 2.5

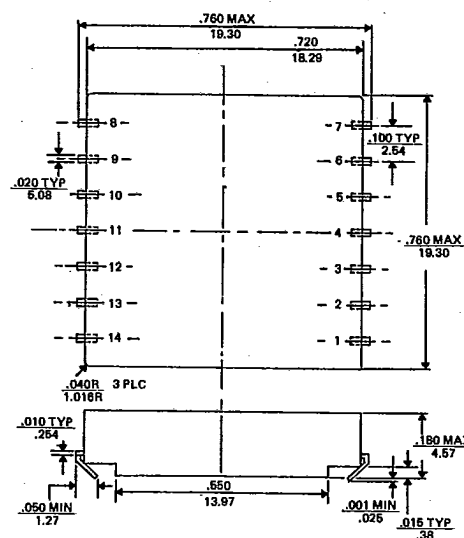
Note: (1) Measured at 1.5v level leading edge.

(2) Measured from 0.75v to 2.4v.

*Time Delay measured with respect to 1st Tap.



SCHEMATIC



INCHES .XXX $\pm$.010
MILLIMETERS .XX $\pm$.25