HB561003 Series

262,144-word x 9-bit Dynamic Random Access Memory Module

The HB561003 is a 2.25M dynamic random-access memory module organized as 262,144 x 9 bits [bit nine (PD, PQ) is generally used for parity and is controlled by $\overline{PCAS}$] in a 30-pin single in-line package comprising nine HM50256CP, 262,144 x 1-bit dynamic RAMs in 18-pin Plastic Leaded Chip Carrier mounted on a substrate together with decoupling capacitors.

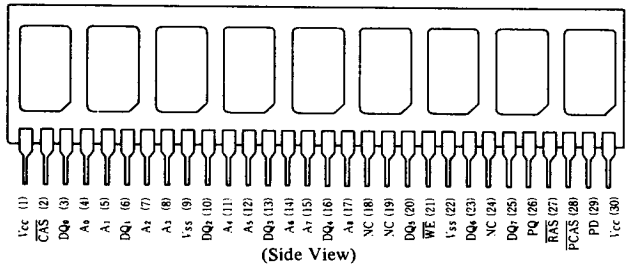
■FEATURES

- 262,144 words x 9 bits Organization
- Industry standard 30-pin Single In-line Package Memory Module
- Single 5V (±10%)
- Utilizes nine 256K Dynamic RAMs in PLCC (HM50256CP)
- HB561003 operates as nine HM50256CPs as shown in the functional block diagram.
- Low Power: Operating: 2,160mW typ. (t_{RC} = 260ns)
  Standby: 135mW typ.
- High speed:

	Access Time from $\overline{RAS}$ (max)	Access Time from $\overline{CAS}$ (max)	Read or Write Cycle (min)
HB561003AR/B-12	120ns	60ns	220ns
HB561003AR/B-15	150ns	75ns	260ns

- Page mode capability
- TTL compatible
- 256 refresh cycles/4ms
- 3 variations of refresh
  $\overline{RAS}$-only refresh
  $\overline{CAS}$-before-$\overline{RAS}$ refresh
  Hidden refresh
- Operating Ambient Air Temperature: 0°C to +70°C
- HB561003AR is leaded type
- HB561003B is leadless type (socket type)

■PIN ARRANGEMENT



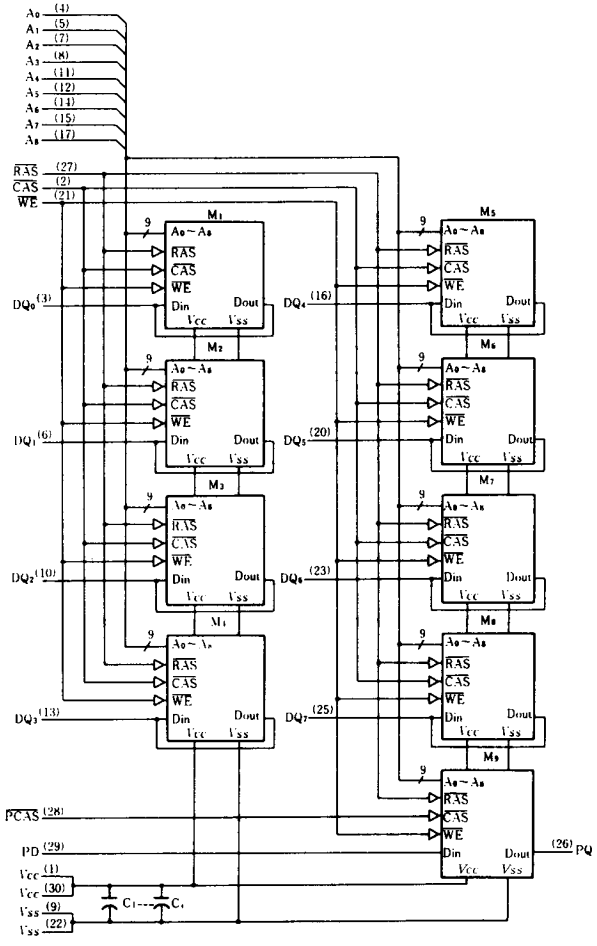
(Side View)

Notes:
1. HB561003B's pin arrangement is same as HD561003AR's.
2. Common $\overline{CAS}$ control for eight common Data-In and Data-Out lines.
3. Separate $\overline{PCAS}$ control for one separate pair of Data-In and Data-Out lines.
4. The common I/O feature dictates the use of only early write operations to prevent contention on Din and Dout.

■ PIN DESCRIPTION

A0-A8	Address Inputs
$\overline{CAS}$, $\overline{PCAS}$	Column Address Strobes
DQ0-DQ7	Data In/Data Out
PD	Data In
NC	No Connection
PQ	Data Out
$\overline{RAS}$	Row Address Strobes
$\overline{WE}$	Write Enable
V_{CC}	+5V Supply
V_{SS}	Ground

■FUNCTIONAL BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS}: −1V to +7V
Operating temperature, T_a (Ambient): 0°C to +70°C
Storage temperature (Ambient): −55°C to +125°C
Power dissipation: 9W
Short circuit output current: 50mA

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	–	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	–	0.8	V	1

Note) 1. All voltages referenced to V_{SS}

■DC ELECTRICAL CHARACTERISTICS (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Test Conditions	Symbol	min.	max.	Unit	Notes
Operating current	$\overline{RAS}$, $\overline{CAS}$ = cycle, t_{RC} = min, t_{RC} = 260ns	I_{CC1}	–	630	mA	1
	t_{RC} = 220ns			747		
Standby current	$\overline{RAS}$ = V_{IH}, D_{out} = High Z	I_{CC2}	–	40	mA	
Refresh current	$\overline{RAS}$ only refresh, t_{RC} = min, t_{RC} = 260ns	I_{CC3}	–	477	mA	
	t_{RC} = 220ns			558		
Standby current	$\overline{RAS}$ = V_{IH}, D_{out} = enable	I_{CC5}	–	90	mA	1
Refresh current	$\overline{CAS}$ before $\overline{RAS}$ refresh, t_{RC} = min, t_{RC} = 260ns	I_{CC6}	–	522	mA	
	t_{RC} = 220ns			621		
Page made supply current	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycle, t_{PC} = min, t_{PC} = 145ns	I_{CC7}	–	432	mA	
	t_{PC} = 120ns			513		
Input leakage	0 < V_{in} < 7V	I_{LI}	−10	10	μA	
Output leakage	0 < V_{out} < 7V, D_{out} = disable	I_{LO}	−10	10	μA	
Output levels	High (I_{out} = −5mA)	V_{OH}	2.4	V_{CC}	V	
	Low (I_{out} = 4.2mA)	V_{OL}	0	0.4	V	

■CAPACITANCE (V_{CC} = 5V ± 10%, Ta = 25°C)

Parameter	Symbol	typ.	max.	Unit	Notes
Address	C_{I1}	–	60	pF	2
Clocks	C_{I2}	–	75	pF	2, 3
DQ	$C_{I/O}$	–	17	pF	2, 3
PQ	C_O	–	12	pF	2, 3
PD	C_{I3}	–	10	pF	2

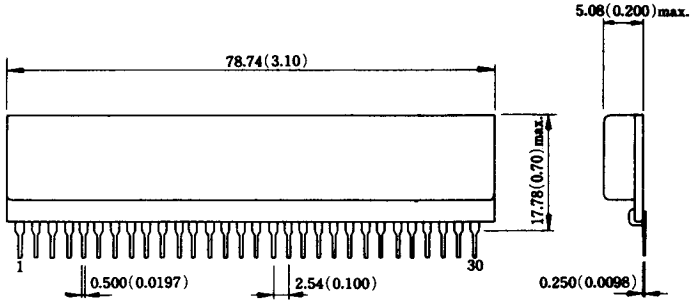
Notes: 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Capacitance measured with Boonton Meter or effective capacitance measuring method.
3. $\overline{CAS}$ = V_{IH} to disable D_{out}.

■AC CHARACTERISTICS

Refer to the HM50256CP data sheet.
The HB561003 writes data only in early write cycle ($t_{WCS} \geqq t_{WCS}$ (min)). Delayed write cycle is not available because of I/O common.

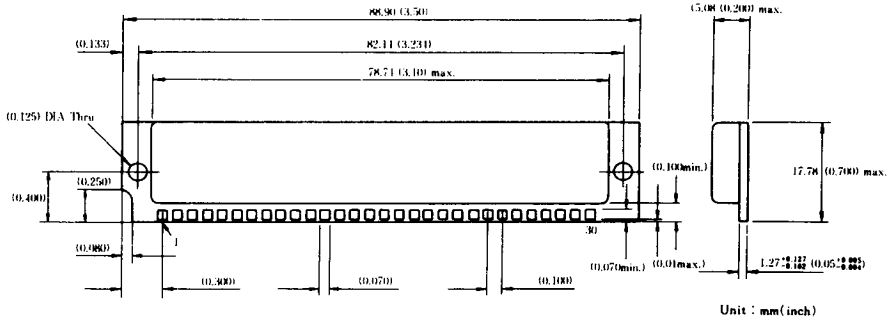
■PACKAGE OUTLINE

● HB561003AR Series



Unit : mm(inch)

● HB561003B Series



Unit : mm(inch)