SRAM MODULE

AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-98598
- MIL-STD-883

FEATURES

- Access times of 20, 25, 35, 45 ns
- Built in decoupling capacitors for low noise operation
- Organized as 32K x 32; User configurable as 64K x 16 or 128K x 8
- Operation with single 5 volt supply
- Low power CMOS
- TTL Compatible Inputs and Outputs

OPTIONS MARKINGS

- Timing

20ns	-20
25ns	-25
35ns	-35
45ns	-45

- Packaging

66 lead Pin Grid Array	P	No. 801

OPTIONS	MARKINGS
•2V Data Retention, low power standby	L

PIN ASSIGNMENT(Top View)
66 Lead PGA

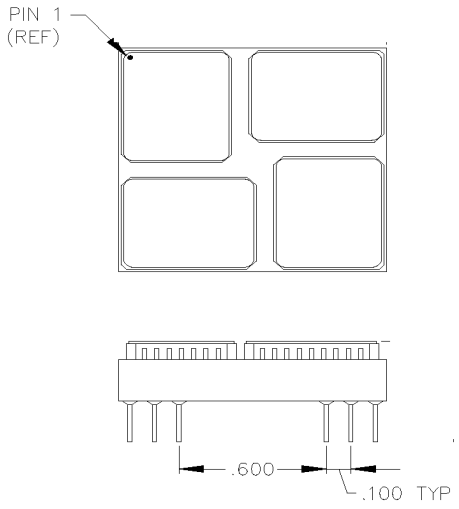
1	12	23	34	45	56
I/O8	WE2\	I/O15	I/O24	VCC	I/O31
I/O9	CE2\	I/O14	I/O25	CE4\	I/O30
I/O10	GND	I/O13	I/O26	WE4\	I/O29
A13	I/O11	I/O12	A6	I/O27	I/O28
A14	A10	OE\	A7	A3	A0
NC	A11	NC	NC	A4	A1
NC	A12	WE1\	A8	A5	A2
NC	VCC	I/O7	A9	WE3\	I/O23
I/O0	CE1\	I/O6	I/O16	CE3\	I/O22
I/O1	NC	I/O5	I/O17	GND	I/O21
I/O2	I/O3	I/O4	I/O18	I/O19	I/O20
11	22	33	44	55	66

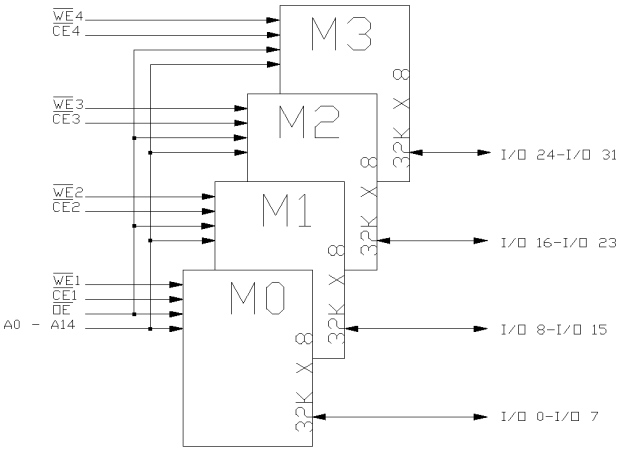
GENERAL DESCRIPTION

The Austin Semiconductor, Inc. AS7S32K32P is a 1 Megabit CMOS SRAM Module organized as 32Kx32-bits and user configurable to 64Kx16 or 128Kx8. The AS7S32K32 achieves high speed access, low power consumption and high reliability by employing advanced CMOS memory technology.

The military temperature grade product is suited for military applications.

The AS7S32K32 module is constructed using a 1.09 inch square ceramic pin grid array substrate. This compact layout reduces space requirements for board assembly to a minimum.





ABSOLUTE MAXIMUM RATINGS*

Voltage of Vcc Supply Relative to Vss.....-1V to +7V
Storage Temperature.....-55°C to +150°C
Short Circuit Output Current(per I/O).....50mA
Voltage on Any Pin Relative to Vss.....-1V to +7V
Junction Temperature**.....+175°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation on the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See the Application Information section at the end of this datasheet for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-55°C ≤ T A ≤ 125°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+.5	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-20	20	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = .8mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

			MAX					
DESCRIPTION	CONDITIONS	SYMBOL	-20	-25	-35	-45	UNITS	NOTES
Power Supply Current: Operating	CE\ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^{t}RC outputs open	I_{CC}	600	560	540	520	mA	3,13
Power Supply Current: Standby	CE\ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^{t}RC outputs open	I_{SBT1}	180	160	160	160	mA	
	CE\ ≥ V_{IH} ,All Oher Inputs ≤ V_{IL} or ≥ VIH, V_{CC} = MAX f = 0 Hz	I_{SBT2}	100	100	100	100	mA	
	CE\ ≥ V_{CC} -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V or $V_{IH} \ge V_{CC}$ -0.2V; f = 0Hz	I_{SBC1}	20	20	20	20	mA	
	"L" Version Only	I_{SBC2}	8	8	8	8	mA	

Capacitance Table

V_{IN} = 0V, f = 1MHz, TA =25°C

Symbol	Parameter	Maximum	Units	Notes
C_{ADD}	A0-A14 Capactiance	32	pF	4
C_{OE}	OE\ Capactiance	32	pF	4
C_{WE}, C_{CE}	WE\ and CE\ Capactiance	8	pF	4
C_{IO}	I/O 0 - I/O 31 Capactiance	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(-55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

DESCRIPTION		-20		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle Time	^tRC	20		25		35		45		ns	
Address access time	^tAA		20		25		35		45	ns	
Chip Enable access time	^tACE		20		25		35		45	ns	
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		ns	
Chip Disable to output in High-Z	^tHZCE		9		10		12		14	ns	6,7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	4
Chip disable to power-down time	^tPD		20		25		35		45	ns	4
Output Enable access time	^tAOE		8		10		12		14	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		9		10		12		14	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	20		25		35		45		ns	
Chip Enable to end of write	^tCW	15		17		20		22		ns	
Address valid to end of write	^tAW	15		17		20		22		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		ns	
WRITE pulse width	$^tWP1$	15		17		20		22		ns	
Data setup time	^tDS	10		12		15		40		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		10		12		15		15	ns	6,7

AC TEST CONDITIONS

Input pulse levels	Vss to 3V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

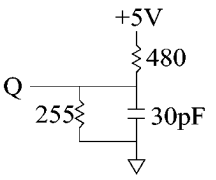


Fig. 1 OUTPUT LOAD EQUIVALENT

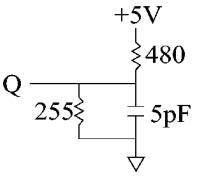


Fig. 2 OUTPUT LOAD EQUIVALENT

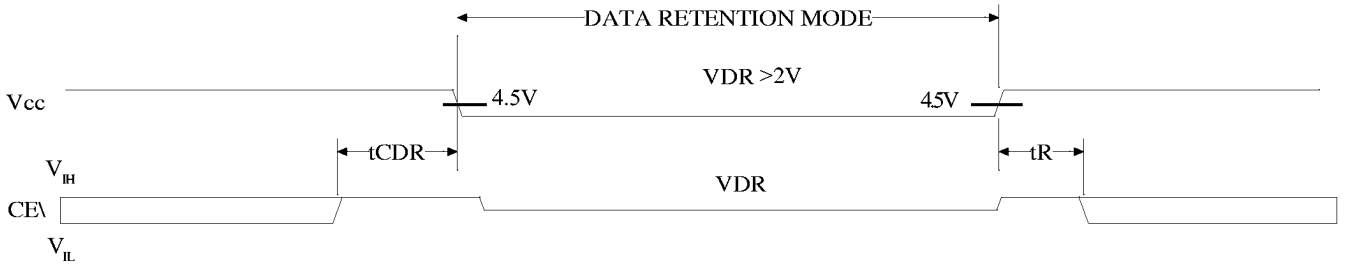
NOTES

1. All voltages referenced to VSS (GND).
2. -3v for pulse width <20ns.
3. ICC is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{t_{RC(MIN)}}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted.
6. tHZCE, tHZOE and tHZWE are specified with CL= 5pF as in Fig. 2. Transition is measured +/- 500 mV typical from steady state voltage, allowing for actual tester RC time constant.
7. At any given temperature and voltage condition, tHZCE is less than tLZCE and tHZWE is less than tLZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enables and output enable are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. tRC= READ cycle time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. ICC is for 32 bit operation.

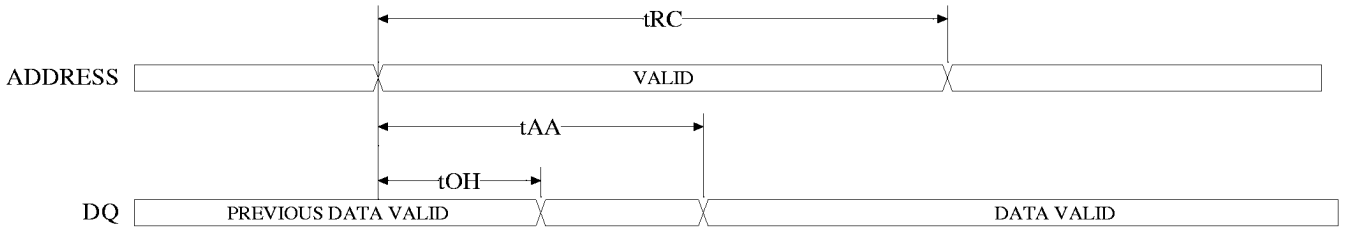
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Rerention Data			V_{DR}	2		V	
Data Retention Current	CE\ ≥ V_{CC} - 0.2 V	V_{CC} = 2.0V	I_{CCDR}		1.5	mA	
	V_{IN} ≥ V_{CC} - 0.2 V	V_{CC} = 3.0V	I_{CCDR}		2	mA	
Chip Deselect to Data Retention Time			t_{CDR}	0		ns	4
Operation Recovery Time			t_R	t_{RC}		ns	4,11

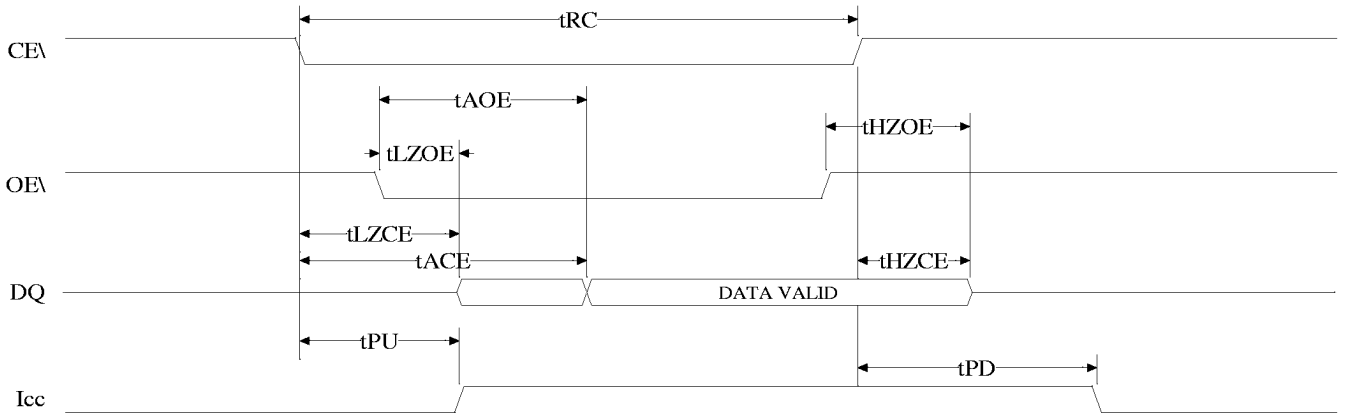
LOW V_{CC} DATA RETENTION WAVEFORM



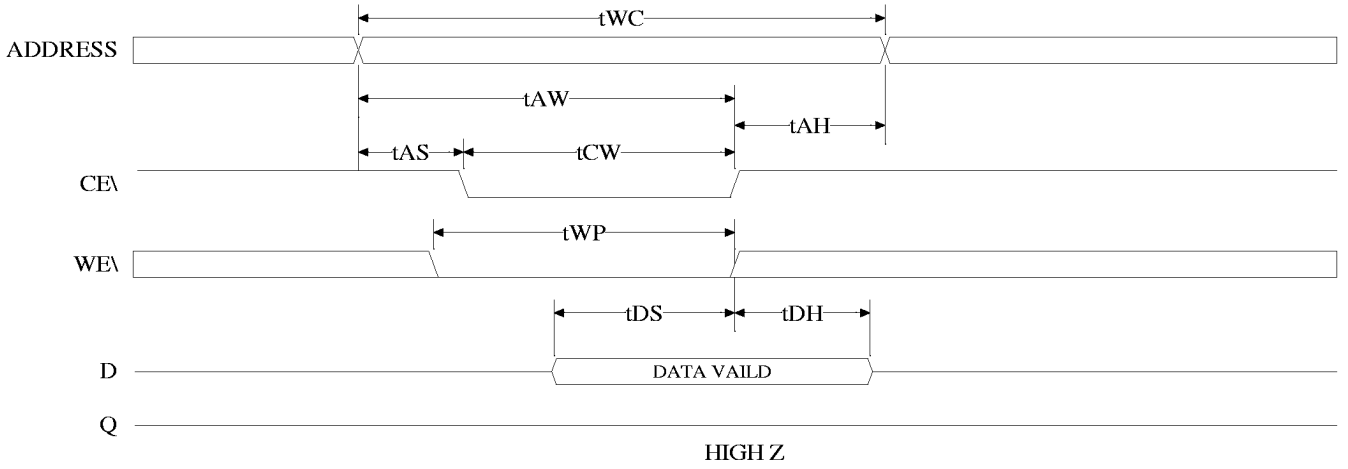
READ CYCLE NO. 1[8,9]



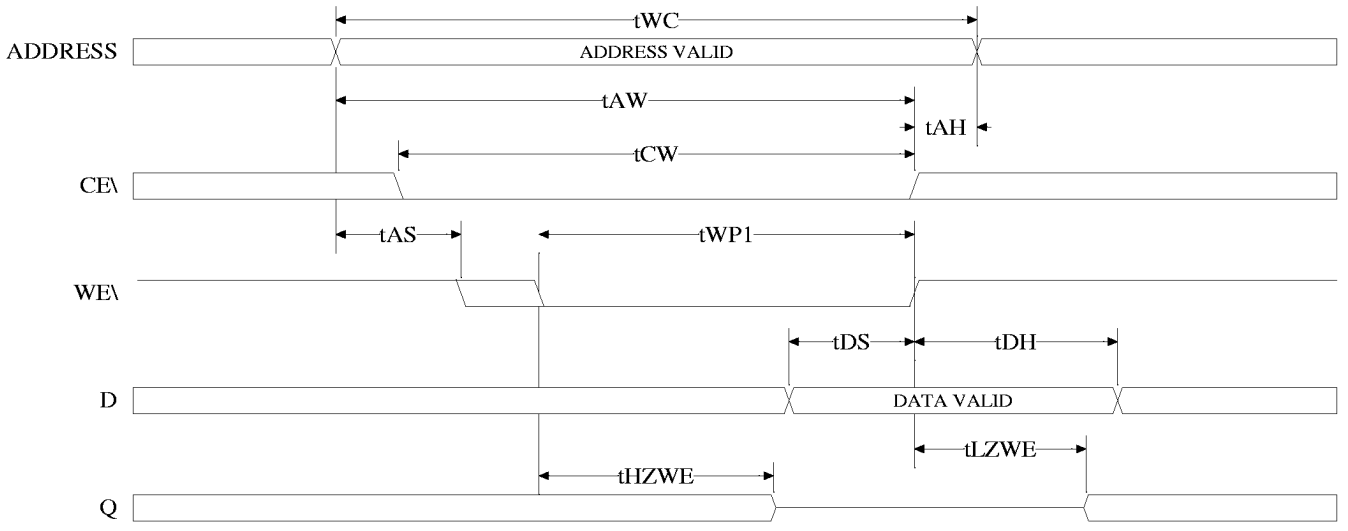
READ CYCLE NO. 2[7,8,10]



WRITE CYCLE NO. 1
(Chip Enable Controlled)



WRITE CYCLE NO. 2[7]
(Write Enable Controlled)



MECHANICAL DEFINITION
for the AS7S32K32 Pin Grid Array