



New Product

SiE802DF

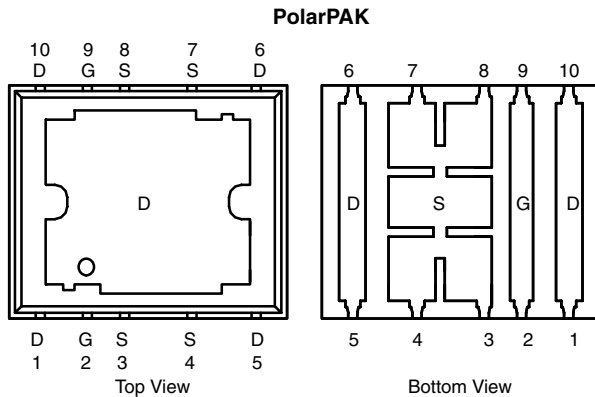
Vishay Siliconix

www.DataSheet4U.com

N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	r _{DS(on)} (Ω) ^e	I _D (A) ^a		Q _g (Typ)
		Silicon Limit	Package Limit	
30	0.0019 @ V _{GS} = 10 V	202	60	50 nC
	0.0026 @ V _{GS} = 4.5 V	173	60	

[Package Drawing](#)



Top surface is connected to pins 1, 5, 6, and 10

Ordering Information: SiE802DF-T1—E3 (Lead (Pb)-Free)

FEATURES

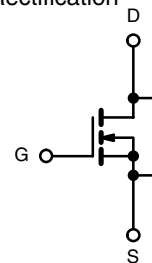
- TrenchFET® Gen II Power MOSFET
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK® Package for Double-Sided Cooling
- Leadframe-Based New Encapsulated Package
 - Die Not Exposed
 - Same Layout Regardless of Die Size
- Low Q_{gd}/Q_{gs} Ratio Helps Prevent Shoot-Through
- 100% R_g and UIS Tested



RoHS COMPLIANT

APPLICATIONS

- VRM
- DC/DC Conversion: Low-Side
- Synchronous Rectification



N-Channel MOSFET

[For Related Documents](#)

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	30	V
Gate-Source Voltage		V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	202 (Silicon Limit)	A
	T _C = 70 °C		60 ^a (Package Limit)	
	T _A = 25 °C		60 ^a	
	T _A = 70 °C		42.7 ^{b, c}	
Pulsed Drain Current		I _{DM}	100	A
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	60 ^a	
	T _A = 25 °C		4.3 ^{b, c}	
Single Pulse Avalanche Current		I _{AS}	50	mJ
Avalanche Energy		E _{AS}	125	
Maximum Power Dissipation	T _C = 25 °C	P _D	125	W
	T _C = 70 °C		80	
	T _A = 25 °C		5.2 ^{b, c}	
	T _A = 70 °C		3.3 ^{b, c}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	–50 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}			260	

Notes:

- Package limit is 60 A.
- Surface Mounted on 1" x 1" FR4 Board.
- t = 10 sec
- See Solder Profile (<http://www.vishay.com/doc?73257>). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	$t \leq 10$ sec	R_{thJA}	20	24	°C/W
Maximum Junction-to-Case (Drain Top)	Steady State	R_{thJC} (Drain)	0.8	1	
Maximum Junction-to-Case (Source) ^{a, c}		R_{thJC} (Source)	2.2	2.7	

Notes:

- a. Surface mounted on 1" x 1" FR4 board.
b. Maximum under steady state conditions is 68 °C/W.
c. Measured at source pin (on the side of the package)

SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\ \mu\text{A}$		32.2		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-6.4		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.5	2.2	2.7	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	25			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 23.6\text{ A}$		0.0016	0.0019	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 21.3\text{ A}$		0.0021	0.0026	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 23.6\text{ A}$		156		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		7000		pF
Output Capacitance	C_{oss}			1200		
Reverse Transfer Capacitance	C_{rss}			500		
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 23.6\text{ A}$		105	160	nC
		$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 23.6\text{ A}$		50	75	
Gate-Source Charge	Q_{gs}			21		
Gate-Drain Charge	Q_{gd}			14		
Gate Resistance	R_g	$f = 1\text{ MHz}$		1.1	1.65	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\ \Omega$		45	70	ns
Rise Time	t_r			195	300	
Turn-Off Delay Time	$t_{d(off)}$			45	70	
Fall Time	t_f			20	30	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$		25	40	
Rise Time	t_r			20	30	
Turn-Off Delay Time	$t_{d(off)}$			65	100	
Fall Time	t_f			10	15	



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SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			60	A
Pulse Diode Forward Current ^a	I_{SM}				100	
Body Diode Voltage	V_{SD}	$I_S = 10\text{ A}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$		55	85	ns
Body Diode Reverse Recovery Charge	Q_{rr}			66	105	nC
Reverse Recovery Fall Time	t_a				25	ns
Reverse Recovery Rise Time	t_b				30	

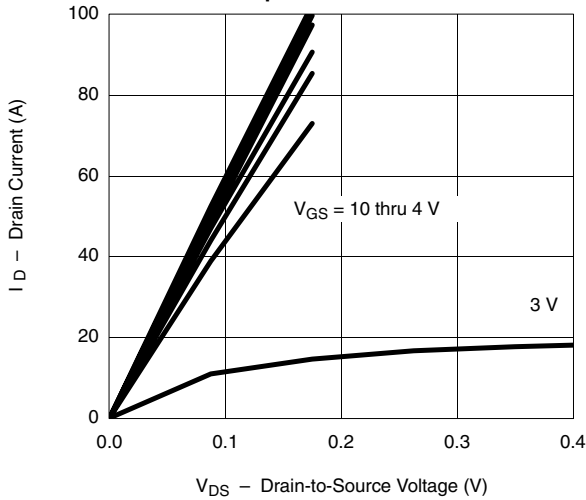
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

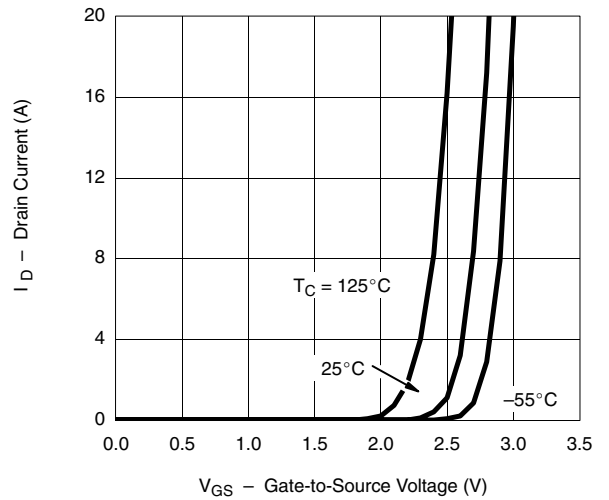
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

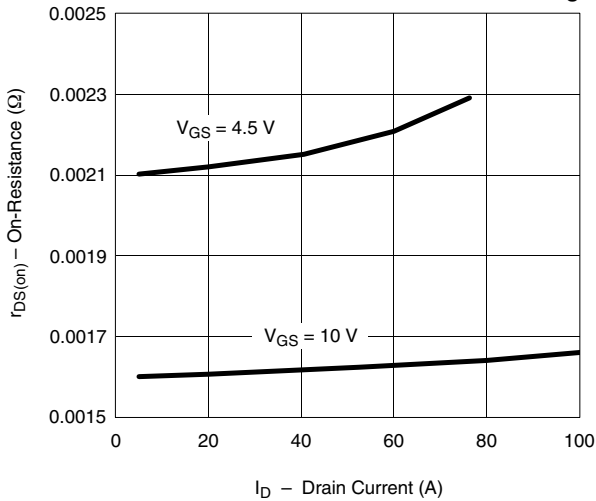
Output Characteristics



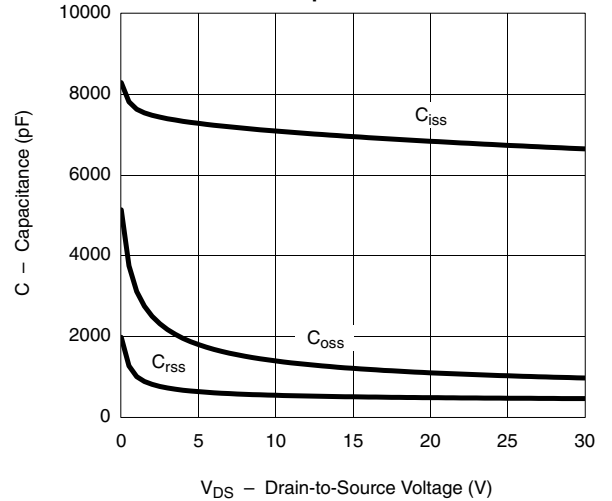
Transfer Characteristics



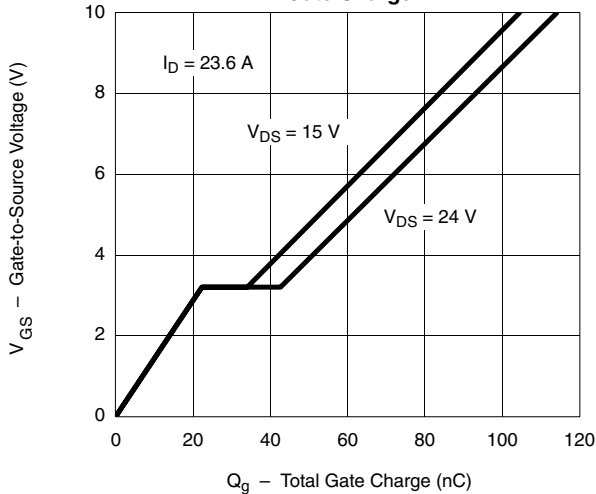
On-Resistance vs. Drain Current and Gate Voltage



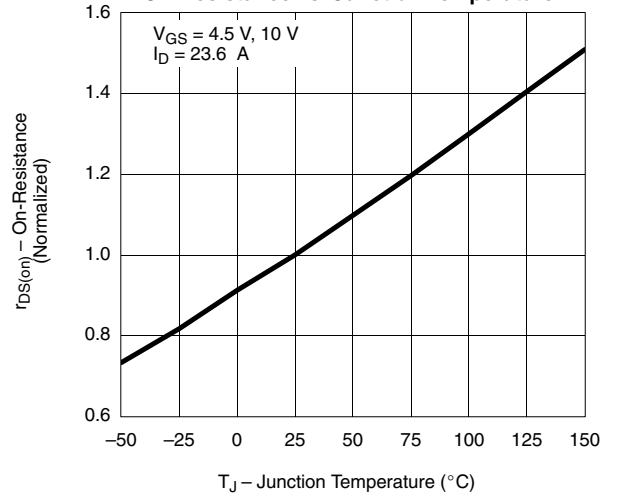
Capacitance



Gate Charge

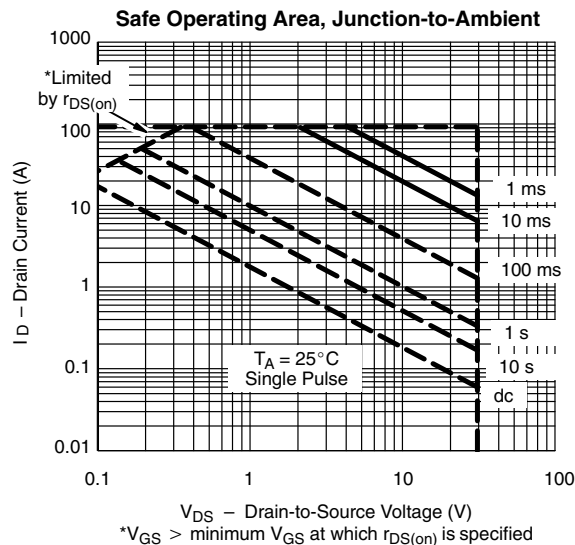
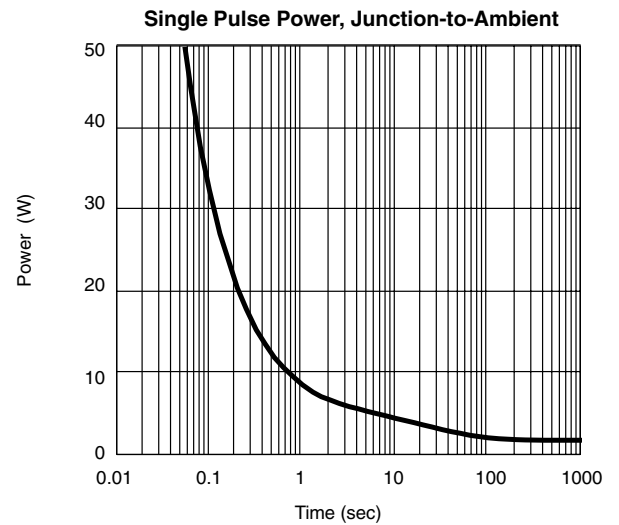
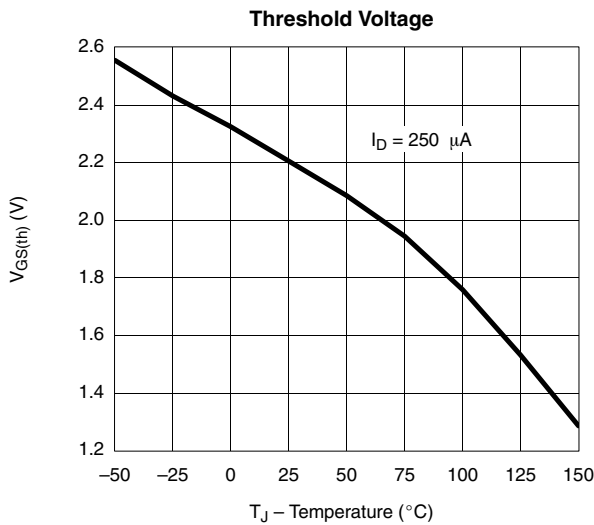
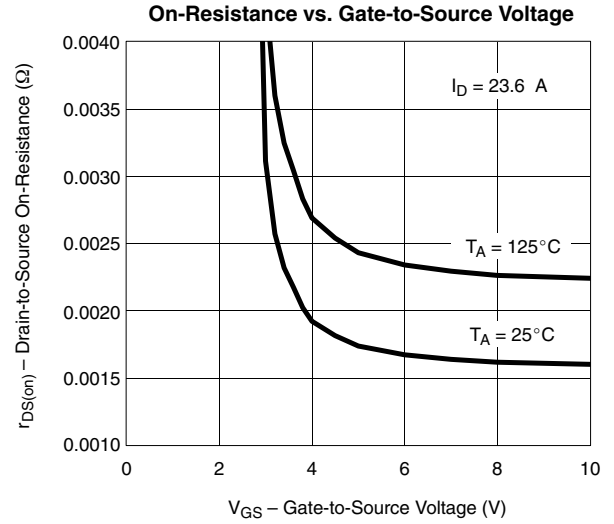
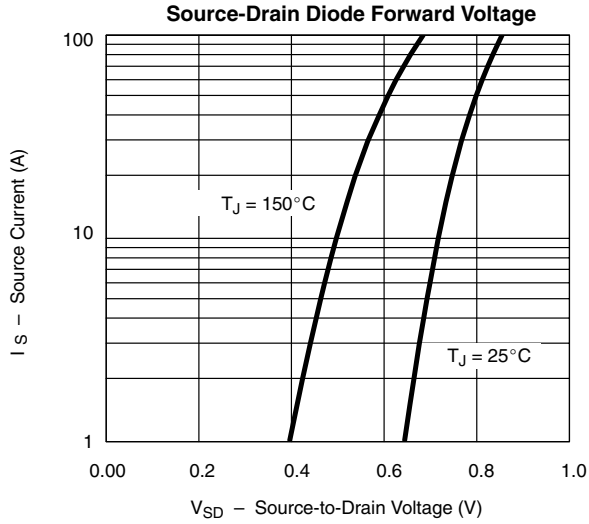


On-Resistance vs. Junction Temperature

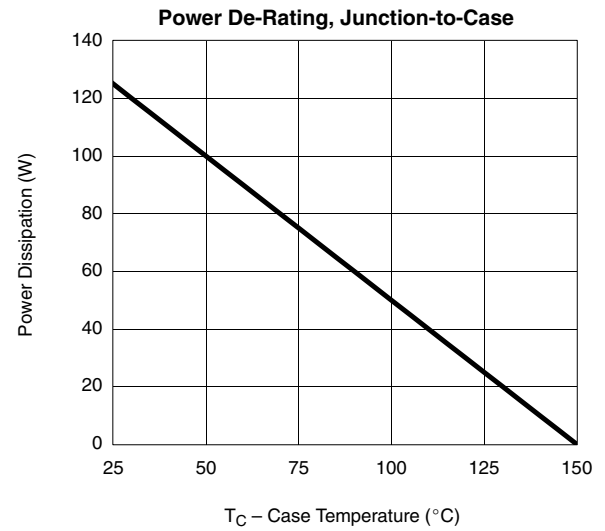
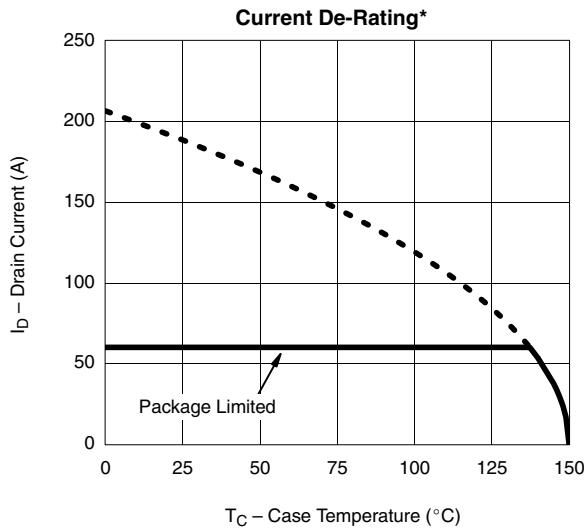




TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



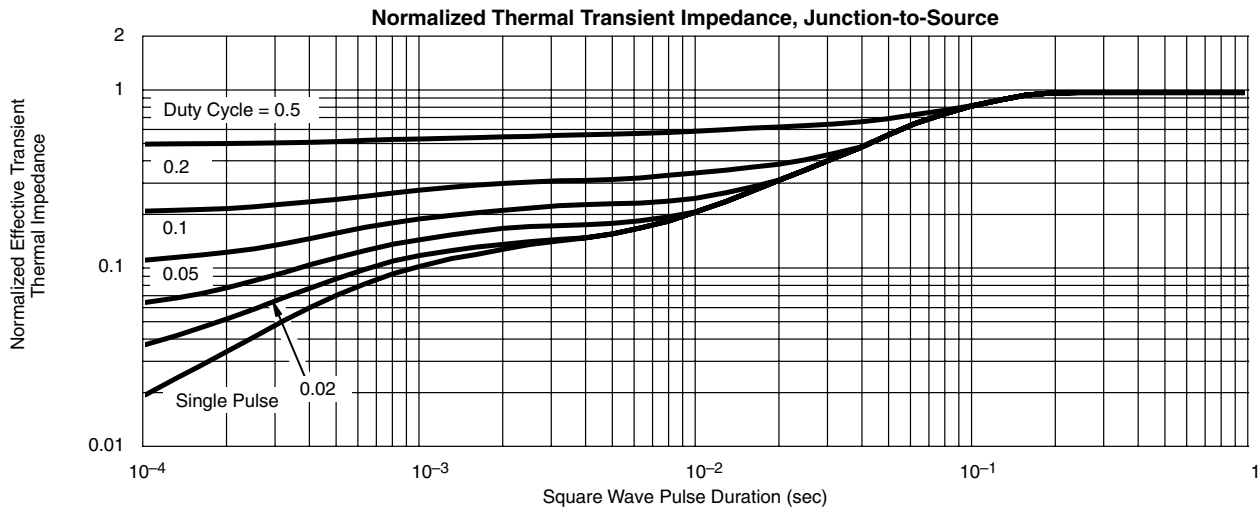
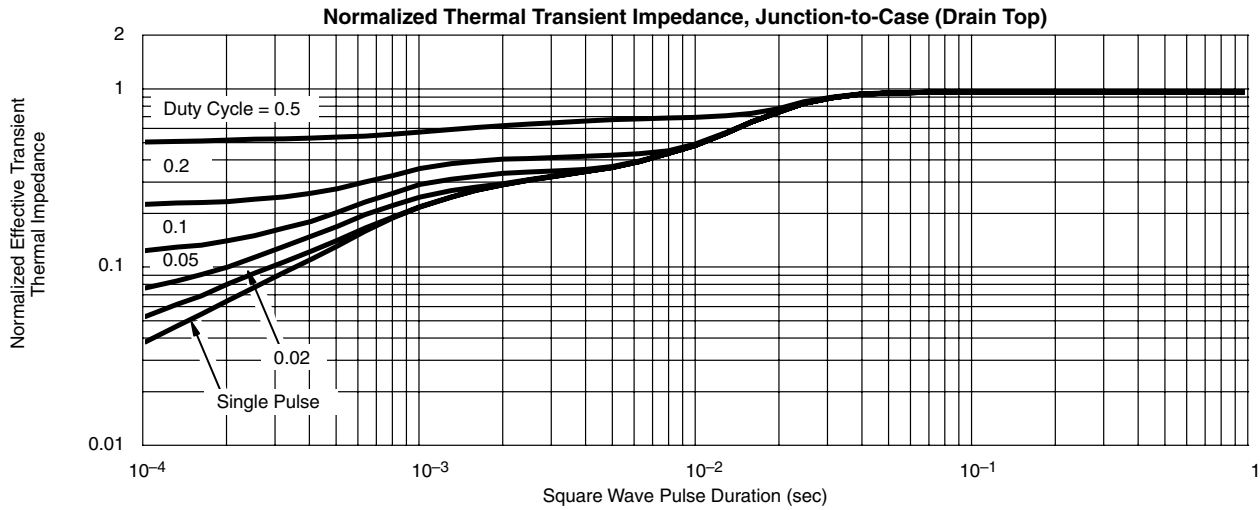
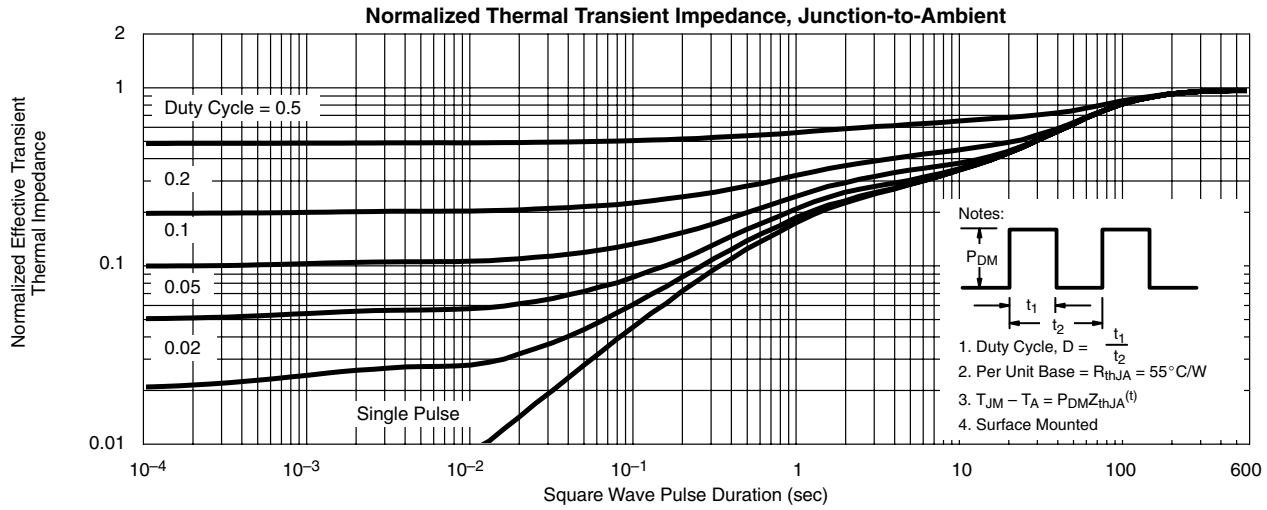
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



*The power dissipation P_D is based on T_{J(max)} = 150°C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?72985>.



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