

## CMOS 4-BIT MICROCONTROLLER

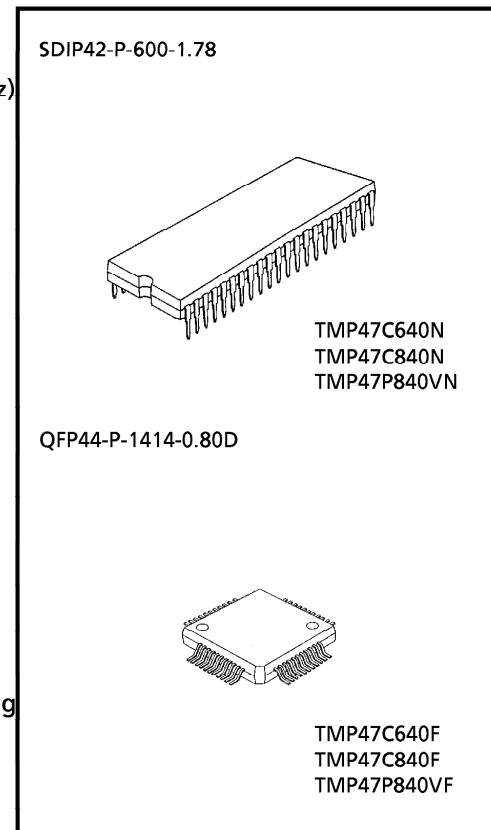
**TMP47C640N, TMP47C840N  
TMP47C640F, TMP47C840F**

The 47C640/840 are high speed and high performance 4-bit single chip microcomputers based on the TLC5470 series with a 8-bit A/D converter.

PART No.	ROM	RAM	PACKAGE	OTP
TMP47C640N	6144 × 8-bit	384 × 4-bit	SDIP42-P-600-1.78	TMP47P840VN
TMP47C640F			QFP44-P-1414-0.80D	TMP47P840VF
TMP47C840N	8192 × 8-bit	512 × 4-bit	SDIP42-P-600-1.78	TMP47P840VN
TMP47C840F			QFP44-P-1414-0.80D	TMP47P840VF

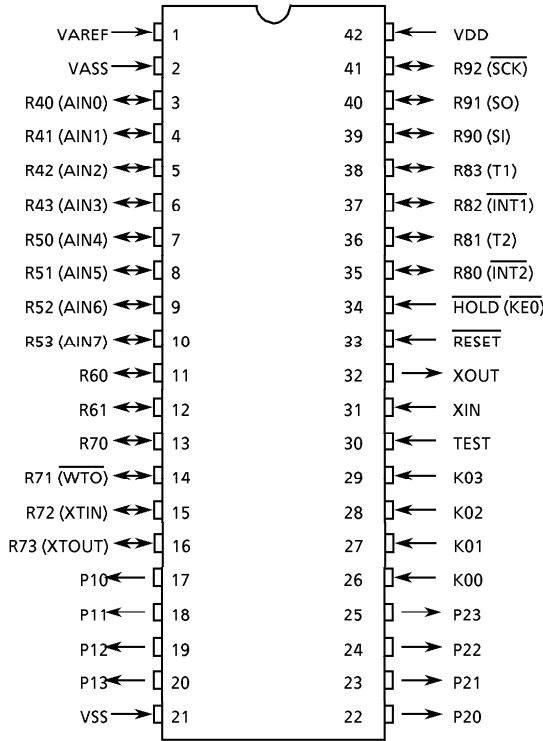
**FEATURES**

- ◆ 4-bit single chip microcomputer
- ◆ Instruction execution time: 1.3  $\mu$ s (at 6 MHz), 244  $\mu$ s (at 32.8 kHz)
- ◆ 92 basic instructions
  - Table look-up instructions
  - 5-bit to 8-bit data conversion instruction
- ◆ Subroutine nesting: 15 levels max.
- ◆ 6 interrupt sources (External: 2, Internal: 4)
  - All sources have independent latches each, and multiple interrupt control is available.
- ◆ I/O port (34 pins)
  - Input 2 ports 5 pins
  - Output 2 ports 8 pins
  - I/O 6 ports 21 pins
- ◆ Interval Timer
- ◆ Two 12-bit Timer/Counters 2 channel
  - Timer, event counter, and pulse width measurement mode
- ◆ Watchdog Timer
- ◆ Serial Interface with 8-bit buffer
  - Simultaneous transmission and reception capability
  - 8/4-bit transfer, external/internal clock, and leading/trailing edge shift mode
- ◆ 8-bit successive approximate type A/D converter
  - With sample and hold
  - 8 analog inputs
  - Conversion time : 32  $\mu$ s (at 6 MHz)
- ◆ Remote control signal pre-processing capability
- ◆ High current outputs
  - LED direct drive capability (typ. 20mA × 8 bits)
- ◆ Dual-clock operation
  - High-speed/Low-power-consumption operating mode
- ◆ Hold function
  - Battery/Capacitor back-up
- ◆ Real Time Emulator : BM47C860A + BM1174

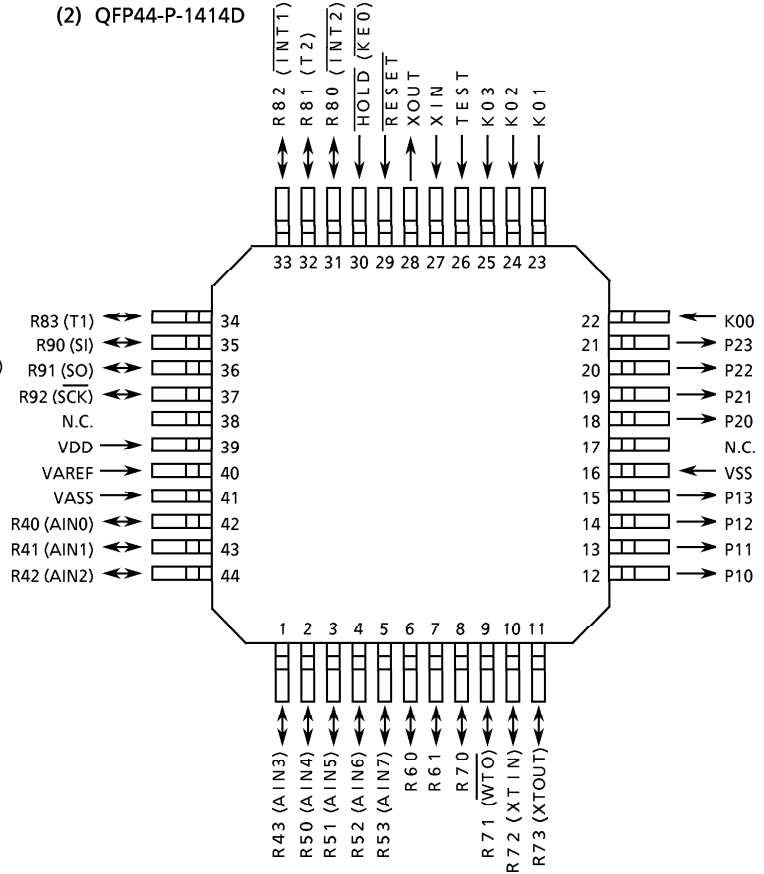


**PIN ASSIGNMENTS (TOP VIEW)**

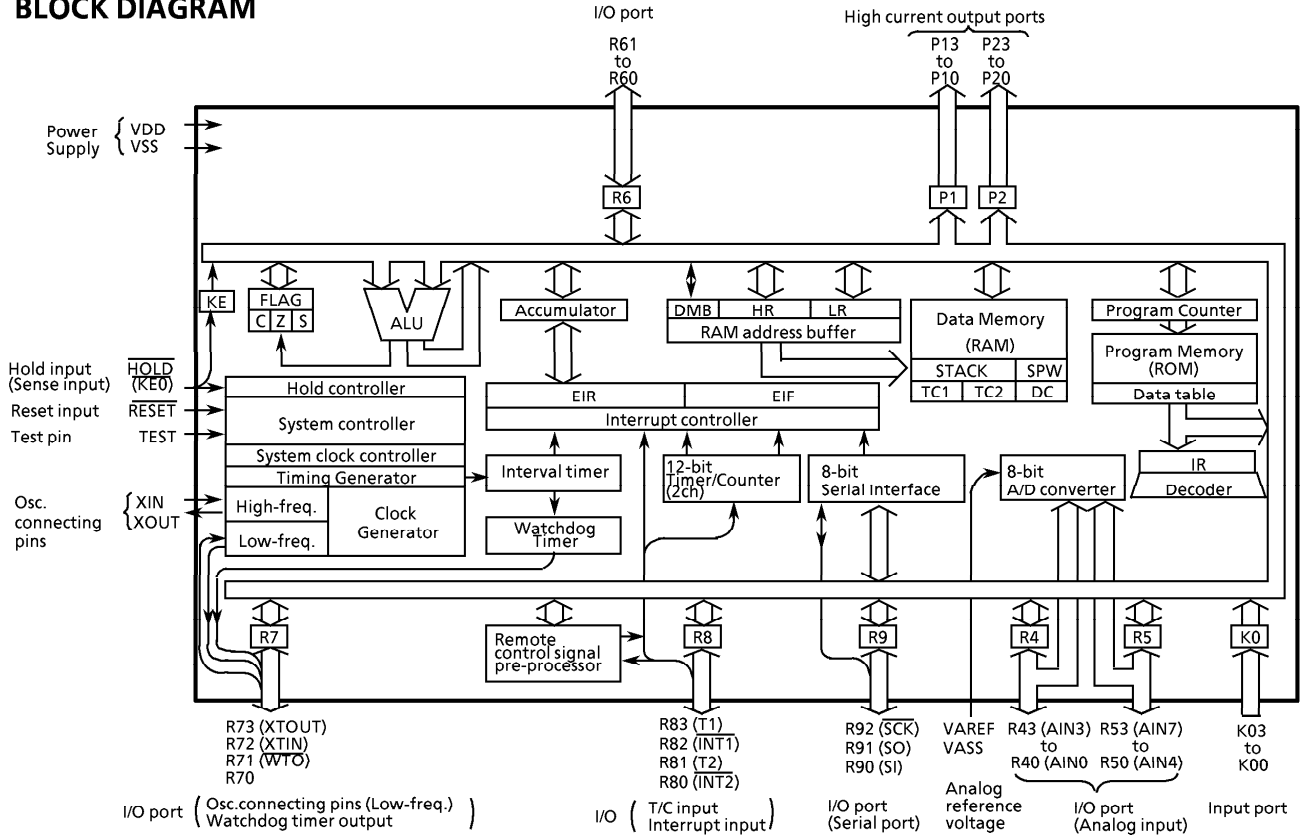
(1) SDIP42-P-600



(2) QFP44-P-1414D



**BLOCK DIAGRAM**



## PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 to K00	Input	4-bit input port	
P13 to P10	Output	4-bit output port with latch.	
P23 to P20		8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @HL].	
R53 (AIN7) to R40 (AIN0)	I/O (Input)	4-bit I/O port with latch. When used as input port, watchdog timer output or analog input, the latch must be set to "1".	A/D converter analog input
R61 to R60	I/O		
R73 (XTOUT)	I/O (Output)	Set to Dual-clock operating mode, when R73,R72 pin use as clock generator.	Resonator connecting pin (Low-freq.). For inputting external clock, XTIN is used and XTOUT is opened.
R72 (XTIN)	I/O (Input)		
R71 ( $\overline{WTO}$ )	I/O (Output)	Can be set, cleared, and tested for each bit as specified by L register indirect addressing bit manipulation instructions.	Watchdog timer output
R70	I/O		
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ( $\overline{INT1}$ )			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ( $\overline{INT2}$ )			External interrupt 2 or REMO-COM input
R92 ( $\overline{SCK}$ )	I/O(I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
XIN	Input	Resonator connecting pin (High-frequency) .	
XOUT	Output	For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ( $\overline{KE0}$ )	Input (Input)	HOLD request/release signal input	Sence input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 5V	
VSS		0V (GND)	
VAREF		A/D converter analog reference voltage (High)	
VASS		A/D converter analog reference voltage (Low)	

## OPERATIONAL DESCRIPTION

Concerning the 47C640/840 the configuration and functions of hardware are described. As the description has been provided with priority on those parts differing from the 47C660/860, the technical data sheets for the 47C660/860 shall also be referred to.

### 1. SYSTEM CONFIGURATION

#### ◆ INTERNAL CPU FUNCTION

Except for the system control circuit, the CPU core functions are the same as those of the 47C660/860.

#### ◆ PERIPHERAL HARDWARE FUNCTION

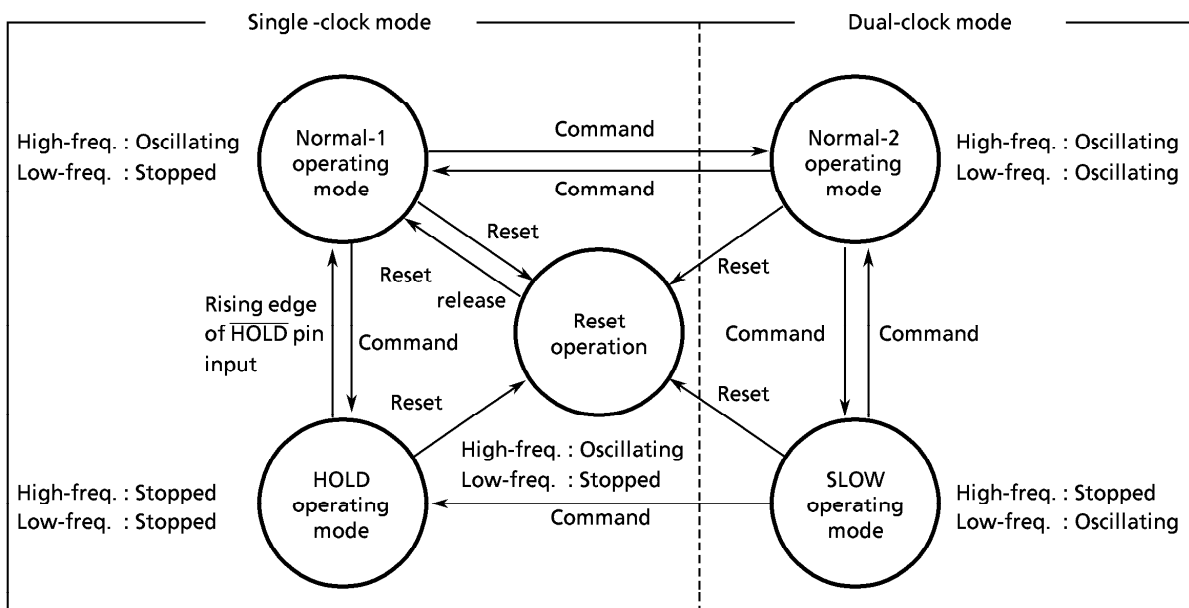
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|-----------------------------|---------------------------------|
| ① I/O Ports                 | ⑤ Remote control pulse detector |
| ② Interval Timer            | ⑥ A/D converter                 |
| ③ Timer/Counters (TC1, TC2) | ⑦ Serial Interface              |
| ④ Watchdog Timer            |                                 |

The description has been provided with priority on the function (①) changed from the 47C660/860, and the system clock control circuit.

### 2. INTERNAL CPU FUNCTION

#### 2.1 SYSTEM CONTROL CIRCUIT

The system clock controller starts or stops the high-frequency and low-frequency clock oscillator and switches between the basic clocks. The operating mode is generally divided into the single-clock mode and the dual-clock mode, which are controlled by command.



*Note.* Normal-1 and Normal-2 operating modes are sometimes referred to as the Normal operating mode collectively.

Figure 2-1. Operating Mode Transition Diagram

## (1) System clock control

System clock control is performed by the command register (OP16). During reset, this register is initialized to "0" and the single-clock mode is selected. Each state at operating mode switching can be read from the status register (IPOE).

System clock control command register  
(Port address : OP16) (Initial value : 0000)

3	2	1	0
DCLK3	SLCK	DCLK1	DWUT
DCLK3 / DCLK1		Selects operation mode (Note 2)	
00 : Single clock mode (Normal-1 operation mode)			
01 : Reserved			
10 : Dual clock mode (Normal-2 operation mode)			
11 : Dual clock mode (SLOW operation mode)			
SLCK		Selects input clock to the eighth stage of TG (Note 3)	
Example : $f_c = 4.19 \text{ MHz}$			
0 : $f_c / 2^7$ [Hz] ..... 32.8 [kHz]			
1 : $f_s$			
DWUT		Sets the warm-up time (Note 4)	
Example : $f_c = 4.19 \text{ MHz}$ $f_s = 32.8 \text{ kHz}$			
0 : $2^8 / f_s + 2^9 / f_c$ [s] ..... 7.9 [ms]			
1 : $2^{11} / f_s + 2^9 / f_c$ ..... 62.6			

System clock control status register  
(Port address : IPOE)

3	2	1	0
(SIOF)	(SEF)	SMF	HOLD/SLS
SMF		Low-frequency clock oscillating state	
Status of binary counter (output of the seventeenth stage of TG)			
HOLD / SLS		HOLD pin state/operation state monitor	
Single clock mode    Dual clock mode 0 : $\overline{\text{HOLD}}$ pin at "H" level    In normal operation 1 : $\overline{\text{HOLD}}$ pin at "L" level    In SLOW operation			
Note1. $f_c$ ; High-frequency clock [Hz] $f_s$ ; High-frequency clock [Hz]			
Note2. Note that the configuration of bits.			
Note3. Only Normal-2 operation mode			
Note4. Only switching from SLOW to Normal-2			
Note5. The access to command register (OP16) may cause the outputs over the eighth stage of timing generator to precede that to be expected by maximum $2^7/f_c$ or $1/f_s$ [s].			

Figure 2-2. System Clock Control Command Register

## (2) Instruction Cycle

The instruction execution and on-chip peripheral hardware operations are performed in synchronization with the basic clock. The smallest unit of instruction execution is called the "instruction cycle". The TLCS-470 series instruction set has 3 kinds of instructions, 1-cycle instruction to 3-cycle instruction. Each instruction cycle consists of 4 states (S1 through S4). Each state consists of 2 basic clock pulses.

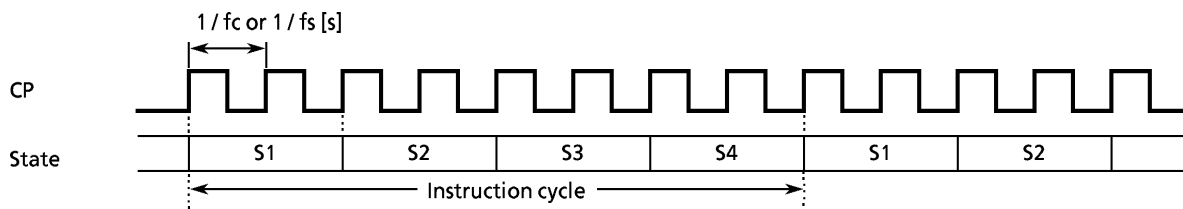


Figure 2-4. Instruction Cycle

## 2.1.2 Operation Mode

## (1) Dual-clock mode

In this mode, the Normal-2 operation is generally performed by generating the instruction cycle from the high-frequency clock ( $f_c$ ). As required, the instruction cycle is generated by the low-frequency clock ( $f_s$ ), and the lower consumption power operation is performed by transferring SLOW operation to HOLD operation. The following describes the switching between the Normal-2, SLOW and HOLD operations in the dual clock mode. At reset, the command register is initialized to the single-clock mode. Since the low-frequency clock is not oscillated, Normal-2 operation.

a. Switching from Normal-2 operation to SLOW operation

Setting DCLK1 (bit 1 of OP16) to "1" switches Normal-2 operation to SLOW operation. However it takes a few seconds to get a stable oscillation of the low-frequency clock. Therefore if there is possible to switch from Normal-2 operation to SLOW operation, wait until the low-frequency clock is stable or check the oscillation state by a program. SMF status (bit 1 of 1P0E) is available to check it.

When the high-frequency clock ( $f_c/27$ ) is input to the 8th stage of TG, first sets SLCK (bit 2 of OP16) to "2" and input the low-frequency clock ( $f_s$ ). Then, SMF is monitored by a program. After confirming that SMF is changed "2" to "0" to "1" or "0" to "0", set DCLK1 to "1". At this time, the high-frequency clock oscillator stops.

b. Returning from SLOW operation to Normal-2 operation

Bit 1 of the command register is cleared to "0" and, at the same time, the warm-up time for return is set to DWUT. When the warm-up time has passed, the Normal-2 operation takes place. By monitoring SLS (bit 0 of the status register), the current operating mode can be known.

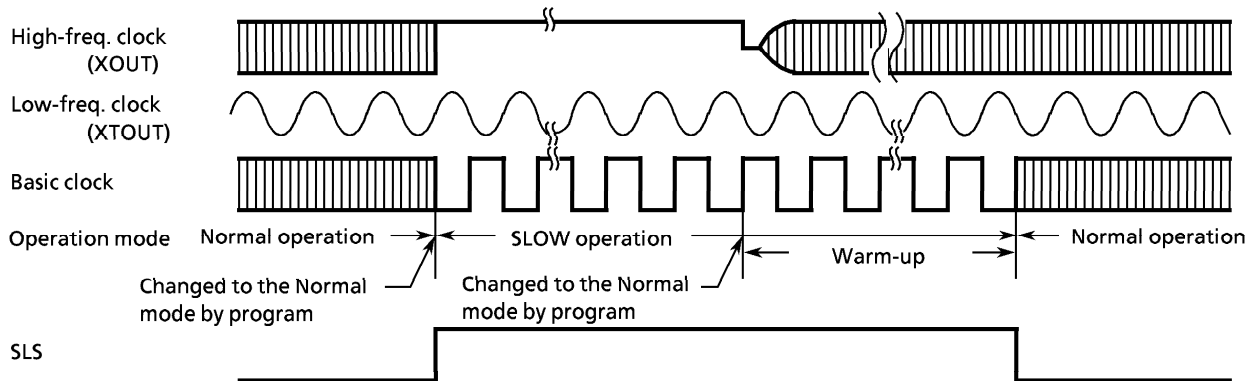


Figure 2-4. System Clock Switching Timing

c. Shifting from the SLOW operation to the HOLD operation

By setting the command in the command register (OP10), the low-frequency clock oscillation stops and the HOLD operation starts.

After being released the HOLD operation, the operation mode is NORMAL-1.

*Note.* In the HOLD and SLOW operating modes, the power consumed by the oscillator and the internal hardware is reduced. However, the power for the pin interface (depending on the external circuitry and program) is not directly associated with the low-power consumption operation. This must be considered in system design as well as interface circuit design.

(2) Single-clock mode

In this mode, only the high-frequency clock oscillator is used. Pins R72 (XTIN) and R73 (XTOUT) become the ordinary I/O port. The HOLD operating mode is available for reducing power consumption. It is controlled by the command register (OP10). In this mode, therefore, the system clock control command register (OP16) need not be manipulated.

### 3.PERIPHERAL HARDWARE FUNCTION

#### 3.1 I/O Ports

The 47C660A/860A have 10 I/O ports (34pins) each as follows:

- ① K0 ; 4-bit input
- ② P1, P2 ; 4-bit output
- ③ R4, R5 ; 4-bit input/output (shared with A/D converter analog inputs)
- ④ R6 ; 4-bit input/output
- ⑤ R7 ; 4-bit input/output (shared with the low-frequency resonator connecting pins and the watchdog timer output)
- ⑥ R8 ; 4-bit input/output (shared with external interrupt request input and timer/counter input)
- ⑦ R9 ; 3-bit input/output (shared with serial port)
- ⑧ KE ; 1-bit sense input (shared with hold request/release signal input)

This section describes a port of ④ which is changed from the 47C660/860.

Table 3-1 lists the port address assignments and the I/O instruction that can access the ports.

##### Port R6 (R61 - R60)

Port R6 is a 2-bit I/O port with latch . When used as an input, the latch must be set to "1". The latch is initialized to "1" during reset.

R63 - R62 pins do not exist actually, execution of the set or clear instruction for R63 - R62 ([SET %OP06, 3 (or 2)] or [CLR %OP06, 3 (or 2)]) affects the operation of the internal CPU. Therefore, these instructions should not be execution on R63 - R62. However, other instructions may be used, in which an uncertain value is read upon execution of an input instruction.

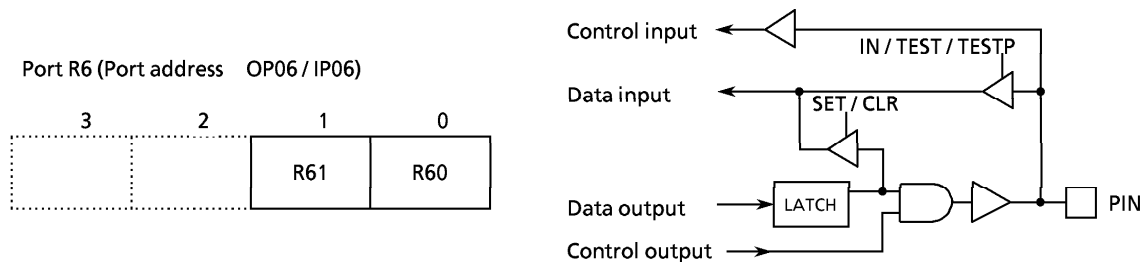


Figure 3-1. Port R6

Port address (**)	Port		Input/Output instruction								
	Input (Ip**)	Output (Op**)	IN %p, A	IN %p, @HL	OUT A, %p	OUT @HL, %p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00H	K0 input port	—	○	○	—	—	—	—	—	○	—
01	P1 output latch	P1 output port	○	○	○	○	○	○	○	○	—
02	P2 output latch	P2 output port	○	○	○	○	○	○	○	○	—
03	—	—	—	—	—	—	—	—	—	—	—
04	R4 input port (Analog input)	R4 output port	○	○	○	○	○	○	○	○	○
05	R5 input port (Analog input)	R5 output port	○	○	○	○	○	○	○	○	○
06	R6 input port	R6 output port	○	○	○	○	○	○	○	○	○
07	R7 input port	R7 output port	○	○	○	○	○	○	○	○	○
08	R8 input port	R8 output port	○	○	○	○	○	○	○	○	○
09	R9 input port	R9 output port	○	○	○	○	○	○	○	○	○
0A	—	—	—	—	—	—	—	—	—	—	—
0B	—	—	—	—	—	—	—	—	—	—	—
0C	—	—	—	—	—	—	—	—	—	—	—
0D	REMO-CON count value	REMO-CON offset value	○	○	○	○	○	○	○	○	—
0E	Status input (Note 3)	REMO-CON control	○	○	○	○	○	○	○	○	—
0F	Serial receive buffer	Serial transmit buffer	○	○	○	○	○	○	○	○	—
10H	—	Hold operating mode control	—	—	—	—	—	—	—	—	—
11	—	—	—	—	—	—	—	—	—	—	—
12	A / D converted value	A / D analog input selector	○	○	○	○	○	○	○	○	—
13	A / D status input	A / D start register	○	○	○	○	○	○	○	○	—
14	—	—	—	—	—	—	—	—	—	—	—
15	—	Watchdog timer control	—	—	—	—	—	—	—	—	—
16	—	System clock control	—	—	—	—	—	—	—	—	—
17	—	—	—	—	—	—	—	—	—	—	—
18	—	Interval Timer interrupt control	—	—	○	○	○	○	○	○	—
19	—	—	—	—	—	—	—	—	—	—	—
1A	—	—	—	—	—	—	—	—	—	—	—
1B	—	—	—	—	—	—	—	—	—	—	—
1C	—	Timer/Counter 1 control	—	—	○	○	○	○	○	○	—
1D	—	Timer/Counter 2 control	—	—	○	○	○	○	○	○	—
1E	—	Serial interface control 1	—	—	○	○	○	○	○	○	—
1F	—	Serial interface control 2	—	—	○	○	○	○	○	○	—

Note 1 : "—" means the reserved state. Unavailable for the user programs.

Note 2 : The 5-bit to 8-bit data conversion instruction [OUTB @HL], automatic access to ports P1 and P2.

Note 3 : The status input of serial interface, clock generator, and HOLD (KE0) pin.

Table 3-1. Port Address Assignments and Available I/O Instructions



## INPUT/OUTPUT CIRCUITRY

## (1) Control pins

The input/output circuitries of the 47C640/840 control pins are similar to those of the 47C660/860.

## (2) I/O ports

The input/output circuitries of the 47C640/840 I/O ports are shown below, any one of the circuitries can be chosen by a code (IA-IC) as a mask option.

PORT	I/O	INPUT/OUTPUT CIRCUITRY and CODE			REMARKS
		IA	IB	IC	
K0	Input				Pull-up/pull-down resistor  $R_{IN} = 70k\Omega$ (typ.) $R = 1k\Omega$ (typ.)
P1 P2	Output				Sink open drain output Initial "Hi-Z" High current $I_{OL} = 20mA$ (typ.)
R4 R5 R6 R7	I/O				Sink open drain output Initial "Hi-Z" $R = 1k\Omega$ (typ.) Analog inputs (R4, R5) $R_A = 5k\Omega$ (typ.) $C_A = 12pF$ (typ.)
R8 R9	I/O				Sink open drain output Initial "Hi-Z"  Hysteresis input $R = 1k\Omega$ (typ.)

## ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V<sub>SS</sub> = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V <sub>DD</sub>		- 0.3 to 6.5	V
Input Voltage	V <sub>IN</sub>		- 0.3 to V <sub>DD</sub> + 0.3	V
Output Voltage	V <sub>OUT</sub>		- 0.3 to V <sub>DD</sub> + 0.3	V
Output Current (per 1 pin)	I <sub>OUT1</sub>	Ports R	3.2	mA
	I <sub>OUT2</sub>	Ports P1, P2	30	
Output Current (total)	Σ I <sub>OUT1</sub>	Ports P1, P2	120	mA
Power Dissipation [T <sub>opr</sub> = 70°C]	PD		600	mW
Soldering Temperature (time)	T <sub>slid</sub>		260 (10 s)	°C
Storage Temperature	T <sub>stg</sub>		- 55 to 125	°C
Operating Temperature	T <sub>opr</sub>		- 40 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V<sub>SS</sub> = 0V, T<sub>opr</sub> = - 40 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V <sub>DD</sub>		f <sub>c</sub> = 6 MHz	4.5	5.5	V
			f <sub>c</sub> = 4.2 MHz	2.7		
			In the SLOW mode	2.7		
			In the HOLD mode	2.0		
Input High Voltage	V <sub>IH1</sub>	Except Hysteresis Input	V <sub>DD</sub> ≧ 4.5 V	V <sub>DD</sub> × 0.7	V <sub>DD</sub>	V
	V <sub>IH2</sub>	Hysteresis Input		V <sub>DD</sub> × 0.75		
	V <sub>IH3</sub>			V <sub>DD</sub> < 4.5 V		
Input Low Voltage	V <sub>IL1</sub>	Except Hysteresis Input	V <sub>DD</sub> ≧ 4.5 V	0	V <sub>DD</sub> × 0.3	V
	V <sub>IL2</sub>	Hysteresis Input			V <sub>DD</sub> × 0.25	
	V <sub>IL3</sub>				V <sub>DD</sub> < 4.5 V	
Clock Frequency	f <sub>c</sub>	XIN, XOUT		0.4	6.0	MHz
	f <sub>s</sub>	XTIN, XTOUT		30	34	kHz

Note 1. Input voltage V<sub>IH3</sub>, V<sub>IL3</sub> : in the SLOW or HOLD mode

## D.C. CHARACTERISTICS

 $(V_{SS} = 0V, T_{opr} = -40 \text{ to } 70^{\circ}\text{C})$ 

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	$V_{HS}$	Hysteresis Input		–	0.7	–	V
Input Current	$I_{IN1}$	Port KO, TEST, RESET, HOLD	$V_{DD} = 5.5V,$	–	–	$\pm 2$	$\mu\text{A}$
	$I_{IN2}$	Ports R (open drain)	$V_{IN} = 5.5V / 0V$				
Low Input Current	$I_{IL}$	Ports R (push-pull)	$V_{DD} = 5.5V, V_{IN} = 0.4V$	–	–	–2	mA
Input Resistance	$R_{IN1}$	Port KO with pull-up/pull-down		30	70	150	k $\Omega$
	$R_{IN2}$	RESET		100	220	450	
Output Leakage Current	$I_{LO}$	Ports (open drain)	$V_{DD} = 5.5V, V_{OUT} = 5.5V$	–	–	2	$\mu\text{A}$
Output Low Voltage	$V_{OL}$	Except XOUT, ports P	$V_{DD} = 4.5V, I_{OL} = 1.6\text{mA}$	–	–	0.4	V
Output Low Current	$I_{OL}$	Ports P1, P2	$V_{DD} = 4.5V, V_{OL} = 1.0V$	–	20	–	mA
Supply Current (in the Normal mode)	$I_{DD}$		$V_{DD} = 5.5V$ $f_c = 4\text{MHz}$	–	3	6	mA
Supply Current (in the SLOW mode)	$I_{DDS}$		$V_{DD} = 3.0V$ $f_s = 32.768\text{kHz}$	–	30	60	$\mu\text{A}$
Supply Current (in the HOLD mode)	$I_{DDH}$		$V_{DD} = 5.5V$	–	0.5	10	$\mu\text{A}$

Note 1. Typ. values show those at  $T_{opr} = 25^{\circ}\text{C}, V_{DD} = 5V$ .

Note 2. Input Current  $I_{IN1}$ ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. Supply Current  $I_{DD}, I_{DDH}$ ;  $V_{IN} = 5.3V/0.2V$

The KO port is open when the input resistor is contained. The voltage applied to the R port is within the valid range.

Supply Current  $I_{DDS}$ ;  $V_{IN} = 2.8V/0.2V$

Low frequency clock is only oscillated (connecting XTIN, XTOUT).

## A / D CONVERSION CHARACTERISTICS

 $(T_{opr} = -40 \text{ to } 70^{\circ}\text{C})$ 

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Reference Voltage	$V_{AREF}$		$V_{DD} - 1.5$	–	$V_{DD}$	V
	$V_{ASS}$		$V_{SS}$	–	1.5	
Analog Reference Voltage Range	$\Delta V_{AREF}$	$V_{AREF} - V_{ASS}$	2.5	–	–	V
Analog Input Voltage	$V_{AIN}$		$V_{ASS}$	–	$V_{AREF}$	V
Analog Supply Current	$I_{REF}$		–	0.5	1.0	mA
Nonlinearity Error		$V_{DD} = 4.5 \text{ to } 5.5V, V_{SS} = 0.0V$ $V_{AREF} = V_{DD} \pm 0.001V$ $V_{ASS} = 0.000V$	–	–	$\pm 1$	LSB
Zero Point Error			–	–	$\pm 1$	
Full Scale Error			–	–	$\pm 1$	
Total Error			–	–	$\pm 2$	

## A. C. CHARACTERISTICS

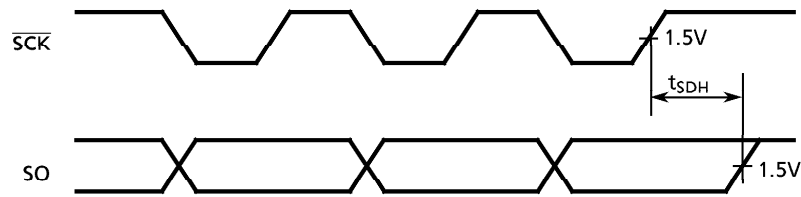
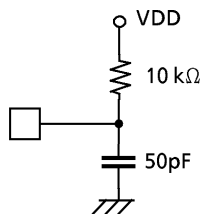
 $(V_{SS} = 0V, V_{DD} = 4.5 \text{ to } 6.0V, T_{opr} = -40 \text{ to } 70^{\circ}C)$ 

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	$t_{cy}$	In the Normal mode	1.3	—	20	$\mu s$
		In the SLOW mode	235	—	267	
High level Clock pulse Width	$t_{WCH}$	External clock mode	80	—	—	ns
Low level Clock pulse Width	$t_{WCL}$					
A / D Sampling Time	$t_{AIN}$	$f_c = 4MHz$	—	4	—	$\mu s$
Shift Data Hold Time	$t_{SDH}$		$0.5t_{cy} - 300$	—	—	ns

## Note. Shift Data Hold Time

External circuit for  $\overline{SCK}$  pin and SO pin

Serial port (completion of transmission)

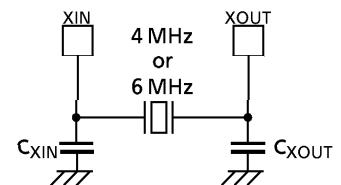


## RECOMMENDED OSCILLATING CONDITIONS

 $(V_{SS} = 0V, V_{DD} = 4.5 \text{ to } 6.0V, T_{opr} = -40 \text{ to } 70^{\circ}C)$ 

## (1) 6 MHz

Ceramic Resonator

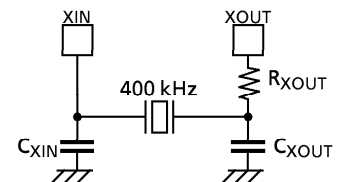
CSA6.00MGU (MURATA)  $C_{XIN} = C_{XOUT} = 30pF$ KBR-6.00MS (KYOCERA)  $C_{XIN} = C_{XOUT} = 30pF$ 

## (2) 4 MHz

Ceramic Resonator

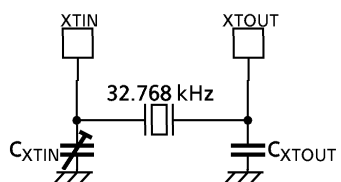
CSA4.00MG (MURATA)  $C_{XIN} = C_{XOUT} = 30pF$ KBR-4.00MS (KYOCERA)  $C_{XIN} = C_{XOUT} = 30pF$ 

Crystal Oscillator

204B-6F 4.0000 (TOYOCOM)  $C_{XIN} = C_{XOUT} = 20pF$ 

## (3) 400 kHz

Ceramic Resonator

CSB400B (MURATA)  $C_{XIN} = C_{XOUT} = 220pF, R_{XOUT} = 6.8 k\Omega$ KBR-400B (KYOCERA)  $C_{XIN} = C_{XOUT} = 100pF, R_{XOUT} = 10 k\Omega$ (4) 32.768 kHz ( $V_{SS} = 0V, V_{DD} = 2.7 \text{ to } 6.0V, T_{opr} = -40 \text{ to } 70^{\circ}C$ )Crystal Oscillator  $C_{XTIN}, C_{XTOUT}; 10 \text{ to } 33pF$ 

Note: In order to get the accurate oscillation frequency, the adjustment of capacitors must be required.

**TYPICAL CHARACTERISTICS**

