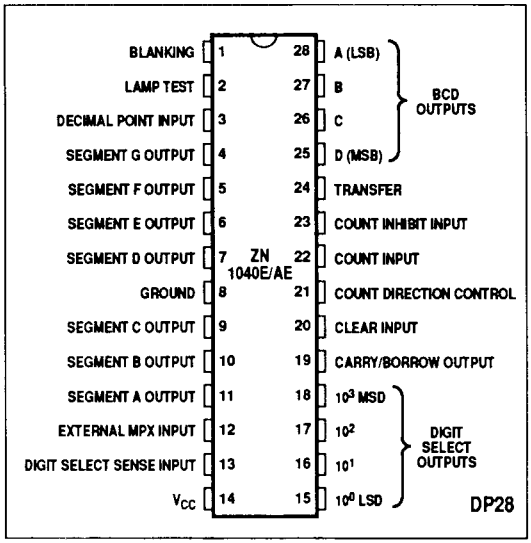
ZN1040E/AE
UNIVERSAL COUNT/DISPLAY CIRCUIT

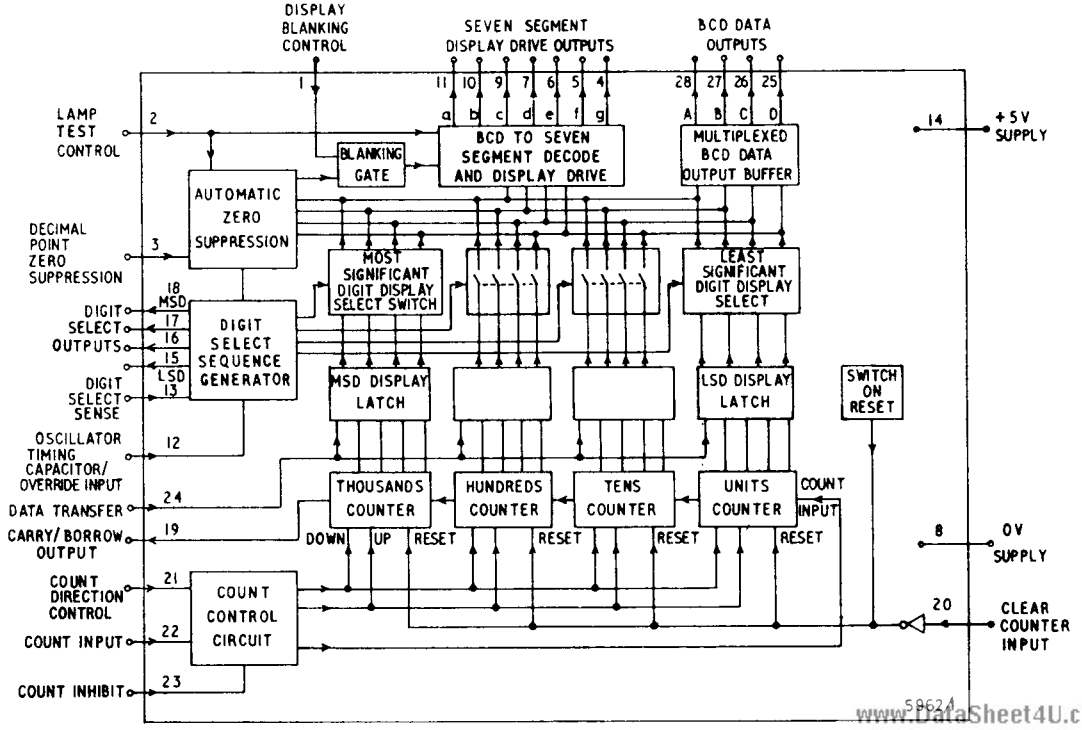
The ZN1040 is designed to satisfy the need for a universal count/display circuit suitable for the widest possible range of applications. This bipolar device allows fast count rates and high output currents to drive seven - segment LED displays, whilst BCD outputs allow interfacing to decoders for other types of display.

FEATURES

- 4 Decade synchronous up/down counter with Memory
- Carry/borrow output for direct synchronous Cascading
- BCD and seven-segment outputs
- Segment outputs can drive LED displays directly
- Schmitt trigger on count input for slow input Waveform
- Count inhibit gating
- Two versions: ZN1040E; high-speed; ZN1040AE, Low-cost
- Fully TTL compatible



Pin connections - top view



Function Diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage, Vcc	+5.5 V
Segment output currents	100 mA (ZN1040E) 80 mA (ZN1040AE)
Other output currents	25 mA
Operating temperature range	- 20°C to + 70°C(ZN1040E) 0°C to + 70°C (ZN1040A
Storage temperature range	- 55°C to + 125°C

ELECTRICAL CHARACTERISTICS: V_{CC} = 5V T_{AMb} = 25°C (unless otherwise specified)

Characteristics	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Count input positive going Threshold	V_T+	—	1.5	—	V	
Count input negative going Threshold	V_T-	—	1	—	V	
High level input voltage(1)	V_{IH}	2.0	—	—	V	
Low level input voltage(1)	V_{IL}	—	—	0.8	V	
High level input current	I_{IH}	—	—	20	µA	
Low level input current	I_{IL}	—	—	- 600	µA	
High level output voltage(2)	V_{OH}	2.4	3.3	—	V	I_{LOAD} = - 0.4mA
Low level output voltage(2)	V_{OL}	—	0. 25	0.5	V	I_{LOAD} = 16mA
Segment low level output Voltage (ZN1040E)		—	0.3	0.6	V	I_{LOAD} = 50mA
Segment low level output Voltage (ZN1040AE)		—	0.3	0.6	V	I_{LOAD} = 40mA
Maximum count rate (ZN1040E)		5	8	—	MHz	
Maximum count rate (ZN1040AE)		3	—	—	MHz	
Transfer pulse width		50	—	—	ns	
Clear pulse width		100	—	—	ns	
Supply voltage	V_{CC}	4.75	—	5.25	V	
Supply current(3)	I_S	—	90	—	mA	

NOTES (1) All inputs except count input
(2) All outputs except segment outputs
(3) All inputs and outputs open circuit

OPERATING NOTES

SECTION 1 : COUNTER

1.1 Counter Operation

The counter section of the ZN1040 is a synchronous four decade BCD counter. Each decade consists of four flip-flops which are clocked simultaneously on the positive going edge of the count input pulse. Suitable steering logic ensures that the 16 flip-flops count in a four decade BCD sequence. The BCD outputs of the counter are connected to data latches in which the count may be stored for subsequent decoding and display.

The counter and count control circuitry are shown in figure 1 whilst the count input and inhibit input circuits are shown in more detail in figure 2.

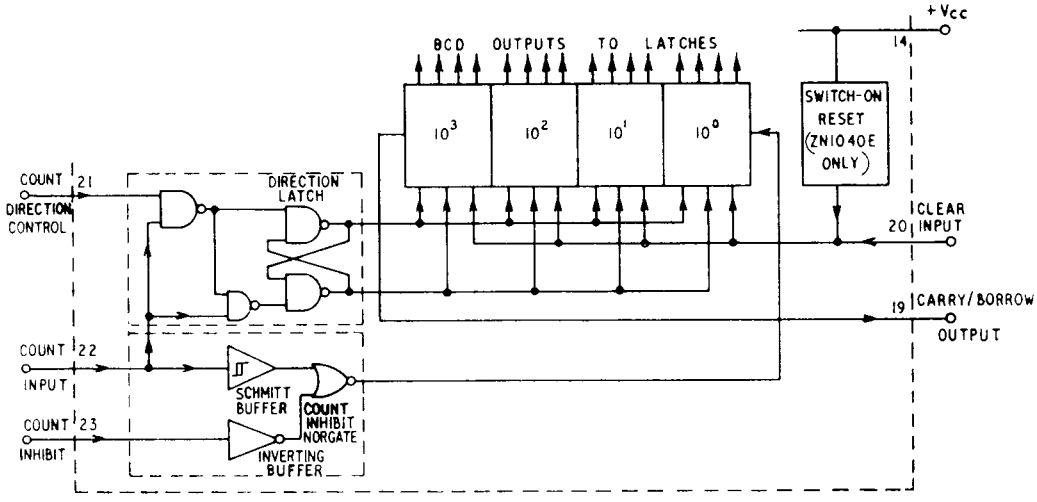


Fig. 1. Count System Functional Diagram

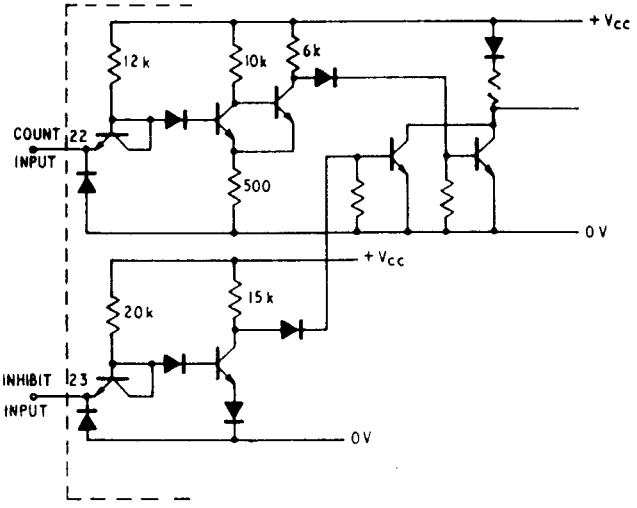


Fig. 2. Count Input and Inhibit Circuit

Counting occurs on the positive going edge of the count input pulse.

The counter input consists of a Schmitt trigger which allows the counter to operate reliably from input waveforms with very slow edges. It also allows a very simple anti-bounce circuit to be used when the count input is taken from a mechanical contact as shown in figure 3.

Bounce occurs mainly on contact closure. R_2 is made very much smaller than R_1 so that when the contact closes C_1 discharges rapidly to below the lower threshold of the Schmitt trigger. However, if the contact subsequently opens due to bounce, the time constant $(R_1 + R_2)\,C_1$ is of sufficient length so that C_1 does not charge to the upper threshold of the Schmitt trigger. When the contact genuinely opens then C_1 will charge and the counter will be clocked. The values of R_1, R_2 and C_1 will depend on the contact characteristics and the maximum count rate.

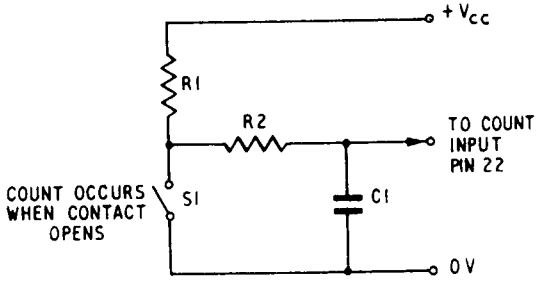


Fig. 3. Anti-Bounce Circuit

1.2 Inhibit Input

The inhibit input is used to gate the count input pulses. When the inhibit input is high then the second input of the inhibit NOR gate is low and count pulses are allowed through. However, when the inhibit input is taken low, the second input of the inhibit NOR gate is taken high. This holds the output low so that the count pulses are blocked. Correct timing of the inhibit control is important. If the inhibit control is taken low when the count input is low then an extra positive going edge will be fed through the inhibit NOR gate and an extra count will result as shown in figure 4a. The inhibit input should thus be operated when the count input is already high as shown in figure 4b. If the count input waveform has a duty cycle which is not 50% then it is advisable to arrange that it is normally high, as in figure 4b, since this makes operation of the inhibit control simpler.

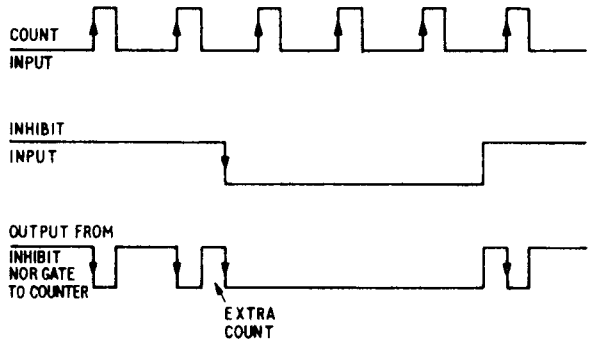


Fig. 4a. Incorrect Inhibit Operation

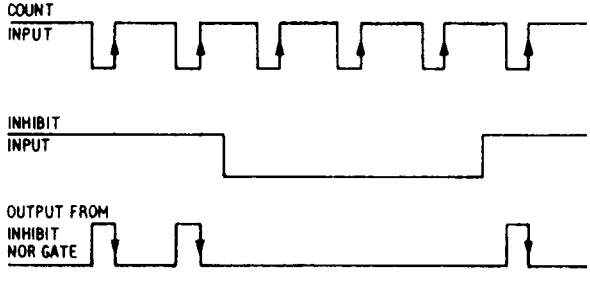


Fig. 4b. Correct Inhibit Operation

1.3 Direction Control

Count direction is controlled by a 'D' latch (see section 1.1) which can be set, for counting up, by taking the mode input high and reset, for counting down, by taking the mode input low. The clock input of this latch is connected to the count input and the state of the latch may therefore be changed only when the count input is high. If the count direction is to be reversed at a particular count then the state of the direction latch must be changed immediately that count is reached, whilst the count input is still high. Waiting until the count input has gone low again will result in the count direction not being reversed until the count input has gone high again, by which time an additional count will have been made in the original direction. Incorrect and correct operation of the direction control is illustrated in figures 5a and 5b.

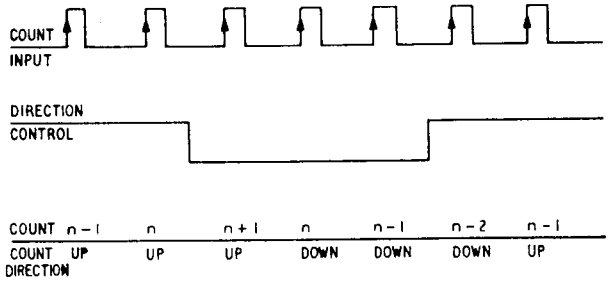


Fig. 5a. Incorrect Operation of Direction Control

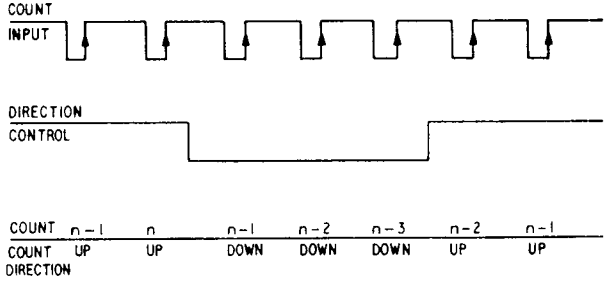


Fig. 5b. Correct Operation of Direction Control

1.4 Counter Reset

The counter may be reset to zero at any time by taking the clear input low. The counter will remain reset until the clear input is taken high again. In addition the ZN1040E incorporates a 'power-on' reset facility which resets the counter to zero when the power is first applied to the IC. This function is not available in the ZN1040AE.

Whichever version of the IC is used, care must be taken to set the direction latch to the correct state immediately after switch-on, otherwise the initial count may be made in the wrong direction. This may occur if the count input is low at switch-on since the direction latch may then set in either state. It is therefore advisable to ensure that the count input is normally high so that the direction latch will be set to the correct state at switch-on by the count direction control.

1.5 Carry/Borrow Output

The carry/borrow output (pin 19) may be used as an overflow indicator or to facilitate direct cascading of ZN1040's. When the count direction is UP then the carry output will go high on the next low-going edge of the count input after a count of 9999 is reached. The carry output will go low again on the next high-going edge at the count input, when the count changes to 0000.

When the ZN1040 is in the count DOWN mode then the carry output will go high on the next low-going edge at the count input after the counter reaches 0000. The carry output will go low again on the next high-going edge at the count input, when the count changes to 9999. In either case the carry output is subject to a propagation delay, t_C of typically 75 ns, relative to the count input edges.

Carry output timing for both up and down counting is shown in figures 6a and 6b.

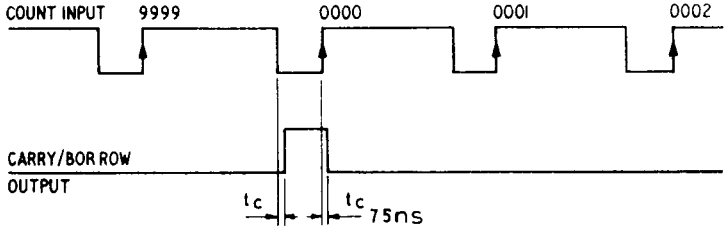


Fig. 6a. Carry Output Timing for Up Count

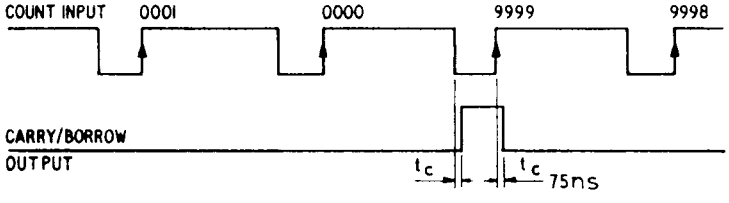


Fig. 6b. Carry Output Timing for Down Count

SECTION 2. COUNT MEMORY

2.1 Display Latch

Each of the decade counters in the ZN1040 produces a binary coded decimal (BCD) number synchronous with the count input. The counter outputs are connected to the inputs of data latches which can store the counter outputs for subsequent display. Whilst the transfer input (pin 24) is high the latches are transparent, and their outputs will follow the data present at the inputs. When the transfer input is taken low the input data present at that instant will be held in the latches and will be unaffected by subsequent changes in the counter outputs.

SECTION 3. DISPLAY MULTIPLEXING

3.1 Multiplex System

In order to economise on pin connections to the ZN1040 and to simplify connection to displays the outputs of the ZN1040 are multiplexed, i.e. the four BCD output digits from the data latches are connected, one at a time, to a common data bus. The multiplexed BCD data is connected to four output pins directly and also via a BCD seven-segment decoder driver so that multiplexed seven-segment outputs are also available. Four digit select outputs indicate which digit is present on the BCD or 7-segment outputs at a particular time.

3.2 Internal Multiplex Oscillator

Clock pulses for the multiplex sequence are generated by the oscillator circuit shown in figure 7. An internal capacitor of nominally 5 pF is charged via a nominal 700k resistor to the upper threshold voltage of the Schmitt trigger. The Schmitt output then goes high, turning on the transistor, and the capacitor discharges through a nominal 10k resistor to the lower threshold of the Schmitt trigger, at which point the output of the Schmitt goes low, the transistor turns off, and the cycle repeats. The nominal frequency of the multiplex oscillator is 500 kHz but this can be altered by adding an external capacitor between pin 12 and ground. A graph of MPX frequency v. external capacitance is shown in figure 8. To ensure stable oscillator operation it is recommended that an external capacitor with a value of at least 100 pF should always be used. When displays are used with the ZN1040 it will frequently be necessary to keep the MPX frequency below 1 kHz to avoid 'ghosting' due to the storage time of the digit-drive transistors. On the other hand the MPX frequency should not be lower than a few hundred Hz otherwise display flicker may become noticeable.

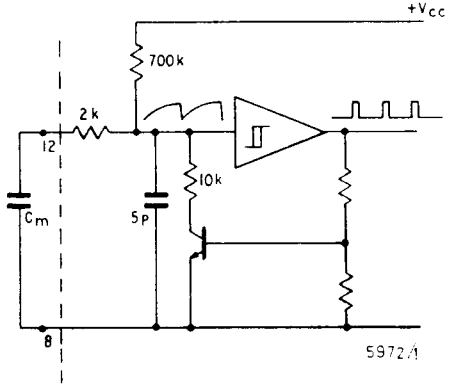


Fig. 7. Multiplex Oscillator Circuit

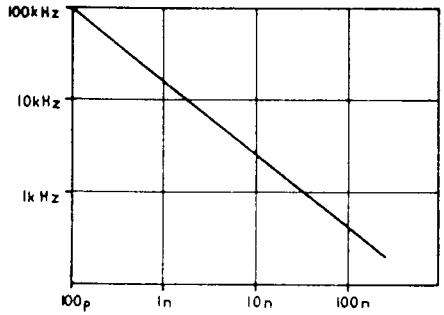


Fig. 8. Nominal MPX Oscillator Frequency v. External Capacitance

3.3 External MPX Oscillator

Since the Schmitt trigger input of the MPX oscillator is only coupled to three fairly high impedances (10k and 700k resistors, and a 5 pF capacitor) it is a simple matter to override the oscillator action by driving pin 12 from a low impedance external source such as a normal TTL output. Taking pin 12 high will hold the MPX oscillator output high, whilst taking pin 12 low will hold the output low. In this way the multiplexed BCD outputs of the ZN1040 can be synchronised to an external clock. This can be useful if, for example, the BCD output data is to be compared, digit by digit, with some preset limit. In this case the MPX frequency must at least be four times the input frequency to ensure that each digit has been compared before the next input pulse arrives.

The MPX input can be overdriven at frequencies up to 1 MHz which means that the BCD outputs can be compared at count frequencies up to 250 kHz.

3.4 Multiplex Sequence Generation

The output of the MPX oscillator is connected to the clock input of a sequence generator which is essentially a four-stage ring counter. This produces a sequence of four output pulses which are used to gate the BCD outputs, in sequence, on to the four output lines as shown in figure 9.

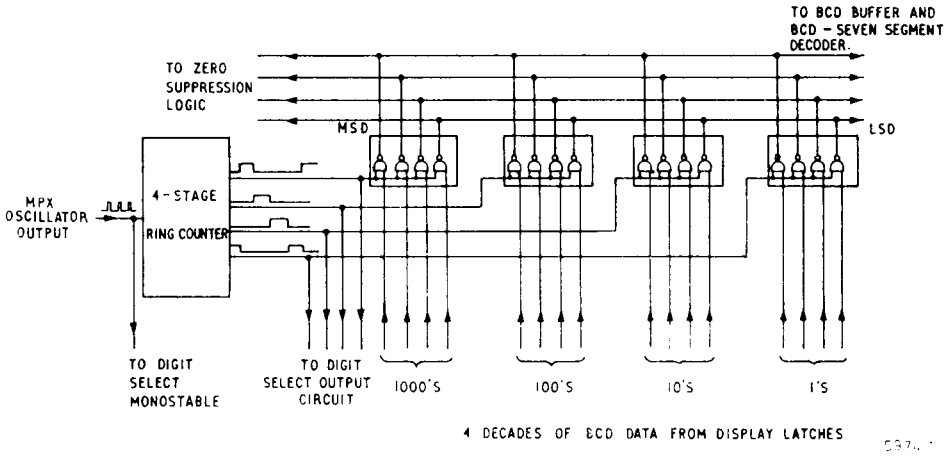


Fig. 9. Operation of Digit Multiplexing Circuit

3.5 Digit Select Output Circuit

The four digit select outputs are derived from the outputs of the MPX sequence ring counter using the circuit shown in figure 10.

To minimise digit drive overlap they are first passed through NAND gates, and a monostable triggered by the MPX oscillator takes a 200 ns 'bite' from the high-going edge of each pulse to provide interdigit blanking.

Further gating allows the selection of either high-going or low-going digit select pulses, thus allowing either common-anode or common-cathode displays to be driven using simple circuits. When the digit select sense input (pin 13) is high then the digit select pulses are high-going, when this input (pin 13) is low the digit select pulses are low-going. A timing diagram for high-going digit select pulses is given in figure 11. For low-going pulses the digit select waveforms are simply inverted. One digit select equivalent output circuit is shown in figure 12.

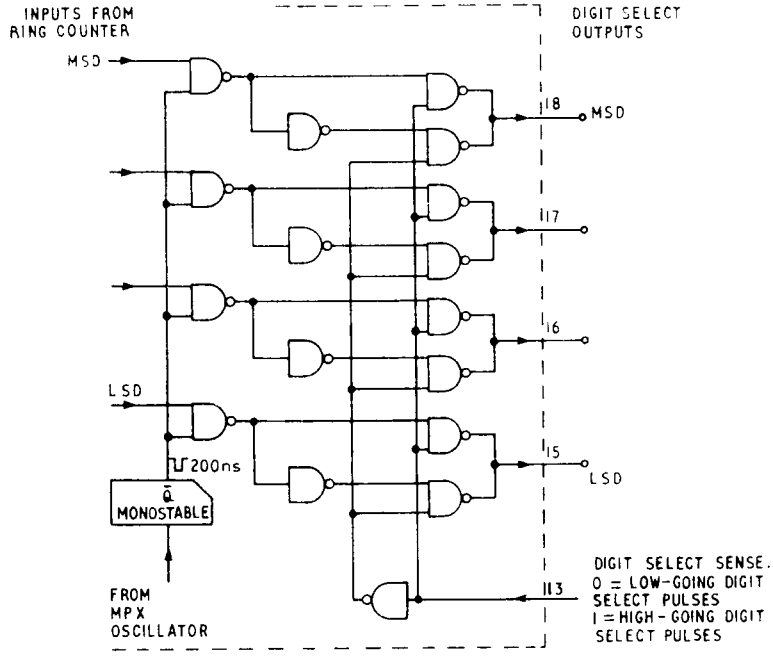


Fig. 10. Digit Select Logic

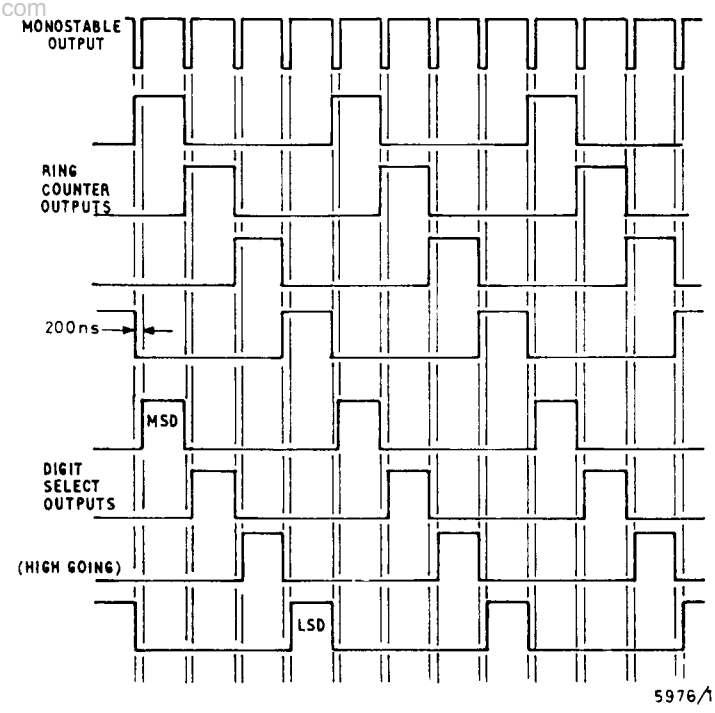


Fig. 11. Digit Select Timing

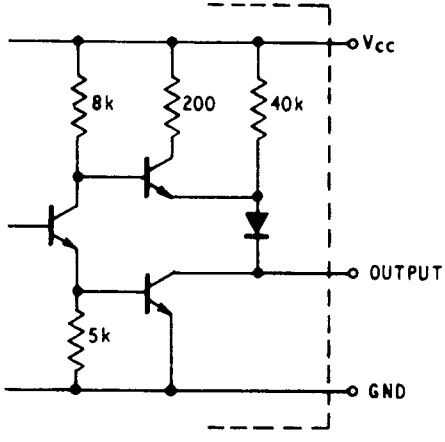


Fig. 12. Digit Select Output Circuit

3.6 Seven-segment Outputs

The seven segment outputs (pins 4-7, 9-11) are active low and can sink at least 50 mA in the case of the ZN1040E and 40 mA in the case of the ZN1040AE. The segment cathodes of common-anode displays may thus be driven directly. Display driving is discussed in detail in section 5. The output circuit for one segment is shown in figure 13.

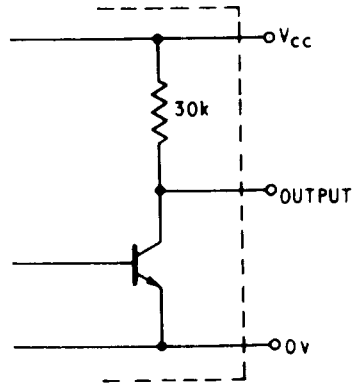


Fig. 13. Segment Output Circuit

3.7 BCD Outputs

The BCD output for each digit appears on the BCD output lines synchronous with the appropriate digit select pulse. However, since the MPX sequence gating is driven directly from the ring counter outputs, there is no inter-digit gap between one set of BCD data and the next. During the transition between digits the BCD data must therefore be considered invalid. If the BCD data is to be utilised (e.g. stored in an external latch or compared) then the simplest way to overcome this problem is to make use of the leading edge of the digit select pulse to indicate when the data is valid. This is illustrated in figure 14.

Similar comments also apply to the seven-segment outputs, but since these are normally used only for display driving, the problem does not usually arise.

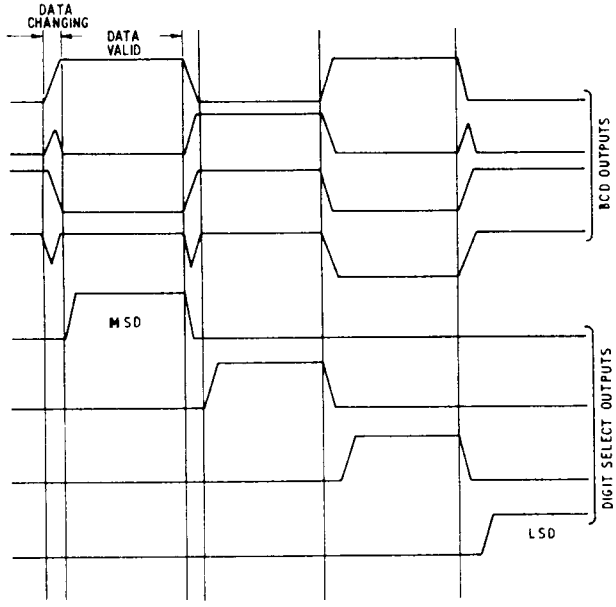


Fig. 14. BCD Output Timing

SECTION 4. ZERO SUPPRESSION, BLANKING, DECIMAL POINT AND LAMP TEST

The ZN1040 provides automatic blanking of leading zeroes in the display, thus improving readability. A decimal point input is also provided which allows leading zeroes to be displayed where these occur after the decimal point. A blanking input is provided to inhibit the display together with a lamp test input to check the operation of all display segments.

These sections of the ZN1040 circuit are shown in figure 15.

4.1 Blanking

Operation of the blanking input is extremely simple. When this input is high the seven-segment decoder functions normally and when this input is taken low the output of AND gate N6 goes low and the seven segment output transistors are all turned off, blanking the display.

4.2 Zero Blanking

Zero blanking operates on the principle of leaving the display blanked until non-zero data is detected at the outputs of the digit select gates. The trailing edge of the LSD output of the ring counter triggers a monostable which sets flip-flop N4/N5. The output of N4 holds one input of N6 low and the display is therefore blanked. It remains blanked until a non-zero digit appears on the BCD data bus, thus taking one or more of the inputs of NOR gate N3 high. The output of N3 then goes low resetting flip-flop N4/N5 so that the leading non-zero digit and all subsequent digits are displayed.

Should all four digits be zero then the flip-flop will be reset when the LSD output of the ring counter goes high and the output of N1 goes low. This ensures that the right hand digit (LSD) is always displayed, even if zero.

4.3 D.P. Input

If not used, the decimal point input is normally held high. If a decimal point is used in the display then the D.P. input can be utilised to prevent the possibility of a blanked digit appearing after the decimal point. This is achieved by feeding a low-going pulse into the D.P. input synchronously with the digit select pulse for the digit where the decimal point is to appear. This resets flip-flops N4/N5 so that the display is unblanked for this digit and all subsequent digits even if there are leading zeroes after the decimal point. Depending on whether the display has left or right-hand decimal points the display will be of the form .0 —— or 0. ——. If there is to be a decimal point before the MSD then left-hand point displays must obviously be used. If no leading zero blanking is required then the D.P. input is simply grounded, when all digits will be displayed.

A timing diagram for the D.P. input is shown in figure 11. Applications circuits using the decimal point are given in section 5. It should be pointed out that the ZN1040 does not produce an output to drive the decimal point of a display, this must be done using a simple external circuit several of which are shown in section 5.

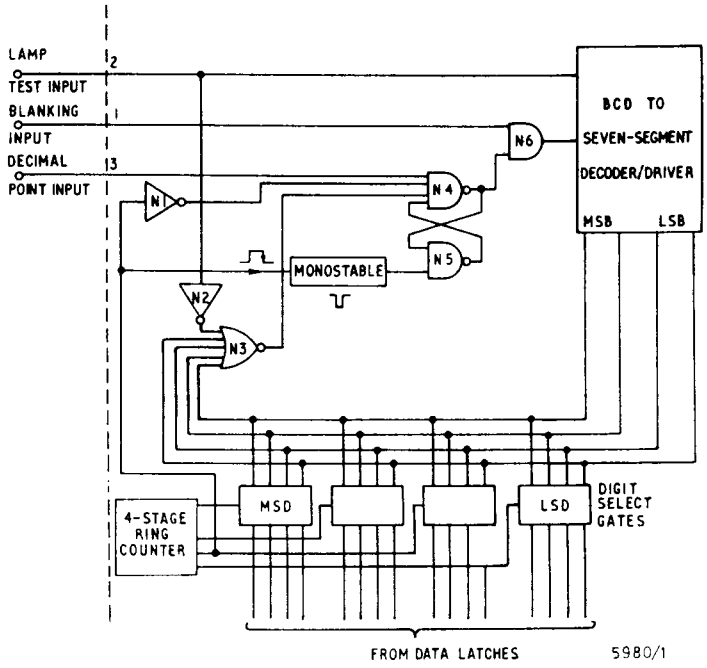


Fig. 15. Zero Suppression, Lamp Test and Blanking

4.4 Lamp Test

Operation of the lamp test function is quite simple. Taking the lamp test input low applies the BCD code 1000 (8) to the inputs of the BCD seven-segment decoder/driver. Simultaneously flip-flop N4/N5 is reset via N2 and N3, the output of N6 goes high, the display is unblanked and displays 8888. The blanking input must be high for lamp test to operate as a low blanking input will override the lamp test input and blank the display.

SECTION 5. USING THE ZN1040

5.1 Driving Common Anode LED Displays

Common anode LED displays can be driven with a minimum of external components, using the circuit of figure 16. The segment cathodes are driven directly (via current limit resistors) whilst the low going digit outputs turn on PNP digit drive transistors. As the display is multiplexed, and each digit is thus active for only a quarter of the time, the segment resistors should be chosen to give a peak current of approximately four times the required average current by using the equation:

$$R = \frac{V_{CC} - V_f}{4I_S}$$

V_{CC} = supply voltage (volts)
V_f = LED forward voltage drop
I_S = average segment current (A)
R = segment resistance (Ω)

The base resistors of the PNP digit drive transistors should be chosen such that the transistors receive sufficient base current to turn them fully on.

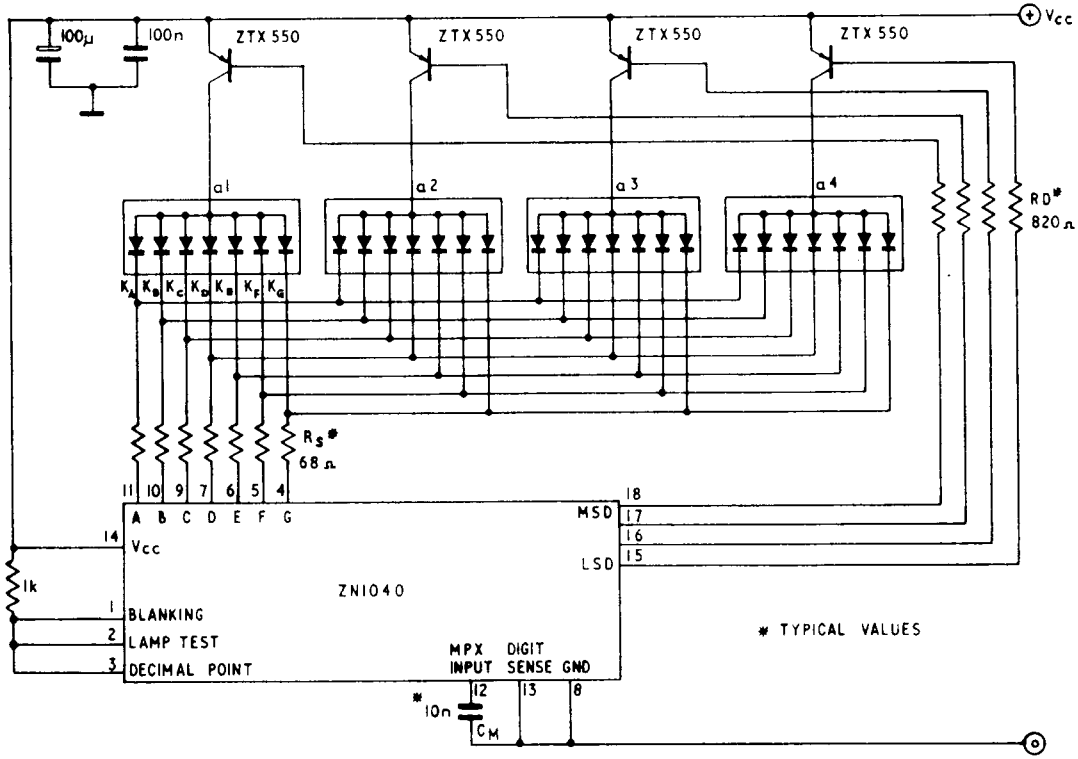


Fig. 16. Interfacing to Common-Anode LED Displays

5.2 Driving Common Cathode LED Displays

A circuit for driving common cathode LED displays is given in figure 17. Since the segment outputs are only active low it is necessary to use PNP segment drive transistors. High going digit select outputs are used to turn on NPN digit drive transistors. As with the common anode display, the segment resistors should be chosen to give the required segment current, and the transistor base resistors should be chosen to turn the transistors hard on. In both cases it is advisable to use displays which are optimised for multiplexed operation. Note that, since the digit outputs have to supply a significant base current to the digit drive transistors, the high level output voltage is less than the minimum specified to drive a TTL input. The digit select outputs therefore cannot be used as normal logic outputs with this circuit configuration.

Good decoupling of the supply to the ZN1040 is essential to avoid erratic counting and other problems. This is especially true when displays are being driven because of the large current pulses taken by these devices. It is therefore recommended that an electrolytic capacitor of between 100 μF and 1000 μF and a 100 nF ceramic capacitor be connected between $+V_{CC}$ and ground, as close as possible to the appropriate pins of the ZN1040.

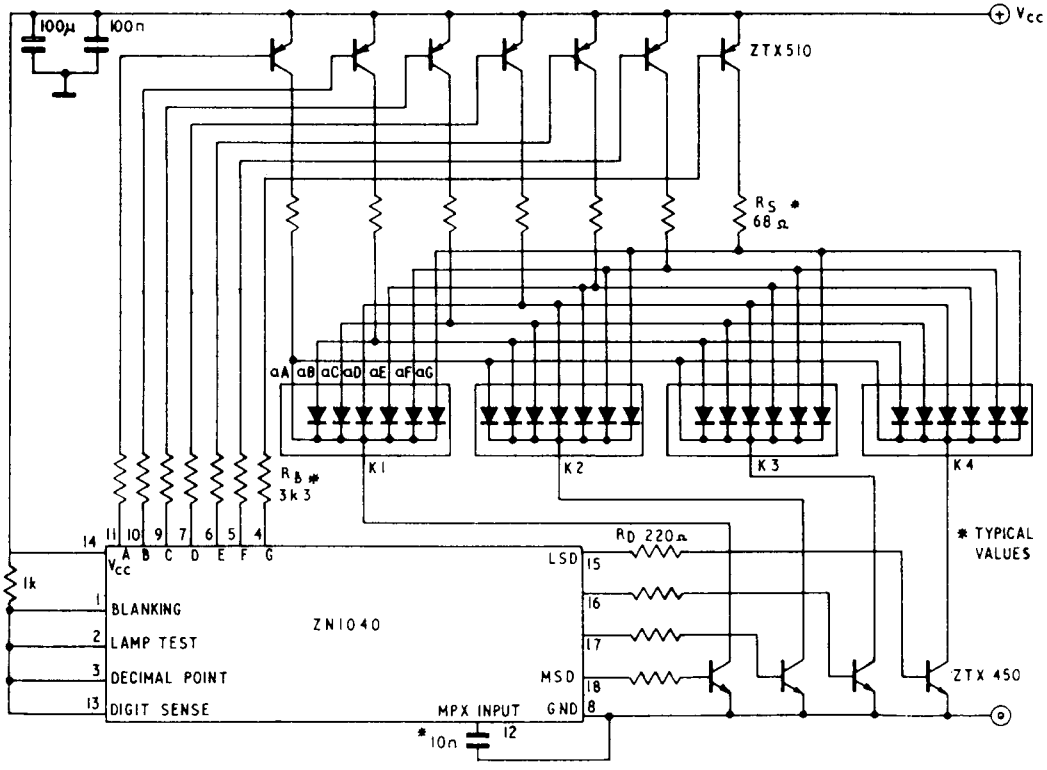


Fig. 17. Interfacing to Common-Cathode LED Displays

5.3 Using the Decimal Point Input

(a) Common Anode Display

Figure 18 shows a circuit which allows a decimal point to be displayed before any one of the display digits. When all the decimal point inputs are low then the 'wire-ANDed' outputs of N5 to N8 are all high and no decimal point is displayed. If for example D.P. input 2 is taken high then, when digit select output 2 goes low, both inputs of N6 will be high. The output of N6 will therefore go low synchronous with the digit 2 select pulse which will apply a low going pulse to the D.P. input of the ZN1040 to unblank the display and also to the decimal point cathode of the display to light decimal point 2.

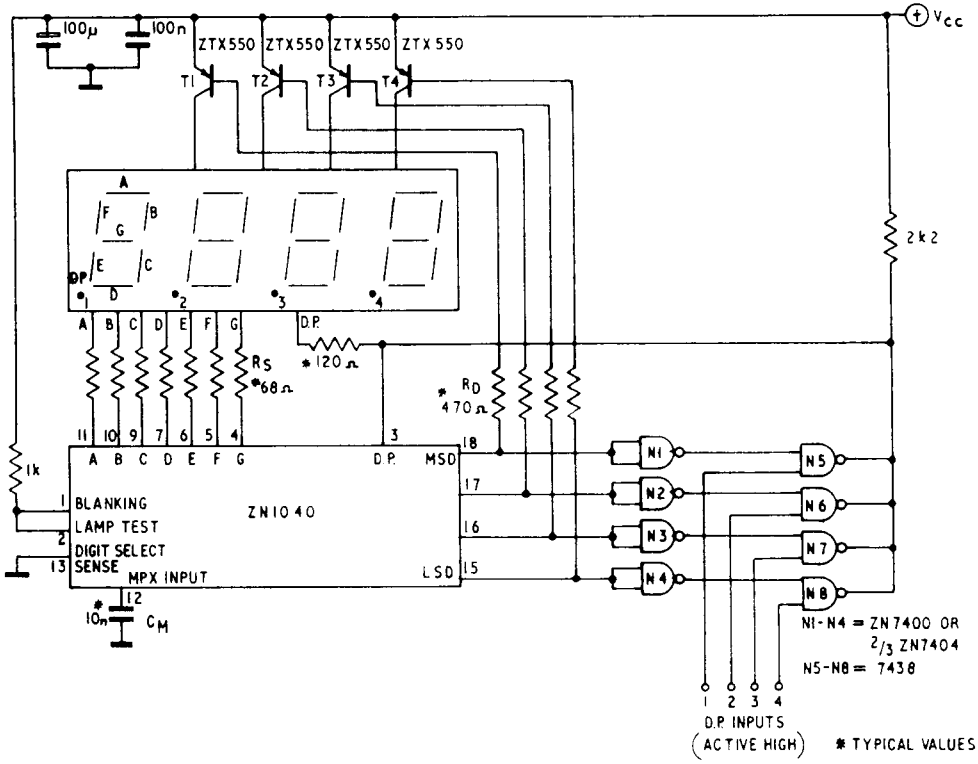


Fig. 18. Driving a Multiplexed Common-Anode Display with Decimal Point

(b) Common Cathode Display

The principle of this circuit is identical to that of figure 18 with minor circuit differences to take account of the different type of display. The digit select outputs are high-going, therefore no inverters are required at the inputs of the NAND gates. However, since the digit select outputs are used as logic outputs (see 5.2), buffers N1-N4 are interposed between them and the digit drive transistors. The wired AND output of N5-N8 turns on T8 when it goes low synchronous with the chosen digit select pulse thus driving the decimal point anode.

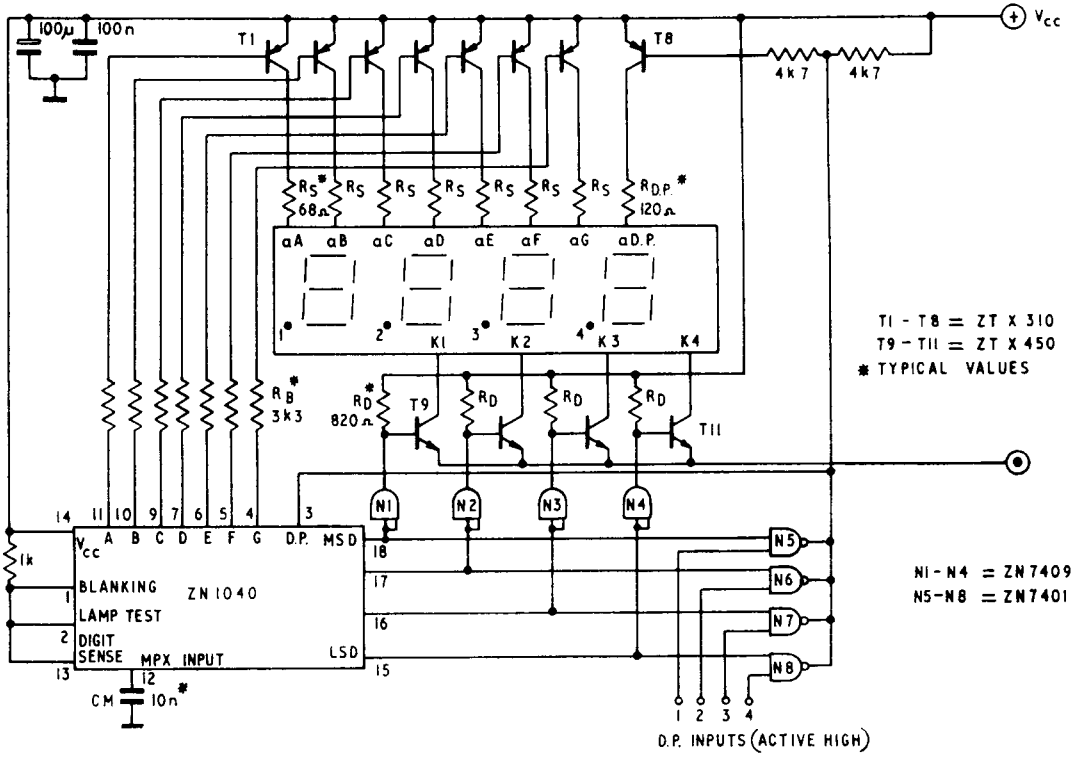


Fig. 19. Driving a Multiplexed Common-Cathode Display with Decimal Point

5.4 Cascading the ZN1040

If a count greater than 4 digits is required then two ZN1040's may be cascaded using the carry/borrow output; or additional TTL decade counters may be added. To cascade two ZN1040's the carry/borrow output of the less significant counter is connected to the inhibit input of the more significant counter and the count inputs are linked as shown in figure 20. The M.S.C. is thus inhibited until after the 9999th clock pulse when the inhibit input will be taken high by the carry output of the L.S.C. On the leading edge of the 1000th clock pulse the M.S.C. count will increase by 1 whilst the L.S.C. count will go to zero. After the carry propagation delay the carry output of the L.S.C. will go low and the M.S.C. will again be inhibited. A timing diagram for this sequence of events is shown in figure 21.

The leading zero blanking facility of the ZN1040 cannot be used directly in this application since the blanking circuits would operate independently for each device, leading to gaps in the display when the count was 999 or less, e.g. – – – 0 – 456.

This problem can be overcome by grounding the D.P. inputs of both counters thus inhibiting the zero blanking, or alternatively the D.P. input of the L.S.C. may be grounded giving zero blanking only on the first three digits of the M.S.C. If full zero blanking is required then the circuit given in Section 5.5 should be used.

When ZN1040's are cascaded then separate display interfacing will be used for each set of four digits.

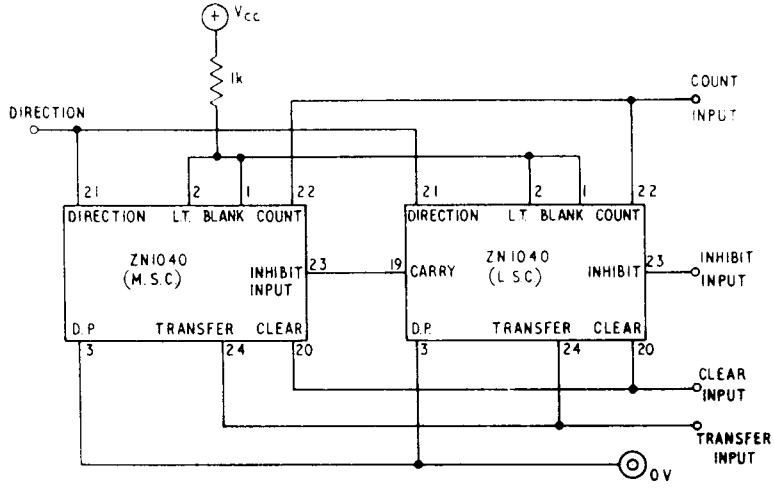


Fig. 20. Cascading ZN1040's without Leading Zero Blanking

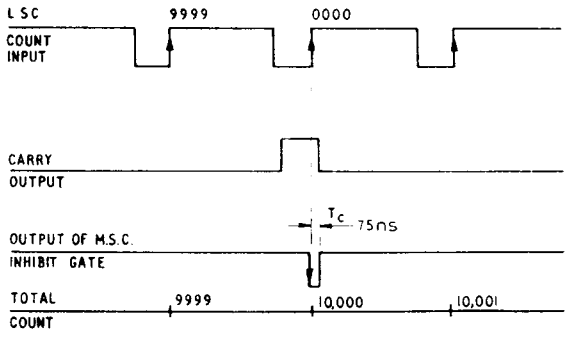


Fig. 21. Timing Diagram for Cascaded ZN1040's

5.5 Cascading ZN1040's with Leading Zero Blanking

The circuit of figure 22 allows cascading of two ZN1040's with full leading zero blanking. It operates by monitoring the BCD outputs of the more significant counter. When these are all zero this counter is blanked and the less significant counter is allowed to operate with leading zero suppression. When any of the BCD outputs is non-zero then the M.S.C. is unblanked and operates with leading zero suppression whilst the zero blanking of the L.S.C. is inhibited. The BCD outputs of the M.S.C. are monitored by a four input open collector NOR gate comprising N2 and N3. Whilst the multiplexed BCD data is zero the outputs of N2 and N3 are high, the output of N1 is low, so that M.S.C. is blanked. The output of N4 holds the D.P. input of the L.S.C. high and therefore the leading zero blanking operates normally.

If, at any time during the multiplex sequence, the BCD data is non-zero, then the output of N2 or N3 will go low discharging C1 rapidly. The D.P. input of the L.S.C. will thus be pulled low, inhibiting the zero blanking, whilst the output of N1 is high, unblanking the M.S.C. If only one of the BCD digits is non-zero, then C1 will be discharged only once during each multiplex sequence and will charge in the interval. The time constant (R2 + R3) C1 must therefore be made considerably longer than one multiplex sequence to ensure that the input to N1 remains low in this event.

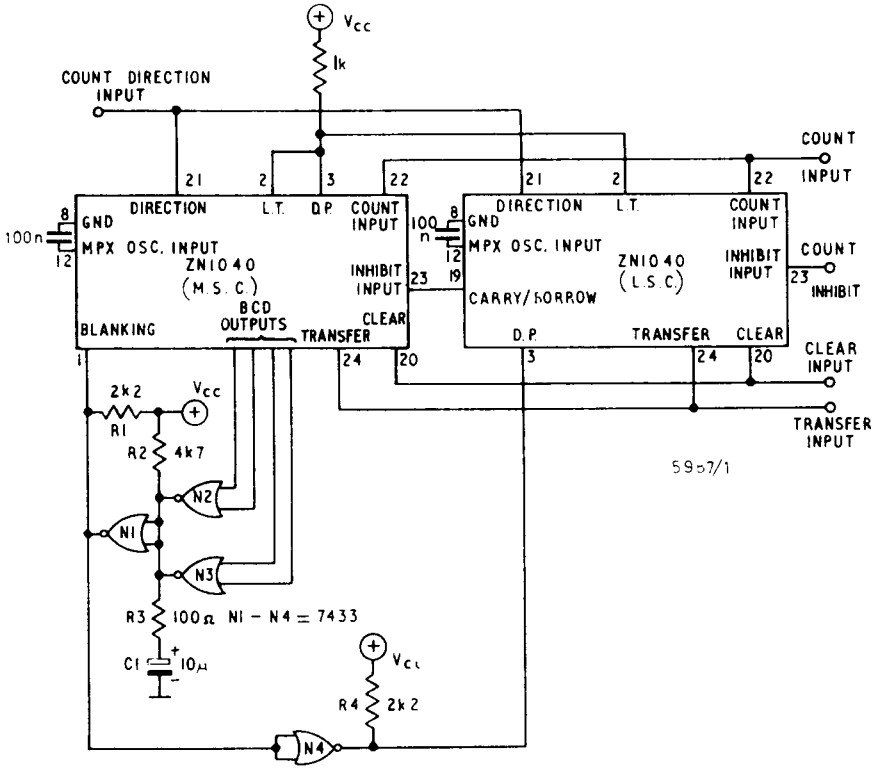


Fig. 22. Cascading ZN1040's with Leading Zero Blanking