

General Description

The AAT3239 MicroPower low dropout (LDO) linear regulator is ideally suited for portable applications where very fast transient response, extended battery life, and small size are critical. The AAT3239 has been specifically designed for high-speed turn-on and turn-off performance, fast transient response, good power supply rejection ratio (PSRR), and is reasonably low noise, making it ideal for powering sensitive circuits with fast switching requirements.

Other features include low quiescent current, typically 70µA, and low dropout voltage which is typically less than 400mV at 300mA. The device is output short-circuit protected and has a thermal shutdown circuit for additional protection under extreme operating conditions.

The AAT3239 also features a low-power shutdown mode for extended battery life. A reference bypass pin has been provided to improve PSRR performance and output noise by connecting a small external capacitor from the AAT3239's reference output to ground.

The AAT3239 is available in a Pb-free, 8-pin TSOPJW package in factory-programmed voltages.

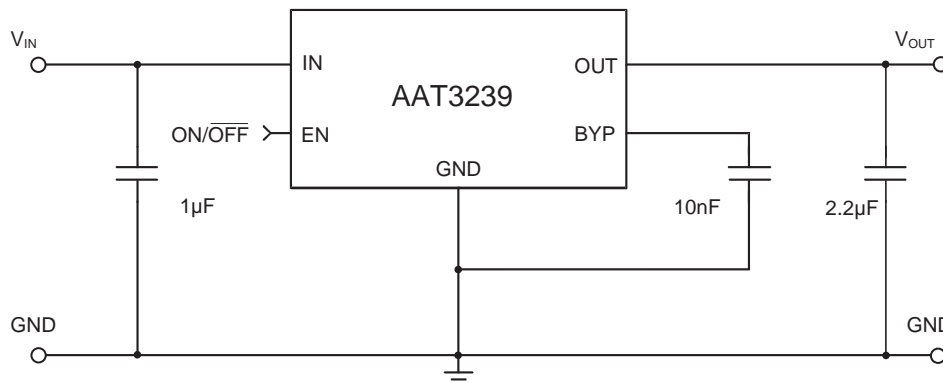
Features

- 500mA Output Current
- Low Dropout: 400mV at 300mA
- High Accuracy: ±2.0%
- 70µA Quiescent Current
- Fast Line and Load Transient Response
- High-Speed Device Turn-On and Shutdown
- High Power Supply Rejection Ratio
- Low Self Noise
- Short-Circuit Protection
- Over-Temperature Protection
- Uses Low Equivalent Series Resistance (ESR) Ceramic Capacitors
- Noise Reduction Bypass Capacitor
- Shutdown Mode for Longer Battery Life
- Low Temperature Coefficient
- TSOPJW 8-Pin Package

Applications

- Cellular Phones
- Digital Cameras
- Notebook Computers
- Personal Portable Electronics
- Portable Communication Devices

Typical Application

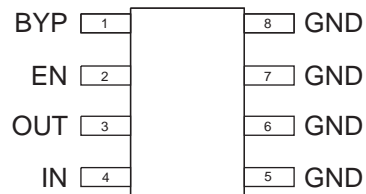


Pin Descriptions

Pin #	Symbol	Function
1	BYP	Bypass capacitor connection; to improve AC ripple rejection, connect a 10nF capacitor to GND. This will also provide a soft-start function.
2	EN	Enable pin; this pin should not be left floating. When pulled low, the PMOS pass transistor turns off and all internal circuitry enters low-power mode, consuming less than 1µA.
3	OUT	Output pin; should be decoupled with 2.2µF ceramic capacitor.
4	IN	Input voltage pin; should be decoupled with 1µF or greater capacitor.
5, 6, 7, 8	GND	Ground connection pin.

Pin Configuration

TSOPJW-8
(Top View)



Absolute Maximum Ratings¹

Symbol	Description	Value	Units
V_{IN}	Input Voltage	6	V
$V_{ENIN(MAX)}$	Maximum EN to Input Voltage	0.3	V
I_{OUT}	DC Output Current	$P_D/(V_{IN} - V_O)$	mA
T_J	Operating Junction Temperature Range	-40 to 150	°C

Thermal Information²

Symbol	Description	Rating	Units
Θ_{JA}	Maximum Thermal Resistance	90	°C/W
P_D	Maximum Power Dissipation ³ ($T_A = 25^\circ\text{C}$)	1.11	W

Recommended Operating Conditions

Symbol	Description	Rating	Units
V_{IN}	Input Voltage ⁴	$(V_{OUT} + V_{DO})$ to 5.5	V
T	Ambient Temperature Range	-40 to +85	°C

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on a demo board.
3. Derate 11.1mW/°C above 25°C.
4. To calculate minimum input voltage, use the following equation: $V_{IN(MIN)} = V_{OUT(MAX)} + V_{DO(MAX)}$ as long as $V_{IN} \geq 2.5\text{V}$.

Electrical Characteristics¹

$V_{IN} = V_{OUT(NOM)} + 1.2V$ for V_{OUT} options greater than 1.5V. $V_{IN} = 2.5$ for $V_{OUT} \leq 1.5V$. $I_{OUT} = 1mA$, $C_{OUT} = 2.2\mu F$, $C_{IN} = 1\mu F$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are $T_A = 25^\circ C$.

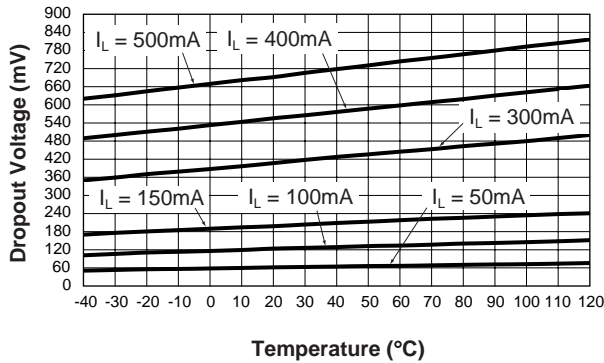
Symbol	Description	Conditions	Min	Typ	Max	Units	
V_{OUT}	Output Voltage Tolerance	$I_{OUT} = 1mA$ to $300mA$	$T_A = 25^\circ C$	-1.5		1.5	%
			$T_A = -40$ to $85^\circ C$	-2.5		2.5	
		$I_{OUT} = 1mA$ to $500mA$	$T_A = 25^\circ C$	-2.0		2.0	
			$T_A = -40$ to $85^\circ C$	-3.5		3.5	
I_{OUT}	Output Current	$V_{OUT} > 1.2V$	500			mA	
V_{DO}	Dropout Voltage ^{2,3}	$I_{OUT} = 300mA$		400	600	mV	
		$I_{OUT} = 500mA$		0.8	1.2	V	
I_{SC}	Short-Circuit Current	$V_{OUT} < 0.4V$		600		mA	
I_Q	Ground Current	$V_{IN} = 5V$, No Load, $EN = V_{IN}$		70	125	μA	
I_{SD}	Shutdown Current	$V_{IN} = 5V$, $EN = 0V$			1	μA	
$\frac{\Delta V_{OUT}}{V_{OUT}} \cdot \Delta V_{IN}$	Line Regulation	$V_{IN} = V_{OUT} + 1$ to $5.0V$			0.09	%/V	
$\Delta V_{OUT}(\text{line})$	Dynamic Line Regulation	$V_{IN} = V_{OUT} + 1V$ to $V_{OUT} + 2V$, $I_{OUT} = 500mA$, $T_R/T_F = 2\mu s$		2.5		mV	
$\Delta V_{OUT}(\text{load})$	Dynamic Load Regulation	$I_{OUT} = 1mA$ to $300mA$, $T_R < 5\mu s$		100		mV	
		$I_{OUT} = 1mA$ to $500mA$, $T_R < 5\mu s$		120			
t_{ENDLY}	Enable Delay Time	$BYP = \text{Open}$		15		μs	
$V_{EN(L)}$	Enable Threshold Low				0.6	V	
$V_{EN(H)}$	Enable Threshold High		1.5			V	
I_{EN}	Leakage Current on Enable Pin	$V_{EN} = 5V$			1	μA	
PSRR	Power Supply Rejection Ratio	$I_{OUT} = 10mA$, $C_{BYP} = 10nF$	1kHz		67	dB	
			10kHz		47		
			1MHz		45		
T_{SD}	Over-Temperature Shutdown Threshold			145		$^\circ C$	
T_{HYS}	Over-Temperature Shutdown Hysteresis			12		$^\circ C$	
e_N	Output Noise	Noise Power BW = $300Hz$ to $50kHz$		50		μV_{rms}	
TC	Output Voltage Temperature Coefficient			22		ppm/ $^\circ C$	

1. The AAT3239 is guaranteed to meet performance specifications over the $-40^\circ C$ to $+85^\circ C$ operating temperature range and is assured by design, characterization, and correlation with statistical process controls.
2. V_{DO} is defined as $V_{IN} - V_{OUT}$ when V_{OUT} is 98% of nominal.
3. For $V_{OUT} < 2.1V$, $V_{DO} = 2.5V - V_{OUT}$.

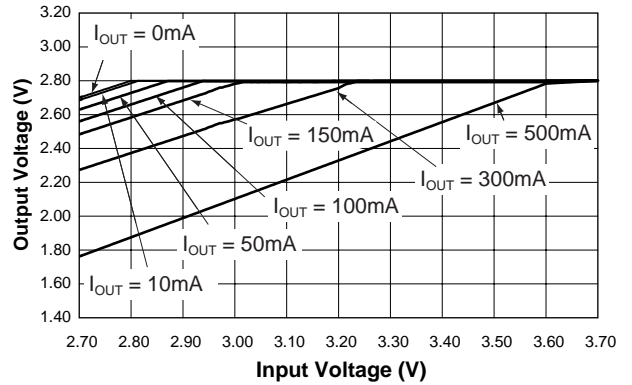
Typical Characteristics

Unless otherwise noted, $V_{IN} = 5V$, $T_A = 25^\circ C$.

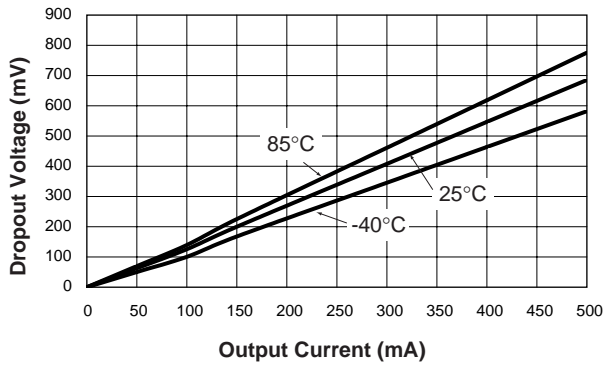
Dropout Voltage vs. Temperature



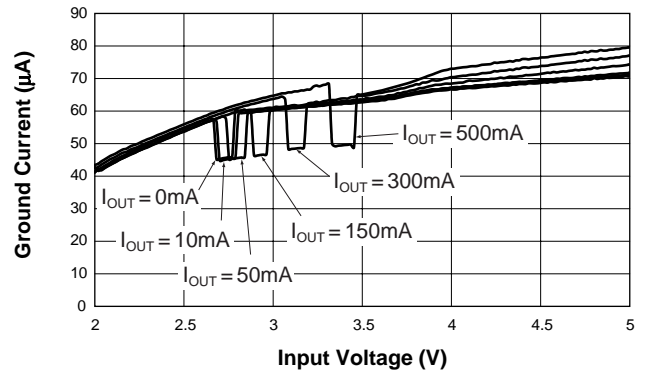
Dropout Characteristics



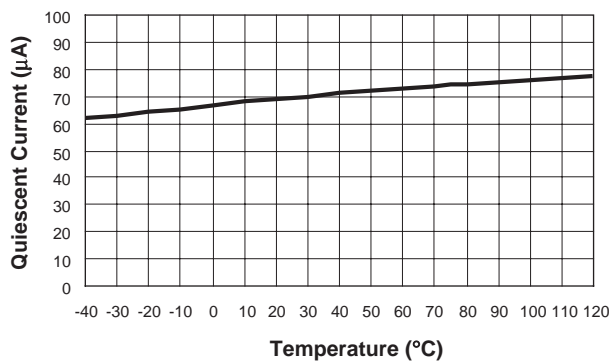
Dropout Voltage vs. Output Current



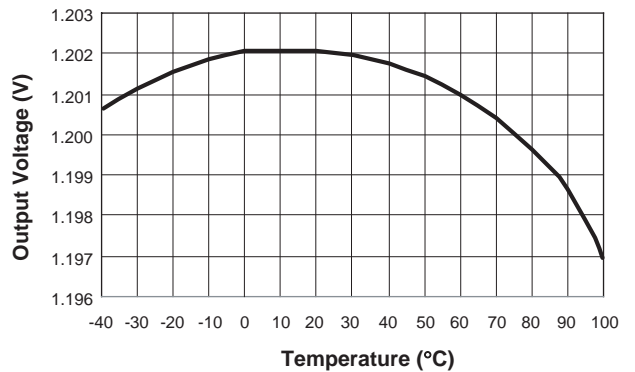
Ground Current vs. Input Voltage



Quiescent Current vs. Temperature



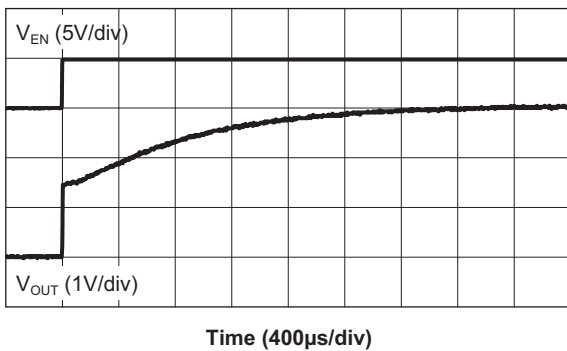
Output Voltage vs. Temperature



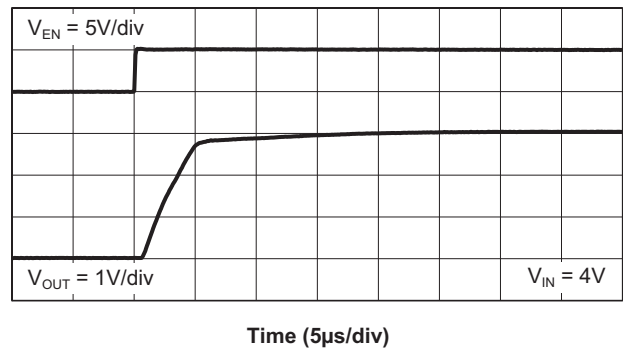
Typical Characteristics

Unless otherwise noted, $V_{IN} = 5V$, $T_A = 25^\circ C$.

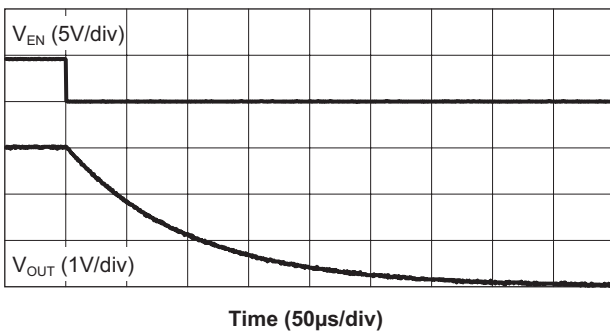
Initial Power-Up Response Time
 $(C_{BYP} = 10nF)$



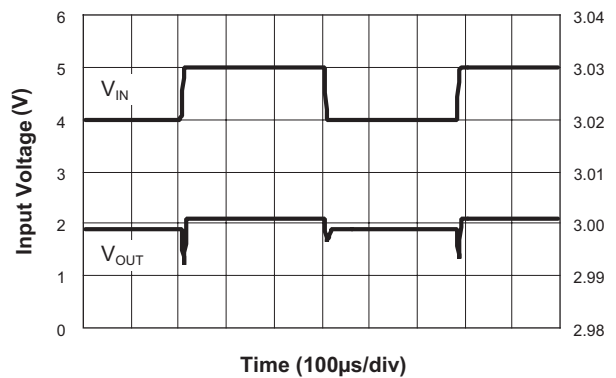
Turn-On Time From Enable (V_{IN} present)
 $(C_{BYP} = 10nF)$



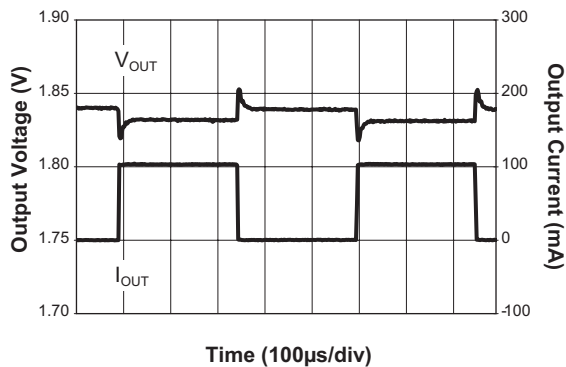
Turn-Off Response Time
 $(C_{BYP} = 10nF)$



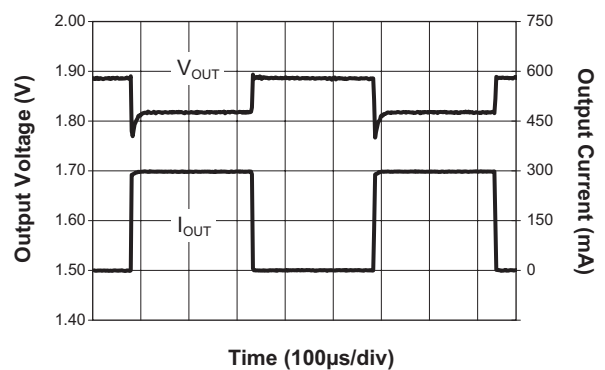
Line Transient Response



Load Transient Response 100mA



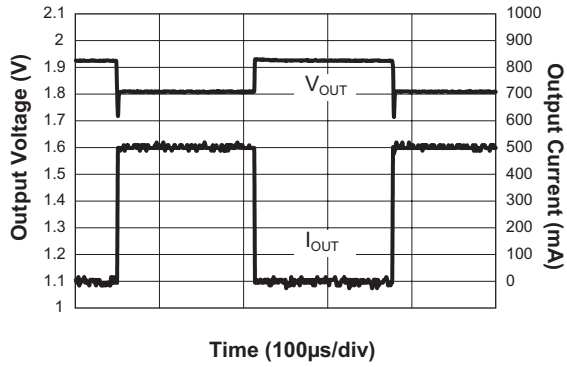
Load Transient Response 300mA



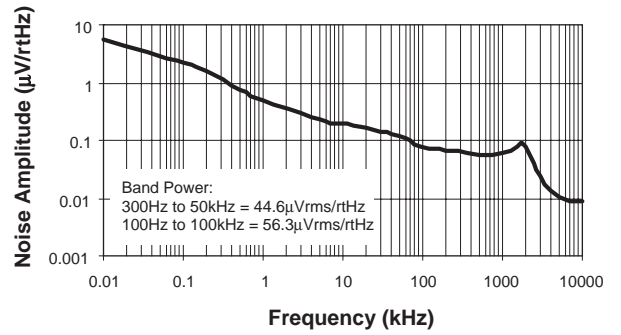
Typical Characteristics

Unless otherwise noted, $V_{IN} = 5V$, $T_A = 25^\circ C$.

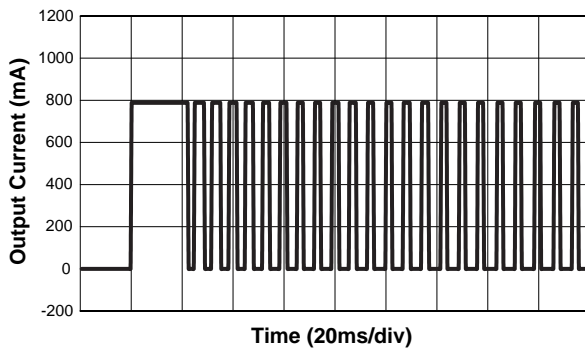
Load Transient Response 500mA



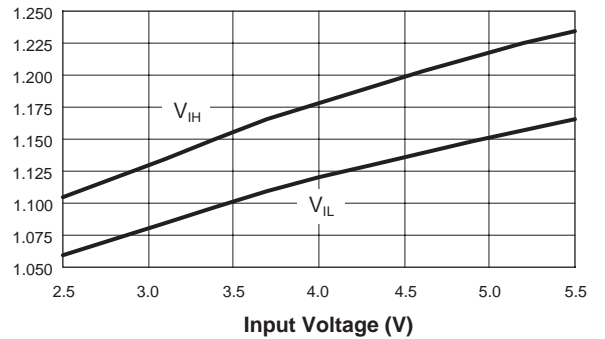
AAT3239 Self Noise
($C_{OUT} = 10\mu F$, ceramic)



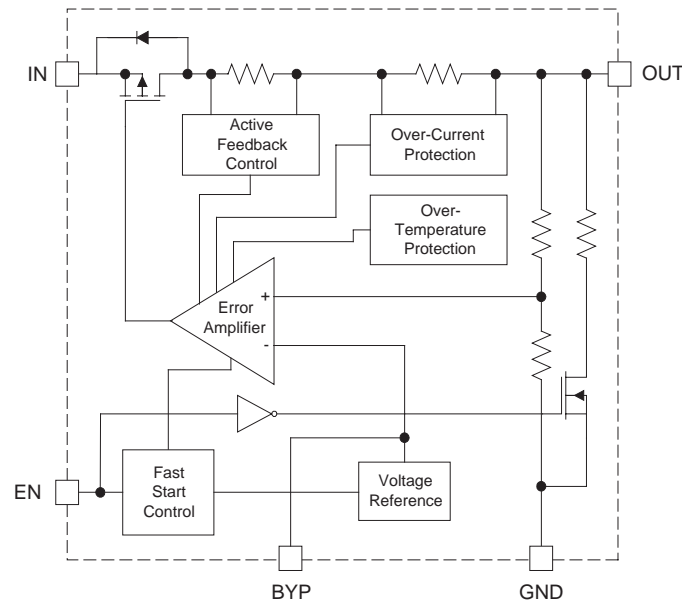
Over-Current Protection



V_{IH} and V_{IL} vs. V_{IN}



Functional Block Diagram



Functional Description

The AAT3239 is intended for LDO regulator applications where output current load requirements range from no load to 500mA. Refer to the Thermal Considerations discussion of this datasheet for details on maximum power dissipation.

The advanced circuit design of the AAT3239 has been specifically optimized for very fast start-up and shutdown timing. This CMOS LDO has been tailored for superior transient response characteristics, a trait which is particularly important for applications that require fast power supply timing, such as GSM cellular telephone handsets.

The high-speed turn-on capability of the AAT3239 is enabled through the implementation of a fast start control circuit, which accelerates the power-up behavior of fundamental control and feedback circuits within the LDO regulator.

Fast turn-off response time is achieved by an active output pull-down circuit, which is enabled when the LDO regulator is placed in shutdown mode. This active fast shutdown circuit has no adverse effect on normal device operation.

The AAT3239 has very fast transient response characteristics, which is an important feature for

applications where fast line and load transient response are required. This rapid transient response behavior is accomplished through the implementation of an active error amplifier feedback control. This proprietary circuit design is unique to this MicroPower LDO regulator.

The LDO regulator output has been specifically optimized to function with low-cost, low-ESR ceramic capacitors. However, the design will allow for operation over a wide range of capacitor types.

A bypass pin has been provided to allow the addition of an optional voltage reference bypass capacitor to reduce output self noise and increase power supply ripple rejection. Device self noise and PSRR will be improved by the addition of a small ceramic capacitor in this pin. However, increased values of C_{BYPASS} may slow down the LDO regulator turn-on time.

This LDO regulator has complete short-circuit and thermal protection. The integral combination of these two internal protection circuits gives the AAT3239 a comprehensive safety system to guard against extreme adverse operating conditions. Device power dissipation is limited to the package type and thermal dissipation properties. Refer to the Thermal Considerations discussion of this datasheet for details on device operation at maximum output current loads.

Applications Information

To assure the maximum possible performance is obtained from the AAT3239, please refer to the following application recommendations.

Input Capacitor

Typically, a 1 μ F or larger capacitor is recommended for C_{IN} in most applications. A C_{IN} capacitor is not required for basic LDO regulator operation. However, if the AAT3239 is physically located more than three centimeters from an input power source, a C_{IN} capacitor will be needed for stable operation. C_{IN} should be located as closely to the device V_{IN} pin as practically possible. C_{IN} values greater than 1 μ F will offer superior input line transient response and will assist in maximizing the highest possible power supply ripple rejection.

Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_{IN} . There is no specific capacitor ESR requirement for C_{IN} . However, for 500mA LDO regulator output operation, ceramic capacitors are recommended for C_{IN} due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required between pins V_{OUT} and GND. The C_{OUT} capacitor connection to the LDO regulator ground pin should be made as direct as practically possible for maximum device performance.

The AAT3239 has been specifically designed to function with very low ESR ceramic capacitors. For best performance, ceramic capacitors are recommended.

Typical output capacitor values for maximum output current conditions range from 1 μ F to 10 μ F. Applications utilizing the exceptionally low output noise and optimum power supply ripple rejection characteristics of the AAT3239 should use 2.2 μ F or greater for C_{OUT} . If desired, C_{OUT} may be increased without limit.

In low output current applications where output load is less than 10mA, the minimum value for C_{OUT} can be as low as 0.47 μ F.

Bypass Capacitor and Low Noise Applications

A bypass capacitor pin is provided to enhance the low noise characteristics of the AAT3239 LDO regulator. The bypass capacitor is not necessary for operation of the AAT3239. However, for best device performance, a small ceramic capacitor should be placed between the bypass pin (BYP) and the device ground pin (GND). The value of C_{BYP} may range from 470pF to 10nF. For lowest noise and best possible power supply ripple rejection performance, a 10nF capacitor should be used. To practically realize the highest power supply ripple rejection and lowest output noise performance, it is critical that the capacitor connection between the BYP pin and GND pin be direct and PCB traces should be as short as possible. Refer to the PCB Layout Recommendations section of this document for examples.

There is a relationship between the bypass capacitor value and the LDO regulator turn-on and turn-off time. In applications where fast device turn-on and turn-off time are desired, the value of C_{BYP} should be reduced.

In applications where low noise performance and/or ripple rejection are less of a concern, the bypass capacitor may be omitted. The fastest device turn-on time will be realized when no bypass capacitor is used.

DC leakage on this pin can affect the LDO regulator output noise and voltage regulation performance. For this reason, the use of a low leakage, high quality ceramic (NPO or C0G type) or film capacitor is highly recommended.

Capacitor Characteristics

Ceramic composition capacitors are highly recommended over all other types of capacitors for use with the AAT3239. Ceramic capacitors offer many advantages over their tantalum and aluminum electrolytic counterparts. A ceramic capacitor typically has very low ESR, is lower cost, has a smaller PCB footprint, and is non-polarized. Line and load transient response of the LDO regulator is improved by using low-ESR ceramic capacitors. Since ceramic capacitors are non-polarized, they are not prone to incorrect connection damage.

Equivalent Series Resistance: ESR is a very important characteristic to consider when selecting a capacitor. ESR is the internal series resistance associated with a capacitor that includes lead resistance, internal connections, size and area, material composition, and ambient temperature. Typically, capacitor ESR is measured in milliohms for ceramic capacitors and can range to more than several ohms for tantalum or aluminum electrolytic capacitors.

Ceramic Capacitor Materials: Ceramic capacitors less than 0.1 μ F are typically made from NPO or C0G materials. NPO and C0G materials generally have tight tolerance and are very stable over temperature. Larger capacitor values are usually composed of X7R, X5R, Z5U, or Y5V dielectric materials. These two material types are not recommended for use with LDO regulators since the capacitor tolerance can vary more than $\pm 50\%$ over the operating temperature range of the device. A 2.2 μ F Y5V capacitor could be reduced to 1 μ F over temperature; this could cause problems for circuit operation. X7R and X5R dielectrics are much more desirable. The temperature tolerance of X7R dielectric is better than $\pm 15\%$.

Capacitor area is another contributor to ESR. Capacitors that are physically large in size will have a lower ESR when compared to a smaller sized capacitor of an equivalent material and capacitance value. These larger devices can improve circuit transient response when compared to an equal value capacitor in a smaller package size.

Consult capacitor vendor datasheets carefully when selecting capacitors for LDO regulators.

Enable Function

The AAT3239 features an LDO regulator enable/disable function. This pin (EN) is active high and is compatible with CMOS logic. To assure the LDO regulator will switch on, the EN turn-on control level must be greater than 1.5V. The LDO regulator will go into the disable shutdown mode when the voltage on the EN pin falls below 0.6V. If the enable function is not needed in a specific application, it may be tied to V_{IN} to keep the LDO regulator in a continuously on state.

When the LDO regulator is in shutdown mode, an internal 1.5k Ω resistor is connected between V_{OUT} and GND. This is intended to discharge C_{OUT} when the LDO regulator is disabled. The internal 1.5k Ω has no adverse effect on device turn-on time.

Short-Circuit Protection

The AAT3239 contains an internal short-circuit protection circuit that will trigger when the output load current exceeds the internal threshold limit. Under short-circuit conditions, the output of the LDO regulator will be current limited until the short-circuit condition is removed from the output or LDO regulator package power dissipation exceeds the device thermal limit.

Thermal Protection

The AAT3239 has an internal thermal protection circuit which will turn on when the device die temperature exceeds 145°C. The internal thermal protection circuit will actively turn off the LDO regulator output pass device to prevent the possibility of over-temperature damage. The LDO regulator output will remain in a shutdown state until the internal die temperature falls back below the 145°C trip point.

The combination and interaction between the short-circuit and thermal protection systems allow the LDO regulator to withstand indefinite short-circuit conditions without sustaining permanent damage.

No-Load Stability

The AAT3239 is designed to maintain output voltage regulation and stability under operational no-load conditions. This is an important characteristic for applications where the output current may drop to zero.

Reverse Output-to-Input Voltage Conditions and Protection

Under normal operating conditions, a parasitic diode exists between the output and input of the LDO regulator. The input voltage should always remain greater than the output load voltage maintaining a reverse bias on the internal parasitic

diode. Conditions where V_{OUT} might exceed V_{IN} should be avoided since this would forward bias the internal parasitic diode and allow excessive current flow into the V_{OUT} pin, possibly damaging the LDO regulator.

In applications where there is a possibility of V_{OUT} exceeding V_{IN} for brief amounts of time during normal operation, the use of a larger value C_{IN} capacitor is highly recommended. A larger value of C_{IN} with respect to C_{OUT} will effect a slower C_{IN} decay rate during shutdown, thus preventing V_{OUT} from exceeding V_{IN} . In applications where there is a greater danger of V_{OUT} exceeding V_{IN} for extended periods of time, it is recommended to place a Schottky diode across V_{IN} to V_{OUT} (connecting the cathode to V_{IN} and anode to V_{OUT}). The Schottky diode forward voltage should be less than 0.45 volts.

Thermal Considerations and High Output Current Applications

The AAT3239 is designed to deliver a continuous output load current of 500mA under normal operations. The short-circuit current limit is greater than 500mA, typically active at 600mA.

The limiting characteristics for the maximum output load current safe operating area is essentially package power dissipation, the internal preset thermal limit of the device, and the input-to-output voltage drop across the AAT3239. In order to obtain high operating currents, careful device layout and circuit operating conditions need to be taken into account.

The following discussions will assume the LDO regulator is mounted on a printed circuit board utilizing the minimum recommended footprint as stated in the layout considerations section of this document. At any given ambient temperature (T_A), the maximum package power dissipation can be determined by the following equation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Constants for the AAT3239 are $T_{J(MAX)}$, the maximum junction temperature for the device which is 125°C, and $T_{JA} = 90^\circ\text{C/W}$, the package thermal resistance. Typically, maximum conditions are calculated at the maximum operating temperature of $T_A = 85^\circ\text{C}$ and under normal ambient conditions where $T_A = 25^\circ\text{C}$. Given $T_A = 85^\circ\text{C}$, the maximum package power dissipation is 444mW. At $T_A = 25^\circ\text{C}$, the maximum package power dissipation is 1.11W.

The maximum continuous output current for the AAT3239 is a function of the package power dissipation and the input-to-output voltage drop across the LDO regulator. Refer to the following simple equation:

$$I_{OUT(MAX)} < \frac{P_{D(MAX)}}{V_{IN} - V_{OUT}}$$

For example, if $V_{IN} = 4.2\text{V}$, $V_{OUT} = 1.8\text{V}$, and $T_A = 25^\circ\text{C}$, $I_{OUT(MAX)} < 463\text{mA}$. If the output load current were to exceed 463mA or if the ambient temperature were to increase, the internal die temperature would increase. If the condition remained constant, the LDO regulator thermal protection circuit would activate.

To determine the maximum output current for a given output voltage, refer to the following equation. This calculation accounts for the total power dissipation of the LDO regulator, including that caused by ground current.

$$P_{D(MAX)} = (V_{IN} - V_{OUT})I_{OUT} + (V_{IN} \times I_{GND})$$

This formula can be solved for I_{OUT} to determine the maximum output current.

$$I_{OUT} = \frac{P_{D(MAX)} - (V_{IN} \times I_{GND})}{V_{IN} - V_{OUT}}$$

The following is an example for an AAT3239 set for a 1.5 volt output:

$$V_{OUT} = 1.5V$$

$$V_{IN} = 4.2V$$

$$I_{GND} = 125\mu A$$

$$I_{OUT} = \frac{1.11W - (4.2V \times 125\mu A)}{4.2 - 1.5}$$

$$I_{OUT(MAX)} = 411mA$$

From the discussion above, $P_{D(MAX)}$ was determined to equal 1.11W at $T_A = 25^\circ C$.

Thus, the AAT3239 can sustain a constant 1.5V output at a 411mA load current at an ambient temperature of $25^\circ C$. Higher input-to-output voltage differentials can be obtained with the AAT3239, while maintaining device functions within the thermal safe operating area. To accomplish this, the device thermal resistance must be reduced by increasing the heat sink area or by operating the LDO regulator in a duty-cycled mode.

For example, an application requires $V_{IN} = 4.2V$ while $V_{OUT} = 1.5V$ at a 500mA load and $T_A = 25^\circ C$. V_{IN} is greater than 3.7V, which is the maximum safe

continuous input level for $V_{OUT} = 1.5V$ at 500mA for $T_A = 25^\circ C$. To maintain this high input voltage and output current level, the LDO regulator must be operated in a duty-cycled mode. Refer to the following calculation for duty cycle operation:

$$I_{GND} = 125\mu A$$

$$I_{OUT} = 500mA$$

$$V_{IN} = 4.2V$$

$$V_{OUT} = 1.5V$$

$$\%DC = \frac{100(P_{D(MAX)})}{(V_{IN} - V_{OUT})I_{OUT} + V_{IN} \times I_{GND}}$$

$$\%DC = \frac{100(1.11W)}{(4.2V - 1.5V)500mA + 4.2V \times 125\mu A}$$

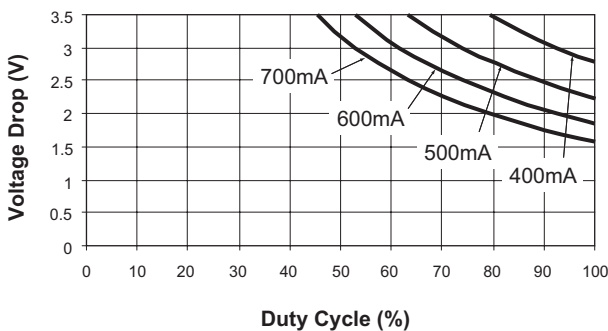
$$\%DC = 82\%$$

$P_{D(MAX)}$ is assumed to be 1.1W

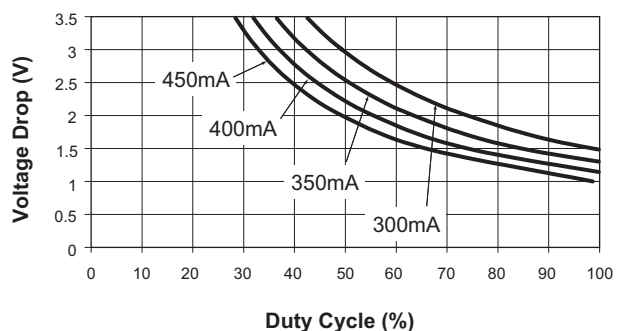
For a 500mA output current and a 2.7V drop across the AAT3239 at an ambient temperature of $25^\circ C$, the maximum on-time duty cycle for the device would be 82%.

The following curves show the safe operating area for duty-cycled operation from ambient room temperature to the maximum operating level.

Device Duty Cycle vs. V_{DROD}
($V_{OUT} = 1.5V @ 25^\circ C$)



Device Duty Cycle vs. V_{DROD}
($V_{OUT} = 1.5V @ 85^\circ C$)



Evaluation Board Layout

The AAT3239 evaluation layout follows the recommend printed circuit board layout procedures and can be used as an example for good application layouts.

Note: Board layout shown is not to scale.

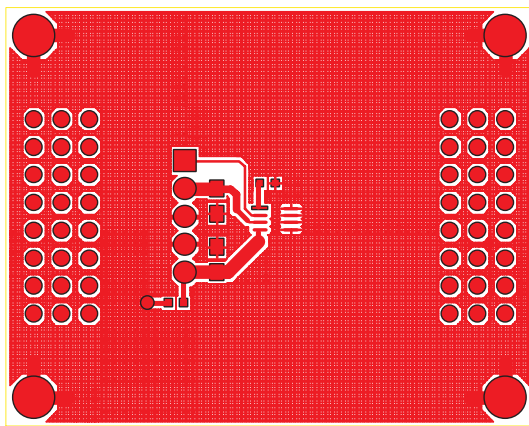


Figure 3: Evaluation Board Component Side Layout.

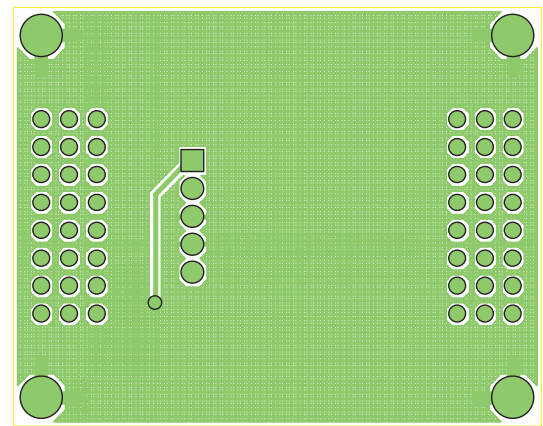


Figure 4: Evaluation Board Solder Side Layout.

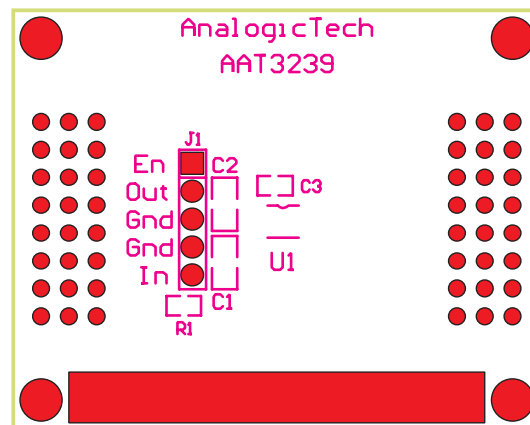


Figure 5: Evaluation Board Top Side Silk Screen Layout/Assembly Drawing.

Ordering Information

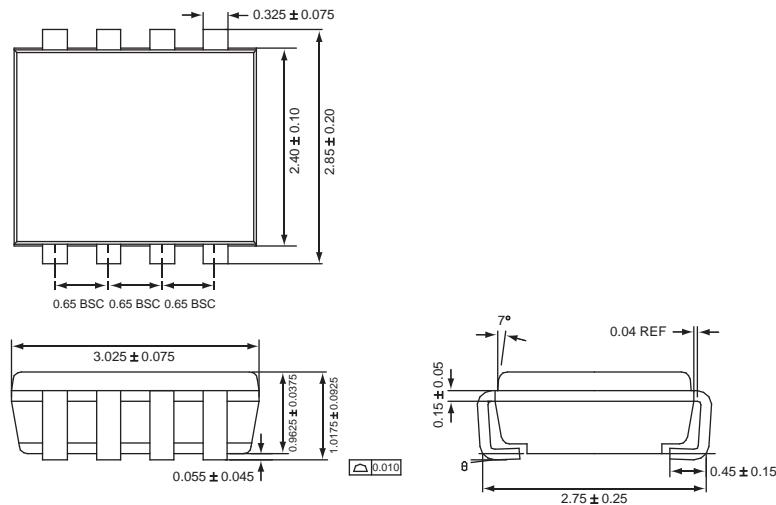
Output Voltage	Package	Marking ¹	Part Number (Tape and Reel) ²
1.5V	TSOPJW-8	JVXYY	AAT3239ITS-1.5-T1
1.8V	TSOPJW-8	NHXYY	AAT3239ITS-1.8-T1
1.85V	TSOPJW-8	JWXYY	AAT3239ITS-1.85-T1
2.5V	TSOPJW-8	QXXYY	AAT3239ITS-2.5-T1
3.3V	TSOPJW-8	MAXYY	AAT3239ITS-3.3-T1



All AnalogicTech products are offered in Pb-free packaging. The term “Pb-free” means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at <http://www.analogictech.com/pbfree>.

Package Information

TSOPJW-8



All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

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