11. ELECTRICAL SPECIFICATIONS

11.1 Absolute Maximum Ratings

Ambient temperature under bias ..... 0°C to 70°C

Storage temperature ..... –65°C to 150°C

Voltage on any pin ..... GND –0.5 V to V_{CC} + 0.5 V

Voltage on any 5 volt tolerant pin ..... GND –0.5 V to 5.5 V

Power supply voltage ..... 5.1 V

Injection current (latch-up testing) ..... 100 mA

CAUTION: Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational ratings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

11.2 DC Specifications (Digital)

(V_{CC} = 3.3 V ± 0.15 V, T_A = 0°C–70°C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Test Conditions
V_{CC} (+3.3V)	Power supply voltage	3.15	3.45	V	Normal operation
V_{IL}	Input low voltage	–0.5	0.3 V_{CC}	V	Not 5-V tolerant
V_{IH}	Input high voltage	0.7 V_{CC}	1.05 V_{CC}	V	Not 5-V tolerant
V_{IH5T}	Input high voltage	0.7 V_{CC}	5.5	V	5-V tolerant[a]
V_{OL}	Output low voltage	–	0.4	V	I_{OL} = 3.2 mA[b]
V_{OH}	Output high voltage	0.9 V_{CC}	–	V	I_{OH} = -200 µA[c]
I_{CC}	Supply current	–	tbd	A	V_{CC} nominal[d]
I_{IH}	Input high current	–	10	µA	$V_{IN} = V_{CC}$
I_{IL}	Input low current	–10	–	µA	V_{CC} = 3.45; V_{IN} = 0
I_{IHP}	Input high current (pull-up)	–10	10	µA	$V_{IN} = V_{CC}$
I_{ILP}	Input low current (pull-up)	–45	12	µA	V_{CC} = 3.45; V_{IN} = 0
I_{OZ}	Input leakage	–10	10	µA	$0 < V_{IN} < V_{CC}$
C_{IN}	Input capacitance	–	10	pF[e]	
C_{OUT}	Output capacitance	–	10	pF[d]	
IREF	DAC current reference	–3	–10	mA	Nominal IREF is –6.67 mA

[a] 5-V tolerant pins — all digital pins except the SGRAM interface.

[b] I_{OL} is specified for a standard buffer. See Chapter 10, “Detailed Pin Descriptions”, for further information.

[c] I_{OH} is specified for a standard buffer. See Chapter 10 for further information.

[d] I_{CC} is measured with VCLK at 157.5 MHz and SMCLK at 100 MHz.

[e] This is not 100% tested, but is periodically sampled.

11.3 DAC Characteristics

Symbol	Parameter	MAX	Units	Test Conditions	Notes
R	Resolution	8	bits		
IO	Output current	30	mA	VO < 1V	
TR	Analog output rise/fall time	3	ns	10% to 90% full scale	a, b
TS	Analog output settling time	15	ns	50% FS to remaining within 2%	a, b
TSK	Analog output skew	tbd	ns		a, b, c, d
FDT	DAC-to-DAC correlation	2.5	%		a, b, c, d
GI	Glitch impulse	tbd	pV/sec		b
IL	Integral linearity	1.5	LSB		
DL	Differential linearity	1.5	LSB		b

a Load is 50 W and 30 pF per analog output.

b IREF = –6.67mA.

c Outputs loaded identically.

d About the mid-point of the distribution of the three DACs measured at full-scale output.

11.4 AC Specifications

Table 11-1. PCI Bus Timing

Symbol	Parameter	MIN	MAX	Units
t_1	PCICLK period	30	–	ns
t_2	High period (CLK) PCI bus	40	60	% t_1
t_3	PCICLK to signal valid delay – bussed signals	2	11	ns
t_3	PCICLK to signal valid delay – point to point	2	12	ns
t_4	PCICLK to active delay	2		ns
t_5	PCICLK to float delay	7		ns
t_6	Input setup time to PCICLK – bussed signals	7		ns
t_6	Input setup time to PCICLK – GNT#	10		ns
t_7	Input hold time from PCICLK	0		ns

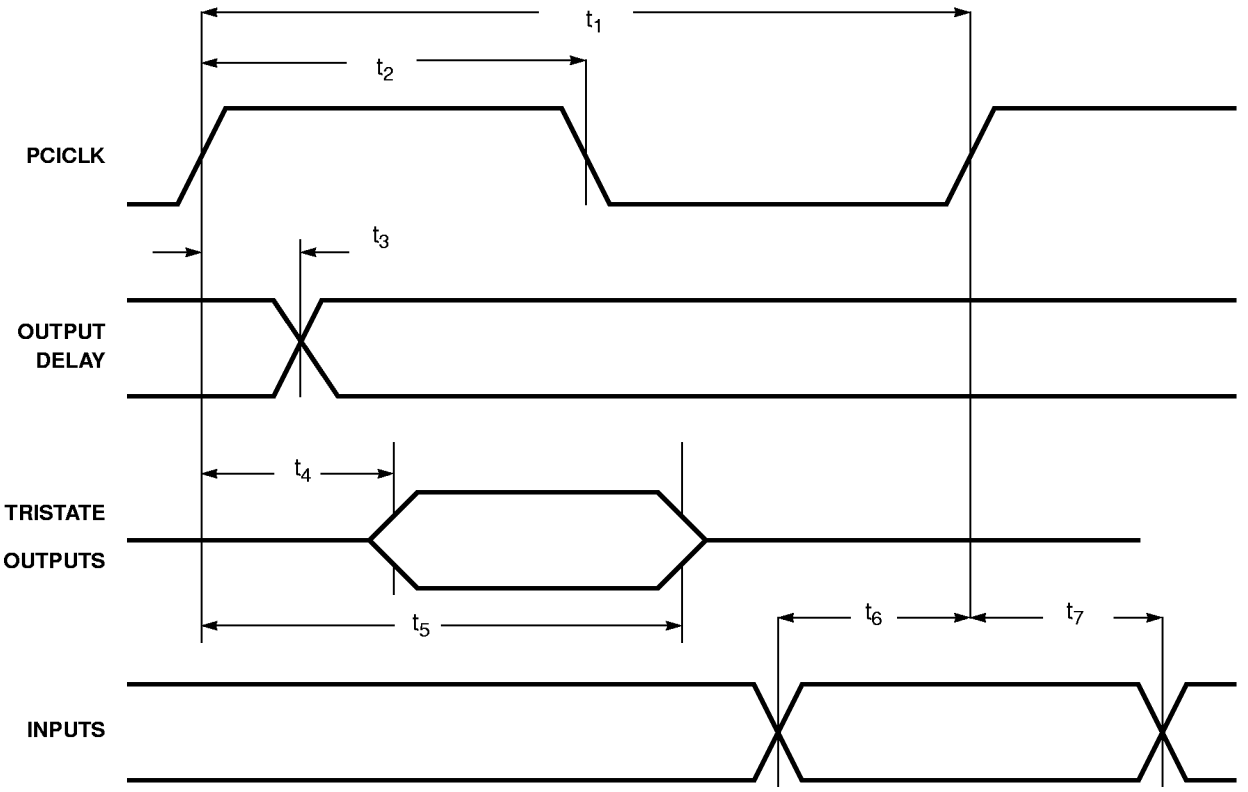
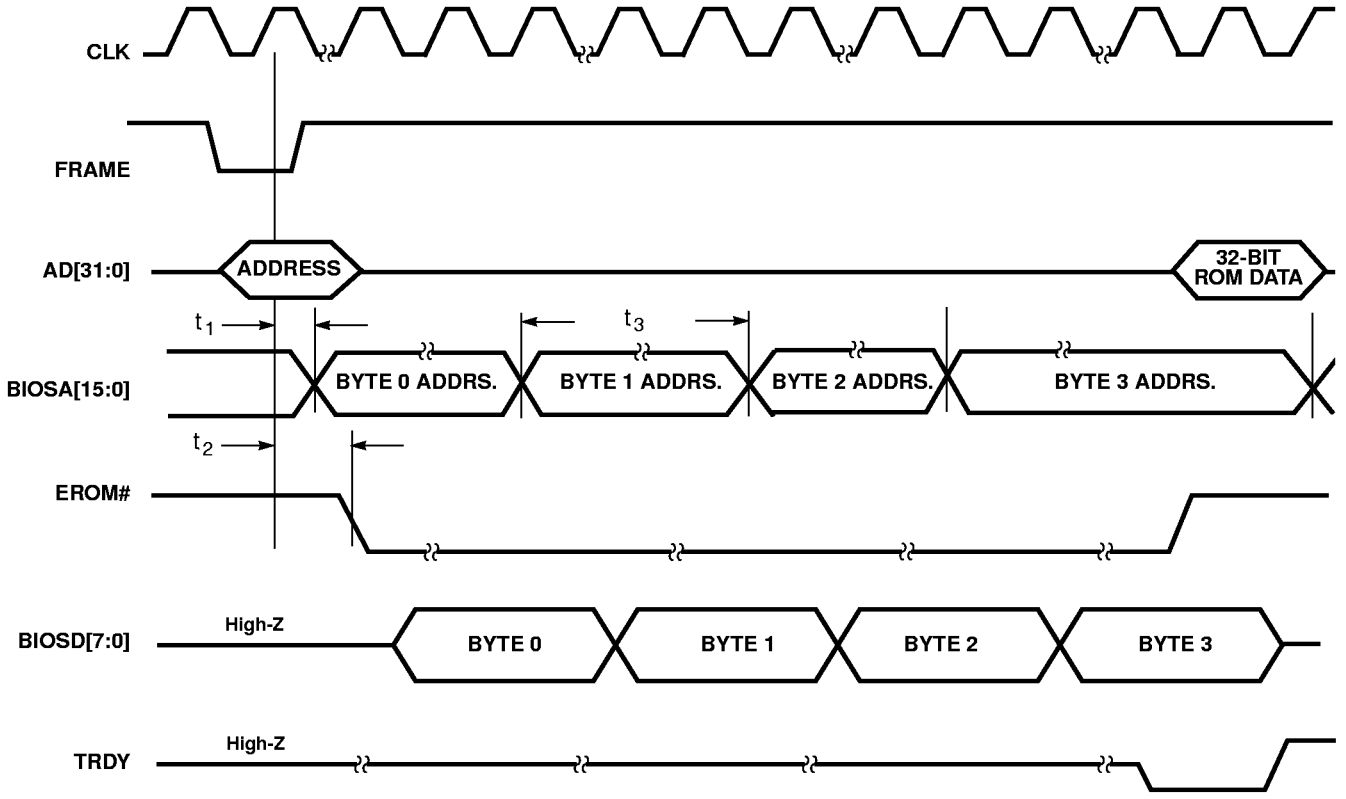


Figure 11-1. PCI Bus Timing

Table 11-2. EROM#, BIOSA[15:0] Timing (PCI Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	BIOSA[15:0] delay from PCICLK	–	15	ns
t_2	EROM# delay from PCICLK	–	15	ns
t_3	Access time	8	–	PCICLK



High-Z = High impedance

Figure 11-2. EROM#, BIOSA[15:0] Timing (PCI Bus)

Table 11-3. SGRAM Timing: Preliminary (Subject to Characterization)

Symbol	Parameter	MIN	MAX	Units
t_1	SMCLK period	10	–	ns
t_2	SMCLK high/low period	35	65	% t_1
t_2	SMCLK to output valid: MD, all controls	2	6	ns
t_3	SMCLK to output valid: MD[63:0]	n/a[a]	n/a	ns
t_4	MD[63:0] output active delay	–	n/a	ns
t_5	MD[63:0] output float delay	–	n/a	ns
t_6	MD[63:0] input setup time to SMCLK	1	–	ns
t_7	MD[63:0] input hold time from SMCLK	3	–	ns

[a] 'n/a' indicates data not available at time of print. Contact Cirrus Logic for up to date information.

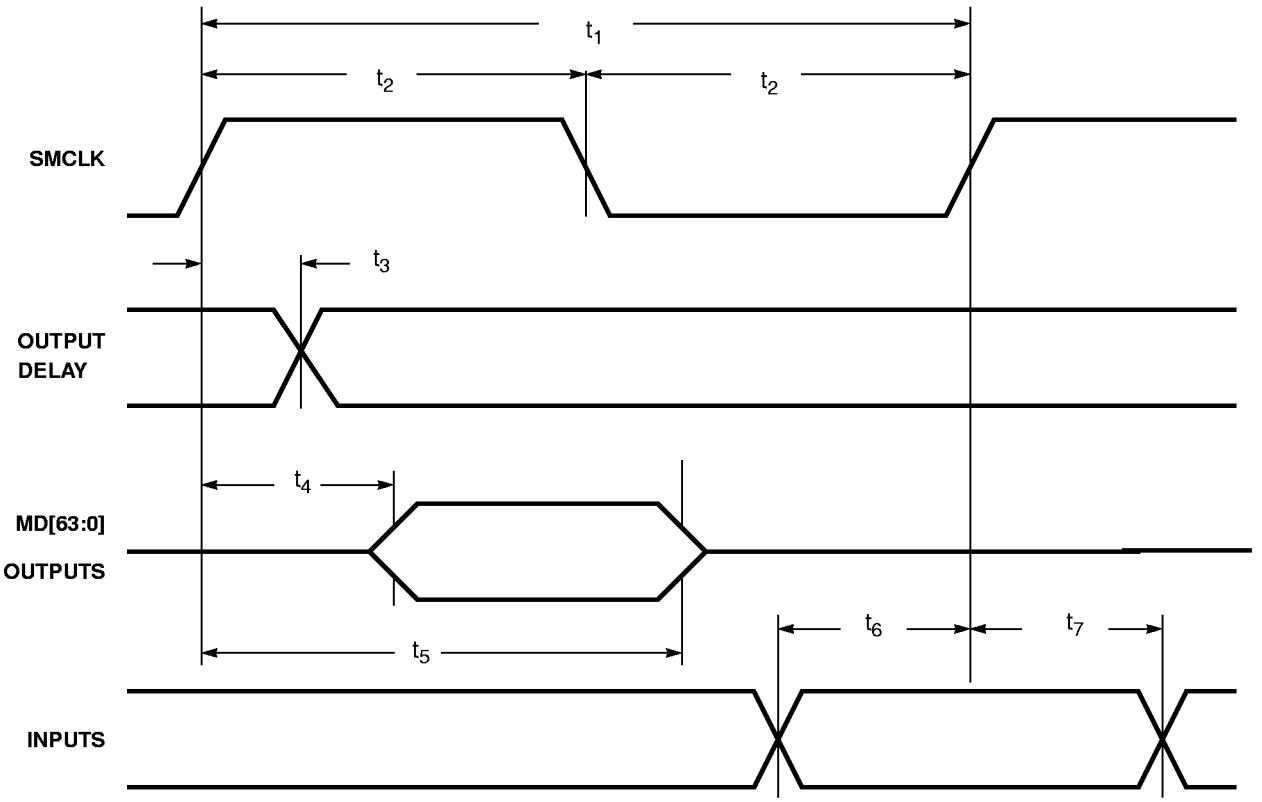


Figure 11-3. SGRAM Timing

Table 11-4. P-Bus as Inputs (External[a] DCLK)

Symbol	Parameter	MIN	MAX	Units
t_1	P[7:0], BLANK# setup to DCLK	0	–	ns
t_2	P[7:0], BLANK# hold from DCLK	6	–	ns

[a] The CL-GD5480 RAMDAC is driven externally.

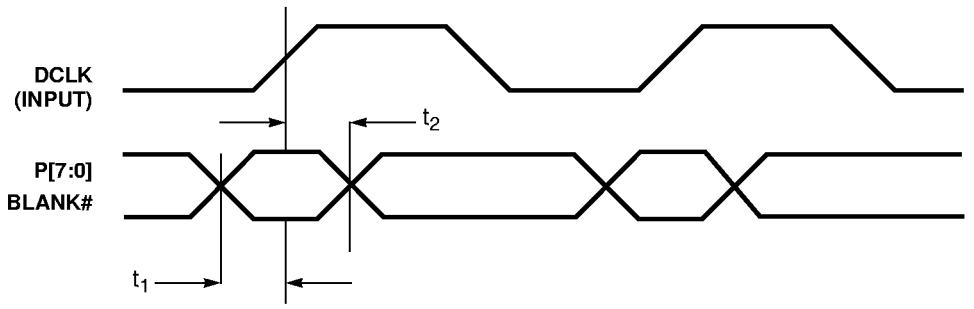


Figure 11-4. P-Bus as Inputs (External DCLK)

Table 11-5. Feature Bus Timing – Output (Internal DCLK)

Symbol	Parameter	MIN	MAX	Units
t_1	DCLK to BLANK# delay	–1	1	ns
t_2	DCLK to HSYNC, VSYNC delay	1	3	ns
t_3	DCLK to P[7:0] delay	–2	0	ns

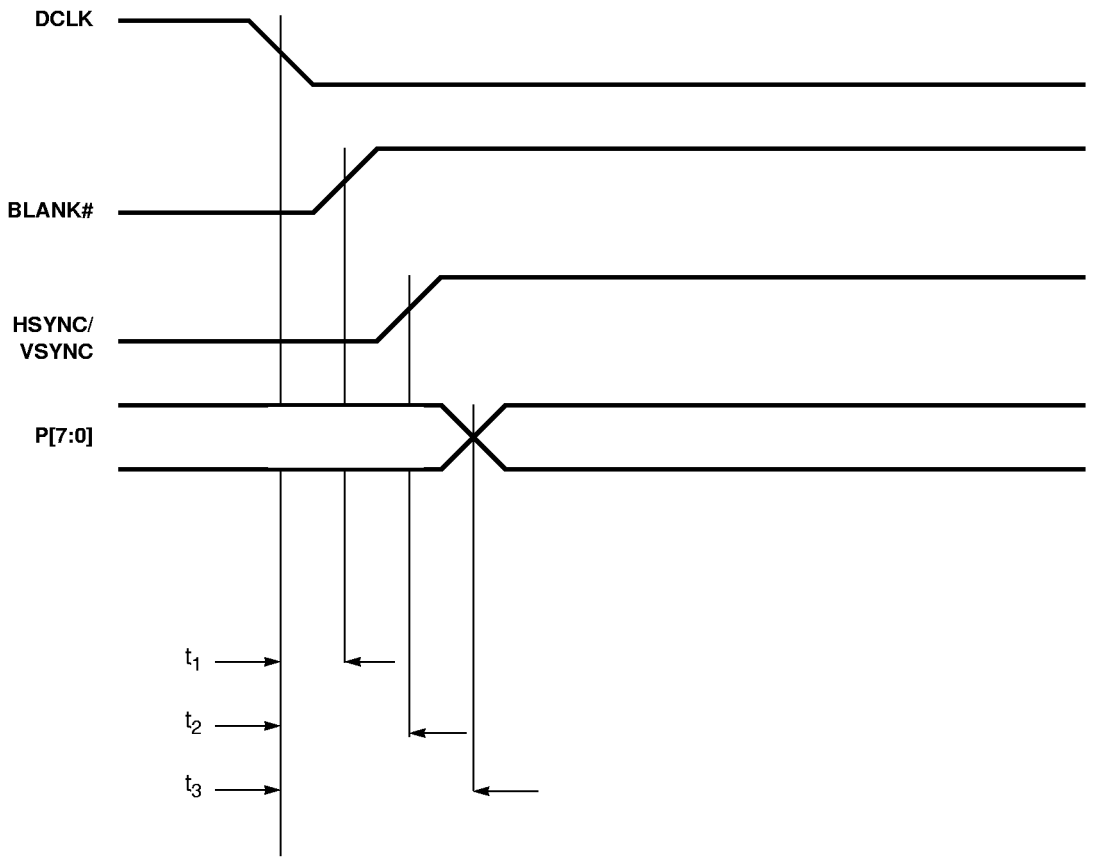


Figure 11-5. Feature Bus Timing – Output (Internal DCLK)

Table 11-6. V-Port™ – PIXCLK Timing

Symbol	Parameter	MIN	MAX	Units
t_1	PIXD[15:0], VACK setup to PIXCLK edge[a]	tbd	–	ns
t_2	PIXD[15:0], VACK hold from PIXCLK edge	tbd	–	ns

[a] PIXD and VACT can be clocked on either or both PIXCLK edges, according to the programming of CR50[5,3].

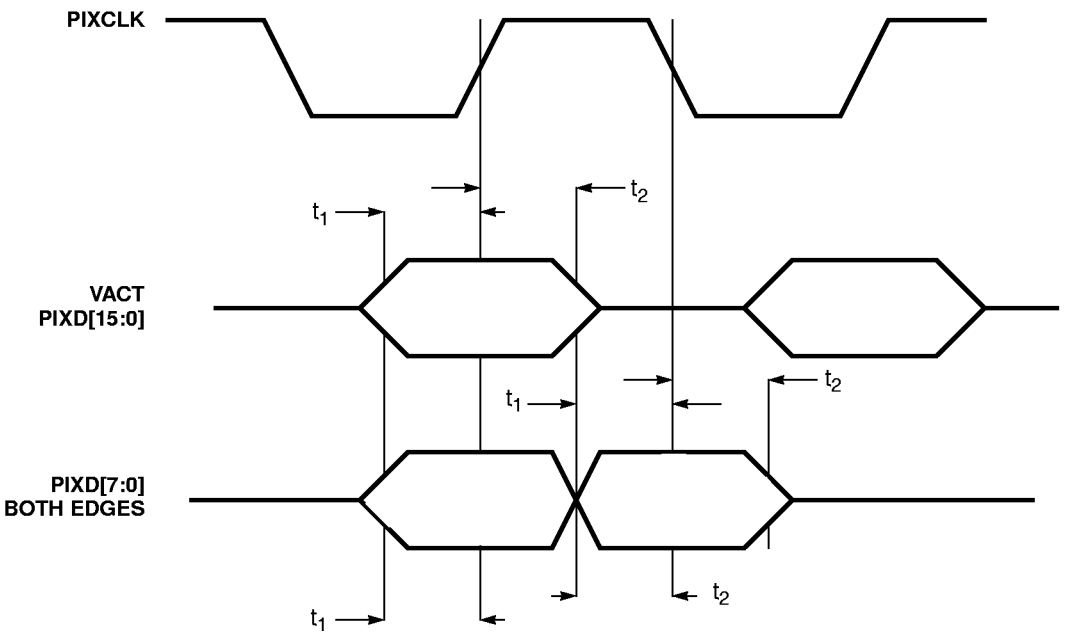


Figure 11-6. V-Port™ – PIXCLK Timing

Table 11-7. V-Port™ Timing – VREF[a]

Symbol	Parameter	MIN	MAX	Units

[a] The terms odd and even are for reference only. The sense can be inverted with CR58[6].

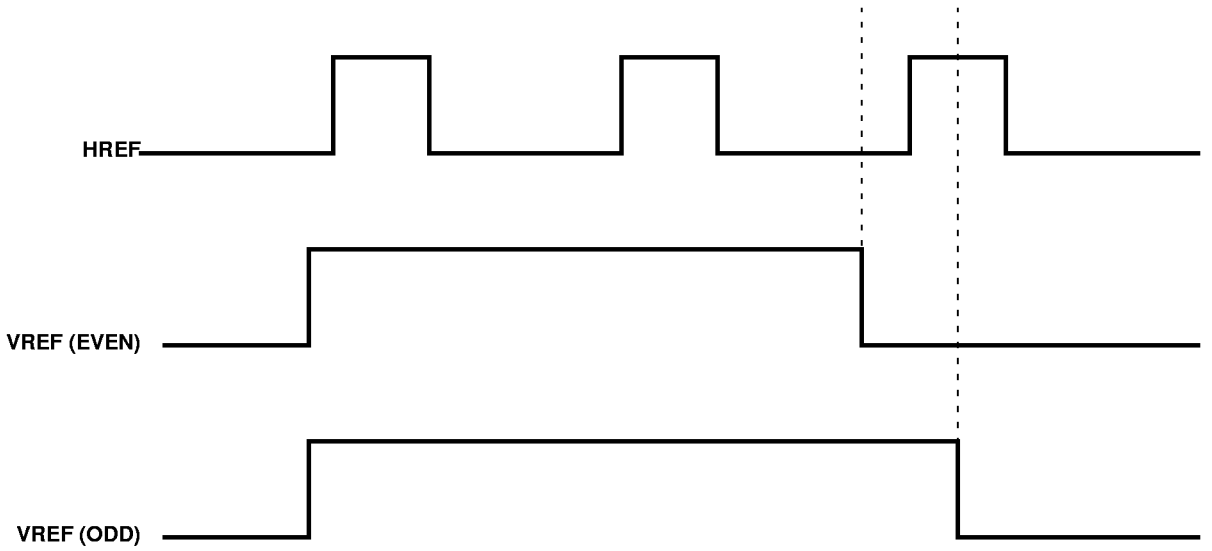


Figure 11-7. V-Port™ Timing – VREF

Table 11-8. Reset Timing

Symbol	Parameter	MIN	MAX	Units
t_1	RST# pulse width	12	–	MCLK
t_2	GPIOD[6:0] setup to RST# rising edge	2	–	ns
t_3	GPIOD[6:0] hold from RST# rising edge	25	–	ns
t_4	RST# inactive to first command	12	–	MCLK

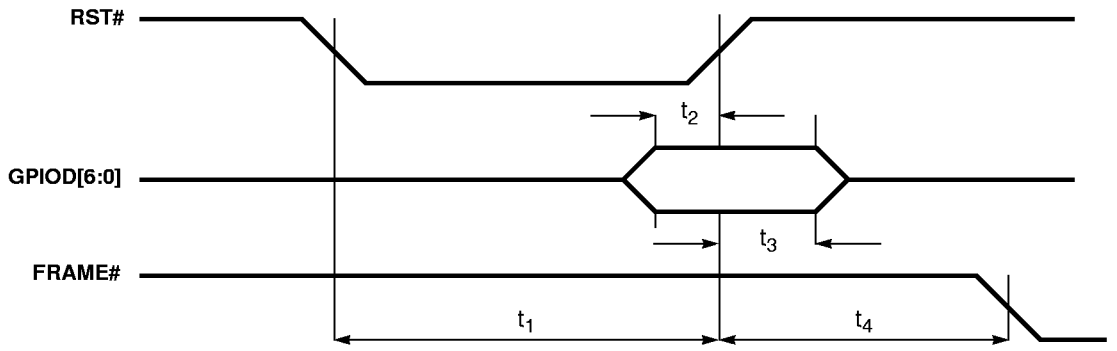


Figure 11-8. Reset Timing