

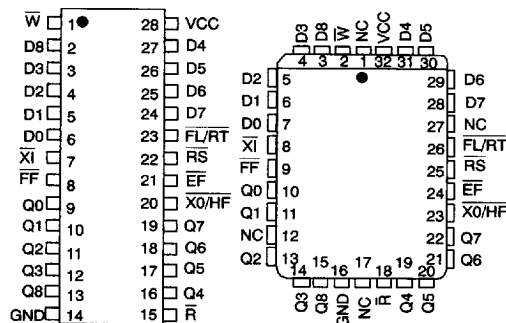
FEATURES

- First-in, first-out memory-based architecture
- Flexible 2048 x 9 organization
- Low-power HCMOS technology
- Asynchronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- High performance
- Available in 50 ns, 65 ns, 80 ns, and 120 ns access times
- Optional industrial temperature range -40°C to +85°C available, designated N

DESCRIPTION

The DS2011 FIFO Chip implements a first-in, first-out algorithm featuring asynchronous read/write operations, full, empty, and half-full flags, and unlimited expansion capability in both word size and depth. The DS2011 is functionally and electrically equivalent to the

PIN ASSIGNMENT



28-Pin DIP
(300 and 600 Mil)
See Mech. Drawings
Figs. 964 & 966

32-Pin PLCC
See Mech. Drawing
Pg. 979

PIN DESCRIPTION

W	– WRITE
R	– READ
RS	– RESET
FL/RT	– First Load/Retransmit
D ₀₋₈	– Data In
Q ₀₋₈	– Data Out
XI	– Expansion In
XO/HF	– Expansion Out/Half Full
FF	– Full Flag
EF	– Empty Flag
VCC	– 5 Volts
GND	– Ground
NC	– No Connect

DS2009 512 x 9 FIFO Chip, with the exceptions listed in the notes for DC Electrical Characteristics of the DS2009 data sheet. Refer to the DS2009 data sheet for detailed device description.