HD-4702

March 1997

CMOS Programmable Bit Rate Generator

Features

- **HD-4702 Provides 13 Commonly Used Bit Rates**
- **Uses a 2.4576MHz Crystal/Input for Standard Frequency Output (16 Times Bit Rate)**
- **Low Power Dissipation**
- **Conforms to EIA RS-404**
- **One HD-4702 Controls up to Eight Transmission Channels**
- **Initialization Circuit Facilitates Diagnostic Fault Isolation**
- **On-Chip Input Pull-Up Circuit**

Ordering Information

PACKAGE	TEMP. RANGE (^{o}C)	PART NUMBER	PKG. NO.
PDIP	-40 to +85	HD3-4702-9	E16.3
CERDIP	-40 to +85	HD1-4702-9	F16.3
SMD#	-55 to +125	5962-9051801MEA	F16.3

Description

The HD-4702 Bit Rate Generator provides the necessary clock signals for digital data transmission systems, such as a UART. It generates 13 commonly used bit rates using an on-chip crystal oscillator or an external input. For conventional operation generating 16 output clock pulses per bit period, the input clock frequency must be 2.4576MHz (i.e. 9600 Baud x 16 x 16, since there is an internal ÷ 16 prescaler). A lower input frequency will result in a proportionally lower output frequency.

The HD-4702 can provide multi-channel operation with a minimum of external logic by having the clock frequency CO and the ÷ 8 prescaler outputs Q0, Q1, Q2 available externally. All signals have a 50% duty cycle except 1800 Baud, which has less than 0.39% distortion.

The four rate select inputs (S0-S3) select which bit rate is at the output (Z). See Truth Table for Rate Select Inputs for select code and output bit rate. Two of the 16 select codes for the HD-4702 do not select an internally generated frequency, but select an input into which the user can feed either a different frequency, or a static level (High or Low) to generate “ZERO BAUD”.

The bit rates most commonly used in modern data terminals (110, 150, 300, 1200, 2400 Baud) require that no more than one input be grounded for the HD-4702, which is easily achieved with a single 5-position switch.

The HD-4702 has an initialization circuit which generates a master reset for the scan counter. This signal is derived from a digital differentiator that senses the first high level on the CP input after the $\overline{E}_{CP}$ input goes low. When $\overline{E}_{CP}$ is high, selecting the crystal input, CP must be low. A high level on CP would apply a continuous reset. See Clock Modes and Initialization below.

Truth Table

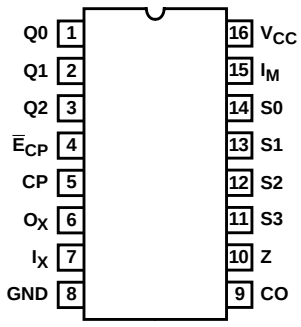
TRUTH TABLE FOR RATE SELECT INPUTS
(Using 2.4576MHz Crystal)

S3	S2	S1	S0	OUTPUT RATE (Z)
L	L	L	L	MUX Input (IM)
L	L	L	H	MUX Input (IM)
L	L	H	L	50 Baud
L	L	H	H	75 Baud
L	H	L	L	134.5 Baud
L	H	L	H	200 Baud
L	H	H	L	600 Baud
L	H	H	H	2400 Baud
H	L	L	L	9600 Baud
H	L	L	H	4800 Baud
H	L	H	L	1800 Baud
H	L	H	H	1200 Baud
H	H	L	L	2400 Baud
H	H	L	H	300 Baud
H	H	H	L	150 Baud
H	H	H	H	110 Baud

NOTE: 19200 Baud by connecting Q2 to IM.

Pinout

HD-4702 (CERDIP, PDIP)
TOP VIEW



Pin Description

PIN NUMBER	TYPE	SYMBOL	DESCRIPTION
16		V_{CC}	V_{CC}: Is the +5V power supply pin. A 0.1µF capacitor between pins 16 and 8 is recommended for decoupling.
8		GND	GROUND
5	I	CP	EXTERNAL CLOCK INPUT
4	I	$\overline{E}_{CP}$	EXTERNAL CLOCK ENABLE: A low signal on this input allows the baud rate to be generated from the CP input.
7	I	I_X	CRYSTAL INPUT
6	O	O_X	CRYSTAL DRIVE OUTPUT
15	I	I_M	MULTIPLEXED INPUT
11, 12, 13, 14	I	S0 - S3	BAUD RATE SELECT INPUTS
9	O	CO	CLOCK OUTPUT
1, 2, 3	O	Q_0 - Q_2	SCAN COUNTER OUTPUTS
10	O	Z	BIT RATE OUTPUT

CLOCK MODES AND INITIALIZATION

IX	$\overline{E}_{CP}$	CP	OPERATION
	H	L	Clocked from I_X
X	L		Clocked from CP
X	H	H	Continuous Reset
X	L		Reset During 1st CP = High Time

H = HIGH Level

L = LOW Level

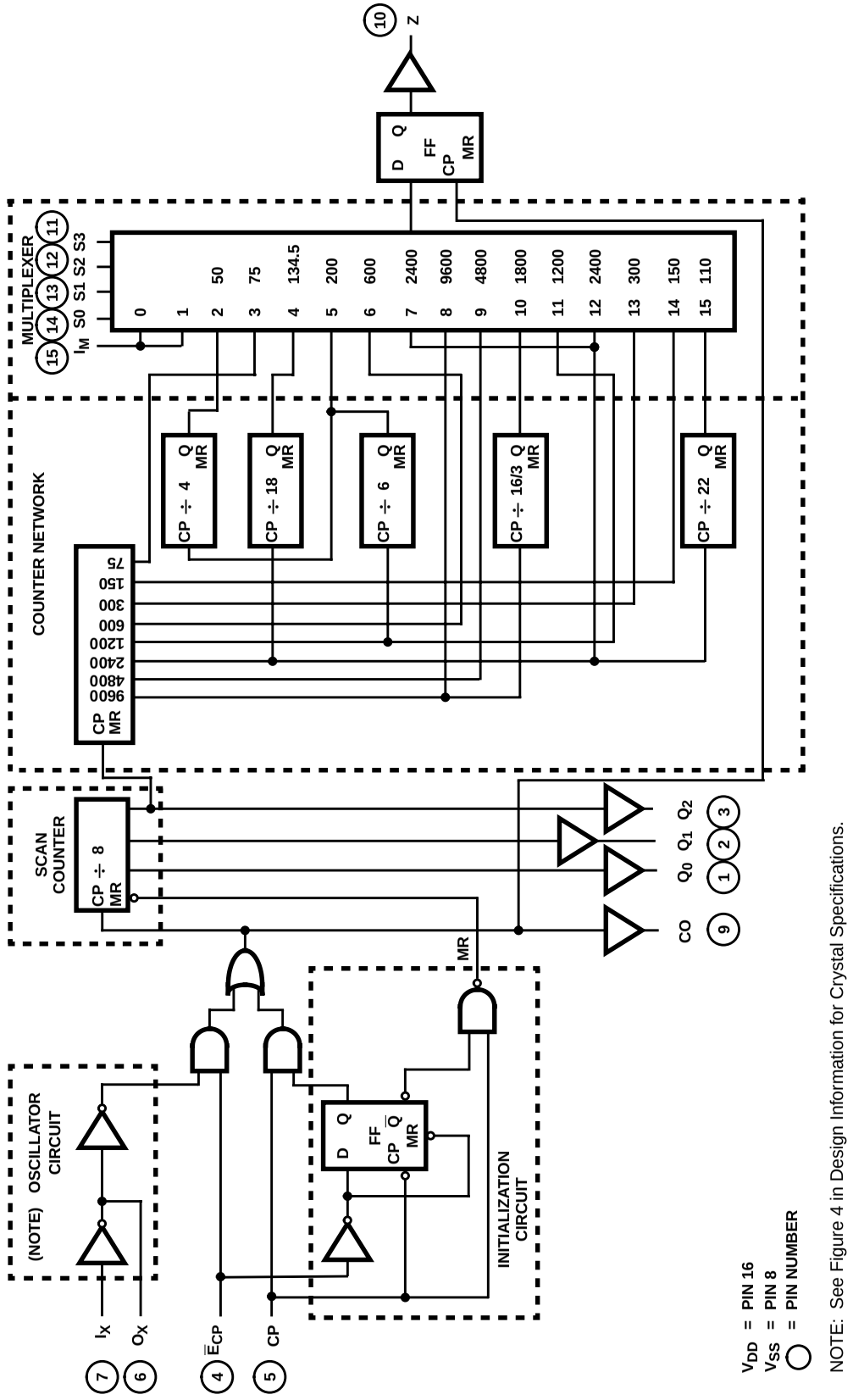
X = Don't Care

 = Clock Pulse

 = 1st HIGH Level Clock Pulse after $\overline{E}_{CP}$ goes LOW

NOTE: Actual output frequency is 16 times the indicated Output Rate, assuming a clock frequency of 2.4576MHz.

Block Diagram

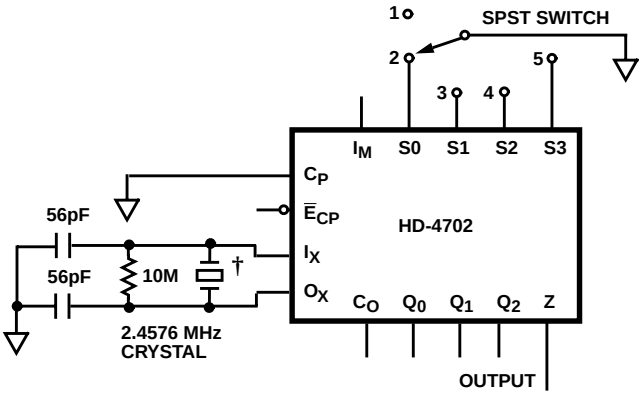


NOTE: See Figure 4 in Design Information for Crystal Specifications.

Application Information

Single Channel Bit Rate Generator

Figure 1 shows the simplest application of the HD-4702. This circuit generates one of five possible bit rates as determined by the setting of a single pole, 5-position switch. The Bit Rate Output (Z) drives one standard TTL load or four low power Schottky loads over the full temperature range. The possible output frequencies correspond to 110, 150, 300, 1200, and 2400 Baud. For many low cost terminals, these five bit rates are adequate.



† See Table 1.

SWITCH POSITION	HD-4702 BIT RATE
1	110 Baud
2	150 Baud
3	300 Baud
4	1200 Baud
5	2400 Baud

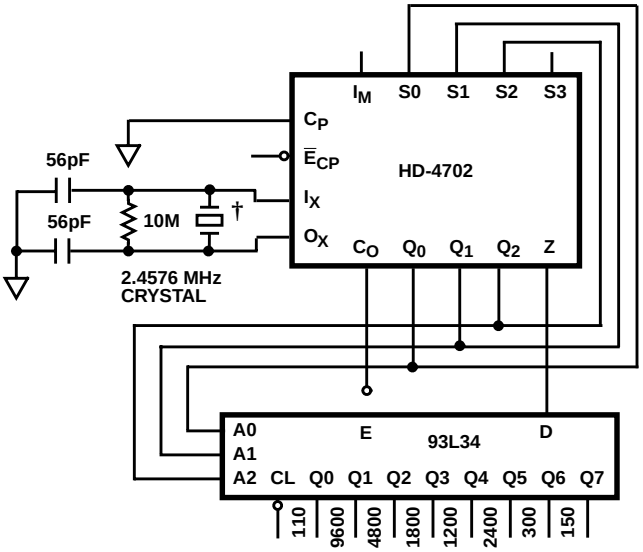
FIGURE 1. SWITCH SELECTABLE BIT RATE GENERATOR CONFIGURATION PROVIDING FIVE BIT RATES

Simultaneous Generation of Several Bit Rates

Figure 2 shows a simple scheme that generates eight bit rates on eight output lines, using one HD-4702 and one 93L34 Bit Addressable Latch. This and the following applications take advantage of the built-in scan counter (prescaler) outputs. As shown in the block diagram, these outputs (Q_0 to Q_2) go through a complete sequence of eight states for every half-period of the highest output frequency (9600 Baud). Feeding these Scan Counter Outputs back to the Select Inputs of the multiplexer causes the HD-4702 to interrogate sequentially eight different frequency signals. The 93L34 8-bit addressable Latch, addressed by the same Scan Counter Outputs, re-converts the multiplexed single Output (Z) of the HD-4702 into eight parallel output frequency signals. In the simple scheme of Figure 2, input S3 is left open (HIGH) and the following bit rates are generated:

Q0: 110 Baud Q1: 9600 Baud Q2: 4800 Baud
Q3: 1800 Baud Q4: 1200 Baud Q5: 2400 Baud
Q6: 300 Baud Q7: 150 Baud

Other bit rate combinations can be generated by changing the Scan Counter to Selector interconnection or by inserting logic gates into this path.

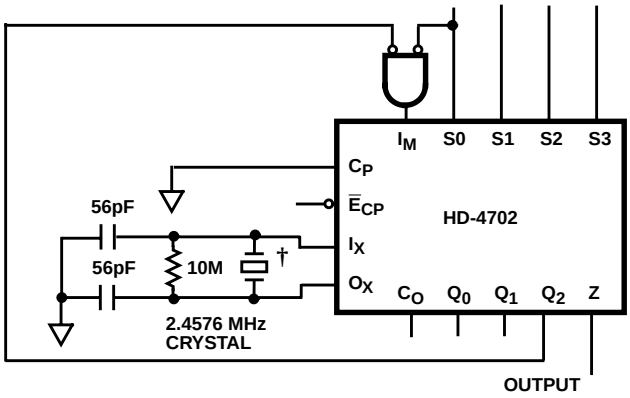


† See Table 1.

FIGURE 2. BIT RATE GENERATOR CONFIGURATION WITH EIGHT SIMULTANEOUS FREQUENCIES

19200 Baud Operation

Though a 19200 Baud signal is not internally routed to the multiplexer, the HD-4702 can be used to generate this bit rate by connecting the Q_2 output to IM input and applying select code. An additional 2-input NOR gate can be used to retain the "Zero Baud" feature on select code 1 for the HD-4702 (See Figure 3).



† See Table 1.

FIGURE 3. 19200 BAUD OPERATION

TABLE 1. CRYSTAL SPECIFICATIONS

PARAMETERS	TYPICAL CRYSTAL SPEC
Frequency	2.4576MHz "AT" Cut
Series Resistance (Max)	250
Unwanted Modes	-6.0dB (Min)
Type of Operation	Parallel
Load Capacitance	32pF +0.5

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1
Typical Derating Factor . . . . . 1mA/MHz Increase in ICCOP

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
CERDIP Package	$78^oC/W$	$23^oC/W$
PDIP Package	$90^oC/W$	N/A

Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Junction Temperature . . . . .
Ceramic Package . . . . . $+175^oC$
Plastic Package . . . . . $+150^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $+300^oC$

Die Characteristics

Gate Count . . . . . 720 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V

Operating Temperature Range
HD-4702-9 . . . . . -40^oC to $+85^oC$
HD-4702-8 . . . . . -55^oC to $+125^oC$

DC Electrical Specifications

V_{CC} = 5V ±10%, T_A = -40^oC to $+85^oC$ (HD-4702-9), T_A = -55^oC to $+125^oC$ (HD-4702-8)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input High Voltage	V_{CC} 70%	-	V	V_{CC} = 4.5V
V_{IL}	Input Low Voltage	-	V_{CC} 30%	V	V_{CC} = 4.5V
V_{OH1}	Output High Voltage	V_{CC} -0.1	-	V	$I_{OH} \le -1\mu A$, V_{CC} = 4.5V, (Note 1)
V_{OL1}	Output Low Voltage	-	0.1	V	$I_{OL} \le +1\mu A$, V_{CC} = 4.5V, (Note 1)
I_{IH}	Input High Current	-1	+1	µA	$V_{IN} = V_{CC}$, All 0ther Pins = 0V, V_{CC} = 5.5V
I_{ILX}	Input Low Current (I_X Input)	-1	+1	µA	V_{IN} = 0V, All Other Pins = V_{CC}, V_{CC} = 5.5V
I_{IL}	Input Low Current (All Other Inputs)	-	-100	µA	V_{IN} = 0V, All Other Pins = V_{CC}, V_{CC} = 5.5V (Note 2)
I_{OHX}	Output High Current (O_X)	-0.1	-	mA	$V_{OUT} = V_{CC}$ - 0.5, V_{CC} = 4.5V, Input at 0V or V_{CC} per Logic Function or Truth Table
I_{OH1}	Output High Current (All Other Outputs)	-1.0	-	mA	V_{OUT} = 2.5V, V_{CC} = 4.5V, Input at 0V or V_{CC} per Logic Function or Truth Table
I_{OH2}	Output High Current (All Other Outputs)	-0.3	-	mA	$V_{OUT} = V_{CC}$ -0.5, V_{CC} = 4.5V, Input at 0V or V_{CC} per Logic Function or Truth Table
I_{OLX}	Output Low Current (O_X)	0.1	-	mA	V_{OUT} = 0.4V, V_{CC} = 4.5V, Input at 0V or V_{CC} per Logic Function or Truth Table
I_{OL}	Output Low Current (All Other Outputs)	1.6	-	mA	V_{OUT} = 0.4V, V_{CC} = 4.5V Input, at 0V or V_{CC} per Logic Function or Truth Table
I_{CC}	Supply Current (Static)	-	1500	µA	$\overline{E}_{CP} = V_{CC}$, CP = 0V, V_{CC} = 5.5V, All Other Inputs = GND, (Note 2)
		-	1000	µA	$\overline{E}_{CP} = V_{CC}$, CP = 0V, V_{CC} = 5.5V, All Other Inputs = V_{CC}, (Note 2)

NOTES:

1. Interchanging of force and sense conditions is permitted.
2. Input Current and Quiescent Power Supply Current are relatively higher for this device because of active pull-up circuits on all inputs except I_X.

AC Electrical Specifications V_{CC} = 5V ±10%, T_A = -40°C to +85°C (HD-4702-9), T_A = -55°C to +125°C (HD-4702-8)

SYMBOL	AC PARAMETER	LIMITS		UNITS	TEST CONDITIONS
		MIN	MAX		
t_{PLH}	Propagation Delay, I_X to CO	-	350	ns	V_{CC} = 4.5V $C_L \leq$ 7pF on O_X C_L = 50pF (Note 1)
t_{PHL}		-	275	ns	
t_{PLH}	Propagation Delay, CP to CO	-	260	ns	
t_{PHL}		-	220	ns	
t_{PLH}	Propagation Delay, CO to Qn	-	(Note 2)	ns	
t_{PHL}		-	(Note 2)	ns	
t_{PLH}	Propagation Delay, CO to Z	-	85	ns	
t_{PHL}		-	75	ns	
t_{TLH}	Output Transition Time (Except O_X)	-	160	ns	
t_{THL}		-	75	ns	
t_S	Set-Up Time, Select to CO	350	-	ns	
t_h	Hold Time, Select to CO	0	-	ns	
t_S	Set-Up Time, I_M to CO	350	-	ns	
t_h	Hold Time, I_M to CO	0	-	ns	
t_{wCP}(L)	Minimum Clock Pulse Width, Low (Notes 3, 4)	120	-	ns	
t_{wCP}(H)	Minimum Clock Pulse Width, High (Notes 3, 4)	120	-	ns	
t_{wCP}(L)	Minimum I_X Pulse Width, Low (Note 4)	160	-	ns	
t_{wCP}(H)	Minimum I_X Pulse Width, High (Note 4)	160	-	ns	
t_{PLH}	Propagation Delay I_X to CO	-	300	ns	V_{CC} = 4.5V $C_L \leq$ 7pF on O_X C_L = 15pF (Note 1)
t_{PHL}		-	250	ns	
t_{PLH}	Propagation Delay CP to CO	-	215	ns	
t_{PHL}		-	195	ns	
t_{PLH}	Propagation Delay CO to Qn	-	(Note 2)	ns	
t_{PHL}		-	(Note 2)	ns	
t_{PLH}	Propagation Delay CO to Z	-	75	ns	
t_{PHL}		-	65	ns	
t_{TLH}	Output Transition Time (Except O_X)	-	80	ns	
t_{THL}		-	40	ns	

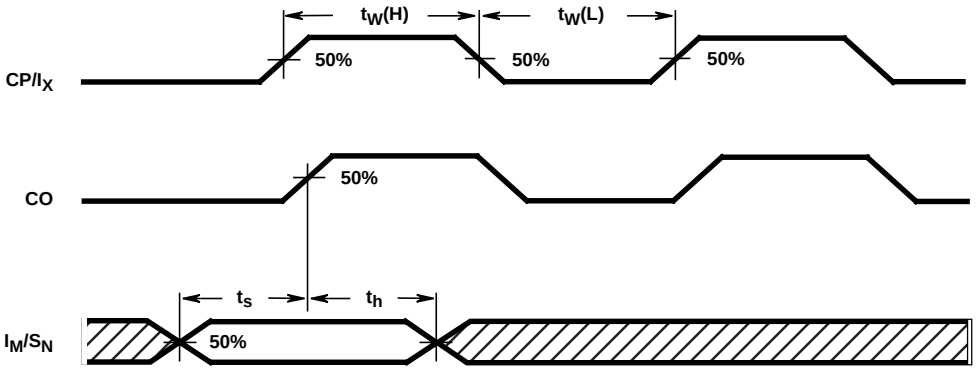
NOTES:

1. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Setup Times (t_S), Hold Times (t_h), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
2. For multichannel operation, Propagation Delay (CO to Qn) plus Set-Up Time, Select to CO, is guaranteed to be ≤ 367ns.
3. The first High Level Clock Pulse after $\overline{E}_{CP}$ goes Low must be at least 350ns long to guarantee reset of all Counters.
4. It is recommended that input rise and fall times to the clock inputs (CP, I_X) be less than 15ns.

Capacitance $T_A = +25^oC$; Frequency = 1MHz

SYMBOL	PARAMETER	TYPICAL	UNITS	CONDITIONS
C_{IN}	Input Capacitance	7	pF	All measurements are referenced the device GND
C_{OUT}	Output Capacitance	15	pF	

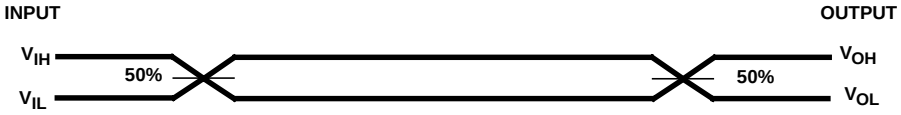
Switching Waveforms



NOTE:

1. Setup and Hold times are shown as positive values but may be specified as negative values.

AC Testing Input, Output Waveform



NOTE:

1. AC Testing: All input signals must switch between V_{IL} and V_{IH}. Input rise and fall times are driven at 1ns per volt.

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