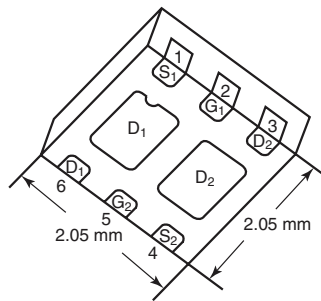


N- and P-Channel 12-V (D-S) MOSFET

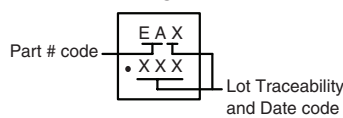
PRODUCT SUMMARY

	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
N-Channel	12	0.040 at V _{GS} = 4.5 V	4.5 ^a	4.5 nC
		0.048 at V _{GS} = 2.5 V	4.5 ^a	
		0.063 at V _{GS} = 1.8 V	4.5 ^a	
P-Channel	- 12	0.070 at V _{GS} = - 4.5 V	- 4.5 ^a	5 nC
		0.100 at V _{GS} = - 2.5 V	- 4.5 ^a	
		0.140 at V _{GS} = - 1.8 V	- 4.5 ^a	

PowerPAK SC-70-6 Dual



Marking Code



FEATURES

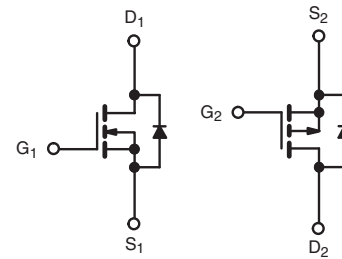
- Halogen-free
- TrenchFET® Power MOSFETs
- New Thermally Enhanced PowerPAK® SC-70 Package
 - Small Footprint Area
 - Low On-Resistance



RoHS
COMPLIANT

APPLICATIONS

- Load Switch for Portable Devices



Ordering Information: SiA511DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V _{DS}	12	- 12	V
Gate-Source Voltage		V _{GS}	± 8		
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	4.5 ^a	- 4.5 ^a	A
	T _C = 70 °C		4.5 ^a	- 4.5 ^a	
	T _A = 25 °C		4.5 ^{a, b, c}	- 4.3 ^{b, c}	
	T _A = 70 °C		4.5 ^{a, b, c}	- 3.4 ^{b, c}	
Pulsed Drain Current		I _{DM}	20	- 10	
Source Drain Current Diode Current	T _C = 25 °C	I _S	4.5 ^a	- 4.5 ^a	
	T _A = 25 °C		1.6 ^{b, c}	- 1.6 ^{b, c}	
Maximum Power Dissipation	T _C = 25 °C	P _D	6.5	6.5	W
	T _C = 70 °C		5	5	
	T _A = 25 °C		1.9 ^{b, c}	1.9 ^{b, c}	
	T _A = 70 °C		1.2 ^{b, c}	1.2 ^{b, c}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{d, e}			260		

THERMAL RESISTANCE RATINGS

Parameter		Symbol	N-Channel		P-Channel		Unit
			Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	52	65	52	65	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	12.5	16	12.5	16	

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 5 s.

d. See Solder Profile (<http://www.vishay.com/ppg73257>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 110 °C/W.

SPECIFICATIONS T _J = 25 °C, unless otherwise noted								
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit	
Static								
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	N-Ch	12			V	
		V _{GS} = 0 V, I _D = - 250 μA	P-Ch	- 12				
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	N-Ch		12		mV/°C	
		I _D = - 250 μA	P-Ch		- 7			
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	N-Ch		- 2.8			
		I _D = - 250 μA	P-Ch		2.1			
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.4		1	V	
		V _{DS} = V _{GS} , I _D = - 250 μA	P-Ch	- 0.4		- 1		
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V	N-Ch P-Ch			± 100 ± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 12 V, V _{GS} = 0 V	N-Ch			1	μA	
		V _{DS} = - 12 V, V _{GS} = 0 V	P-Ch			- 1		
		V _{DS} = 12 V, V _{GS} = 0 V, T _J = 55 °C	N-Ch			10		
		V _{DS} = - 12 V, V _{GS} = 0 V, T _J = 55 °C	P-Ch			- 10		
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	N-Ch	15			A	
		V _{DS} ≤ - 5 V, V _{GS} = - 4.5 V	P-Ch	- 8				
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 4.2 A	N-Ch		0.033	0.040	Ω	
		V _{GS} = - 4.5 V, I _D = - 3.3 A	P-Ch		0.058	0.070		
		V _{GS} = 2.5 V, I _D = 3.8 A	N-Ch		0.039	0.048		
		V _{GS} = - 2.5 V, I _D = - 2.8 A	P-Ch		0.082	0.100		
		V _{GS} = 1.8 V, I _D = 1.6 A	N-Ch		0.051	0.063		
		V _{GS} = - 1.8 V, I _D = - 0.7 A	P-Ch		0.111	0.140		
Forward Transconductance ^b	g _{fs}	V _{DS} = 10 V, I _D = 4.2 A	N-Ch		13		S	
		V _{DS} = - 10 V, I _D = - 3.3 A	P-Ch		9			
Dynamic ^a								
Input Capacitance	C _{iss}	N-Channel V _{DS} = 6 V, V _{GS} = 0 V, f = 1 MHz P-Channel V _{DS} = - 6 V, V _{GS} = 0 V, f = 1 MHz	N-Ch		400		pF	
Output Capacitance	C _{oss}		P-Ch		400			
			N-Ch		120			
Reverse Transfer Capacitance	C _{rss}		P-Ch		140			
		N-Ch		70				
Total Gate Charge	Q _g	N-Channel V _{DS} = 6 V, V _{GS} = 4.5 V, I _D = 5.5 A P-Channel V _{DS} = - 6 V, V _{GS} = - 4.5 V, I _D = - 4.3 A	N-Ch		7.5	12	nC	
			P-Ch		8	12		
			N-Ch		4.5	6.8		
			P-Ch		5	7.5		
	Gate-Source Charge	Q _{gs}	N-Ch		0.6			
			P-Ch		0.8			
Gate-Drain Charge	Q _{gd}	N-Ch		0.8				
		P-Ch		1.4				
Gate Resistance	R _g	f = 1 MHz	N-Ch		2.5		Ω	
			P-Ch		7			

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.



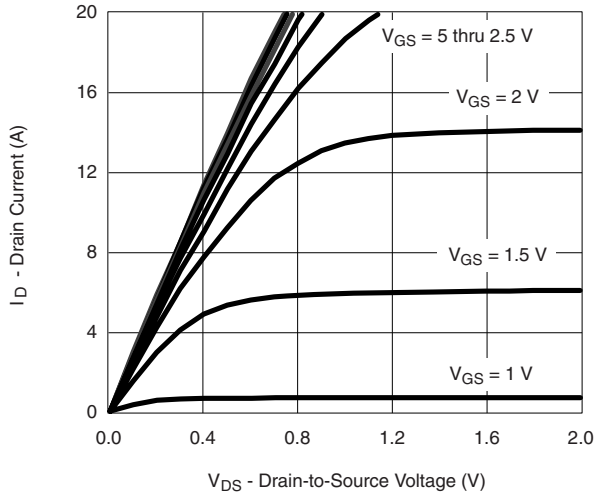
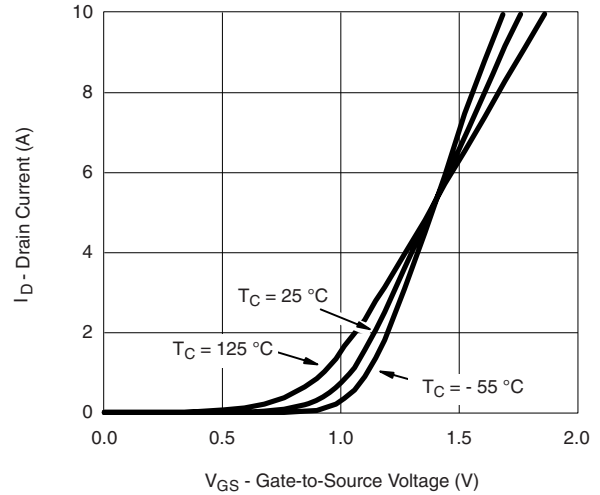
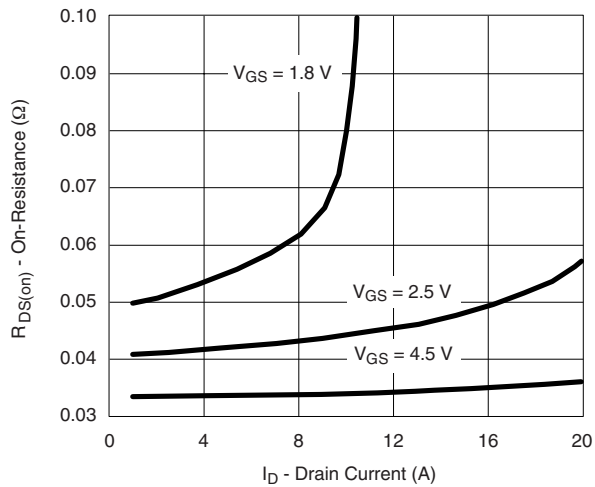
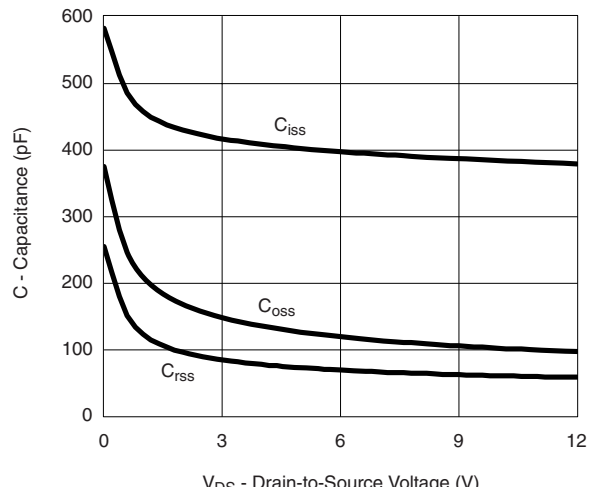
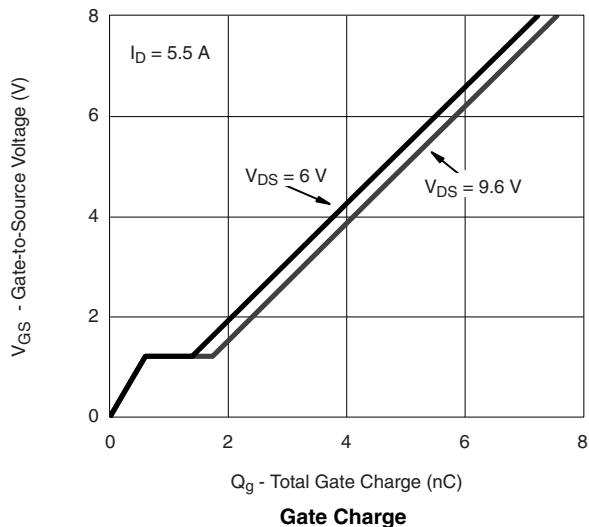
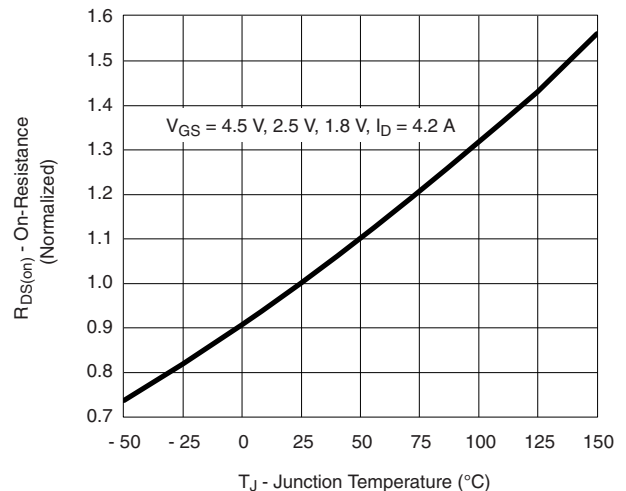
SPECIFICATIONS T _J = 25 °C, unless otherwise noted								
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit		
Dynamic ^a								
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 6 V, R _L = 1.4 Ω I _D ≅ 4.4 A, V _{GEN} = 4.5 V, R _g = 1 Ω	N-Ch		5	10	ns	
			P-Ch		15	25		
Rise Time	t _r		N-Ch		15	25		
			P-Ch		25	40		
Turn-Off Delay Time	t _{d(off)}	P-Channel V _{DD} = - 6 V, R _L = 1.8 Ω I _D ≅ - 3.4 A, V _{GEN} = - 4.5 V, R _g = 1 Ω	N-Ch		35	55		
			P-Ch		20	30		
Fall Time	t _f		N-Ch		15	25		
			P-Ch		10	15		
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 6 V, R _L = 1.4 Ω I _D ≅ 4.4 A, V _{GEN} = 10 V, R _g = 1 Ω	N-Ch		5	10		
			P-Ch		5	10		
Rise Time	t _r		N-Ch		10	15		
			P-Ch		12	20		
Turn-Off Delay Time	t _{d(off)}	P-Channel V _{DD} = - 6 V, R _L = 1.8 Ω I _D ≅ - 3.4 A, V _{GEN} = - 10 V, R _g = 1 Ω	N-Ch		15	25		
			P-Ch		20	30		
Fall Time	t _f		N-Ch		10	15		
			P-Ch		10	15		
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	N-Ch			4.5	A	
			P-Ch			- 4.5		
Pulse Diode Forward Current ^a	I _{SM}		N-Ch			20		
			P-Ch			- 10		
Body Diode Voltage	V _{SD}	I _S = 4.4 A, V _{GS} = 0 V	N-Ch		0.8	1.2	V	
		I _S = - 3.4 A, V _{GS} = 0 V	P-Ch		- 0.8	- 1.2		
Body Diode Reverse Recovery Time	t _{rr}	N-Channel I _F = 4.4 A, di/dt = 100 A/μs, T _J = 25 °C P-Channel I _F = - 3.4 A, di/dt = - 100 A/μs, T _J = 25 °C	N-Ch		15	30	ns	
			P-Ch		30	60		
Body Diode Reverse Recovery Charge	Q _{rr}		N-Ch		8	20	nC	
			P-Ch		12	24		
Reverse Recovery Fall Time	t _a			N-Ch		8.5		ns
				P-Ch		14		
Reverse Recovery Rise Time	t _b			N-Ch		8.5		
				P-Ch		16		

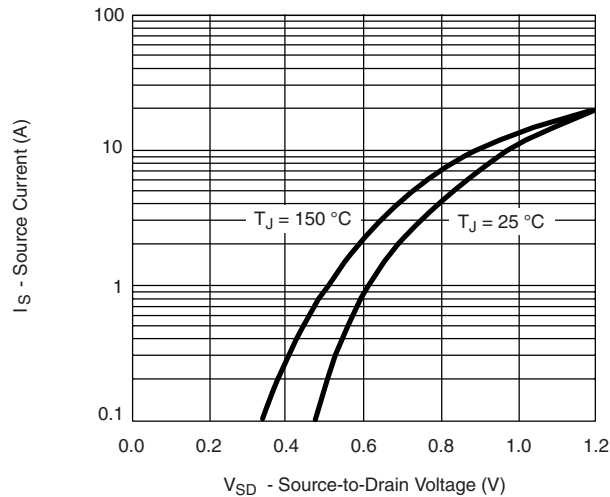
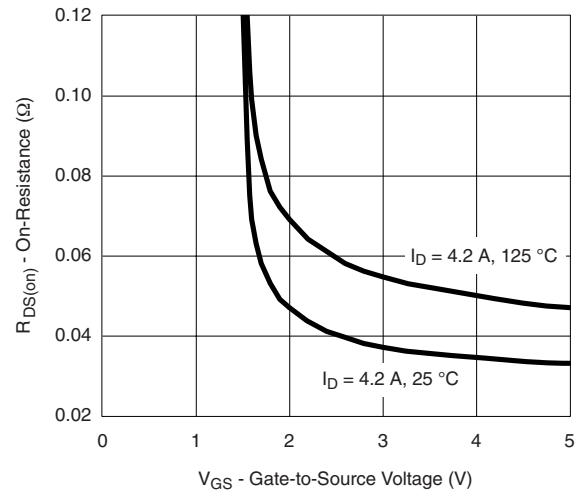
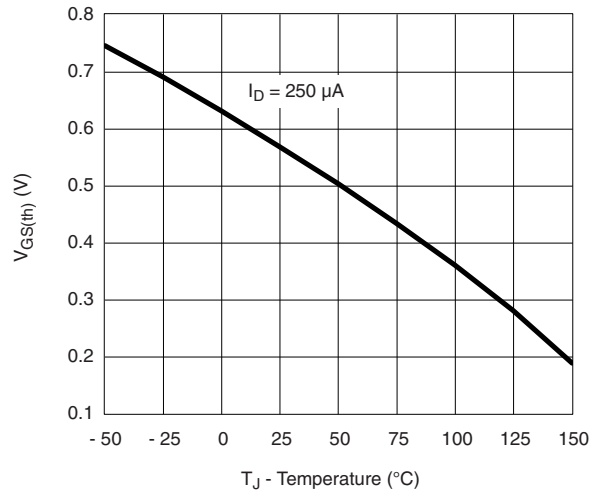
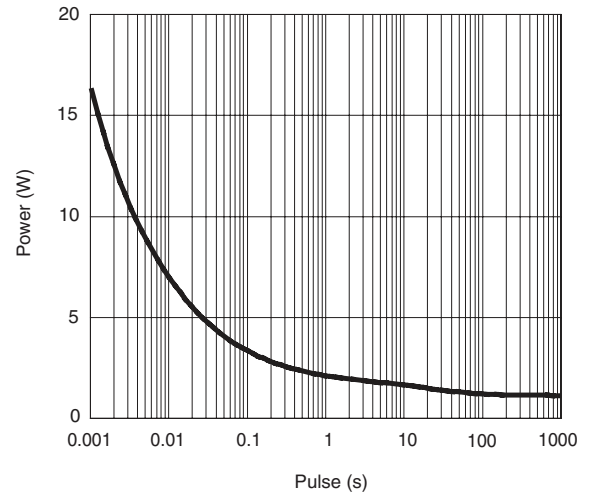
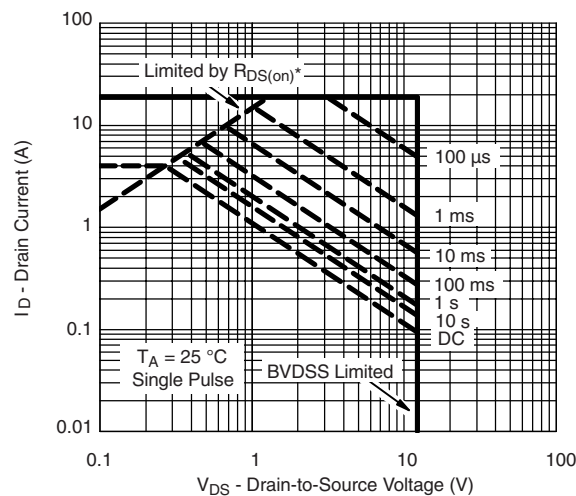
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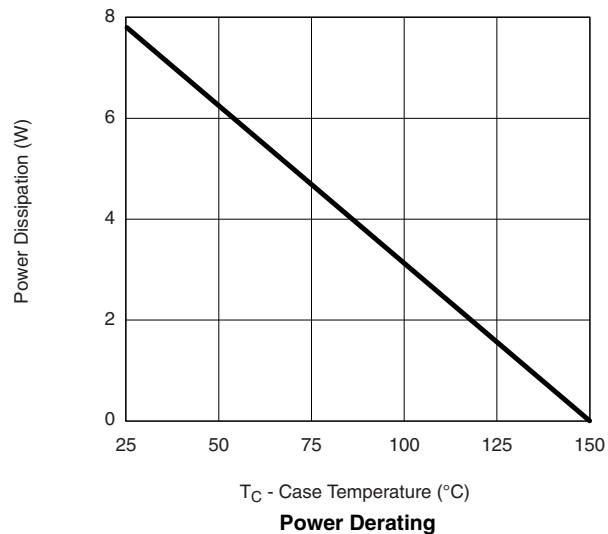
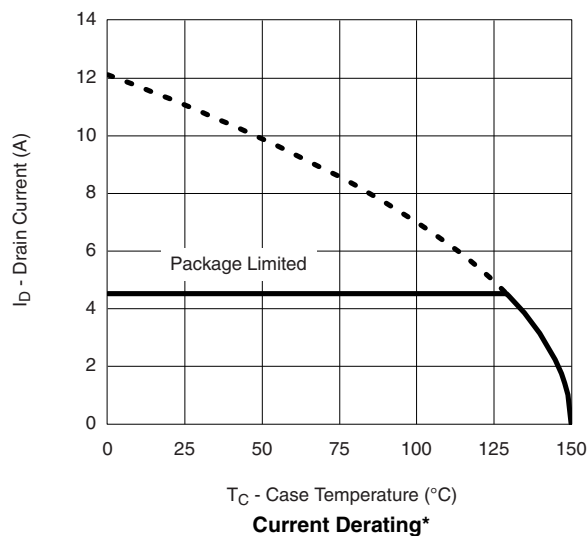
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

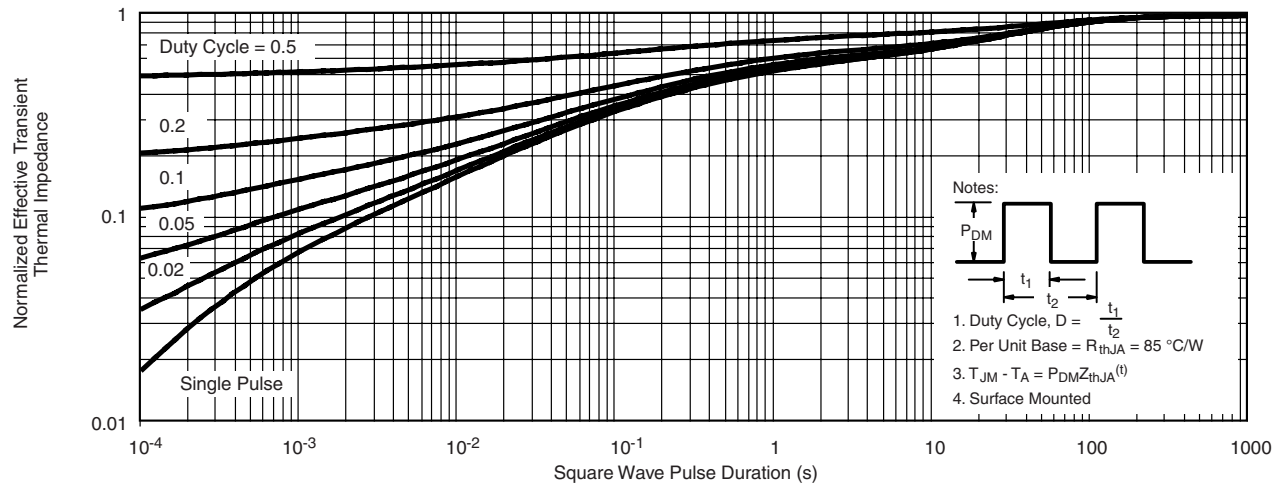
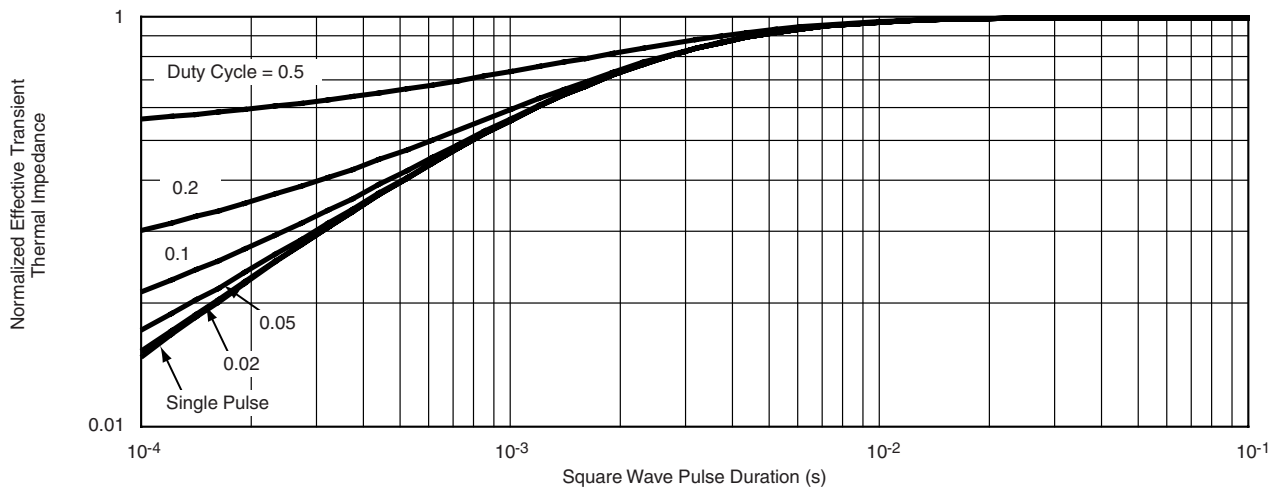
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

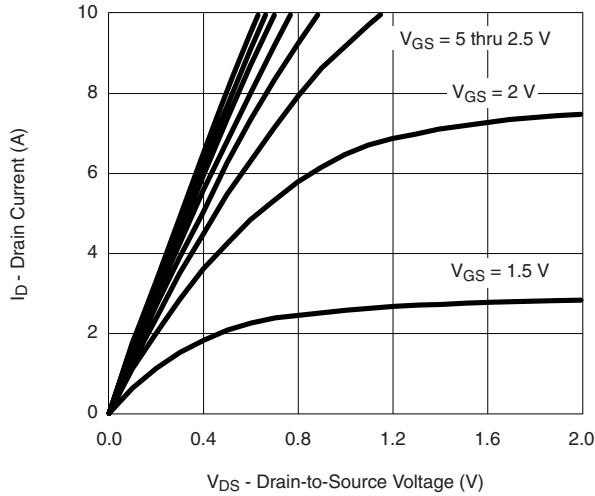
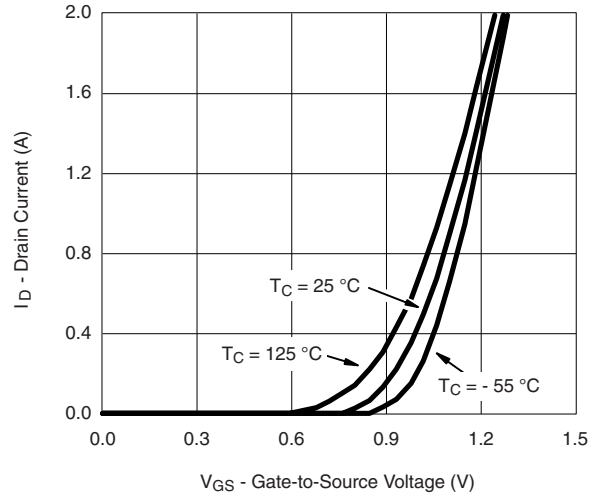
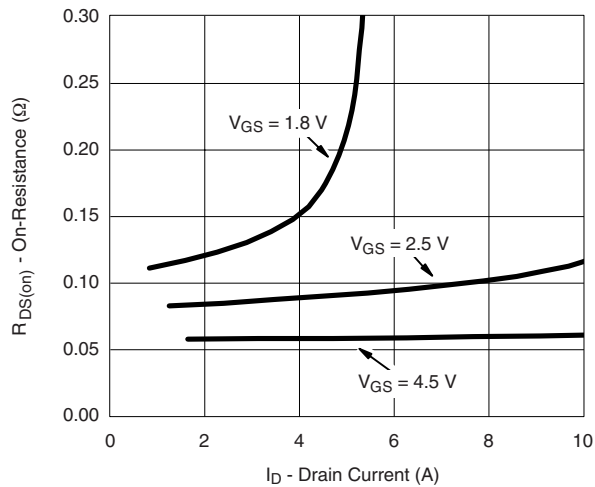
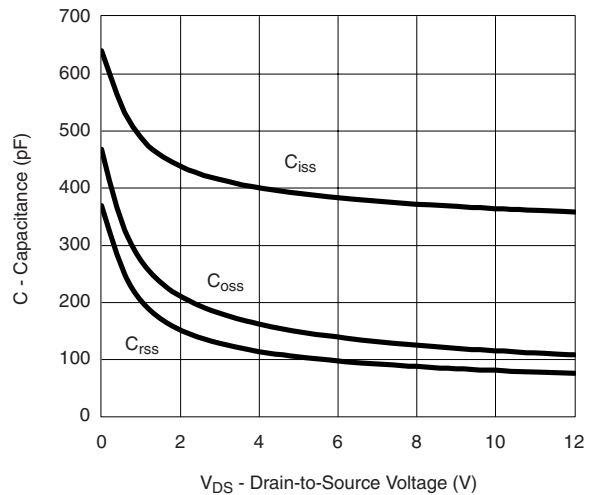
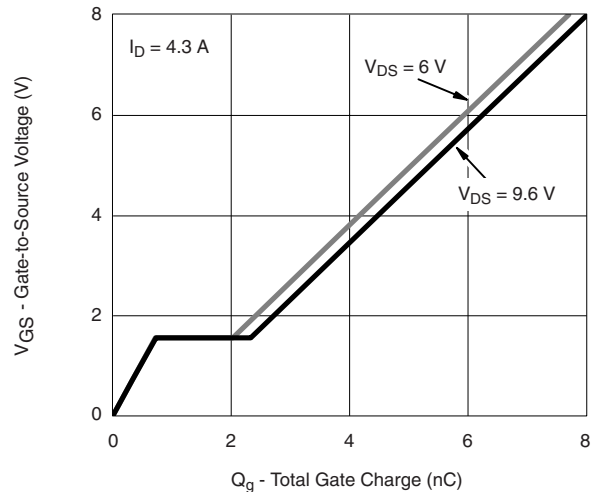
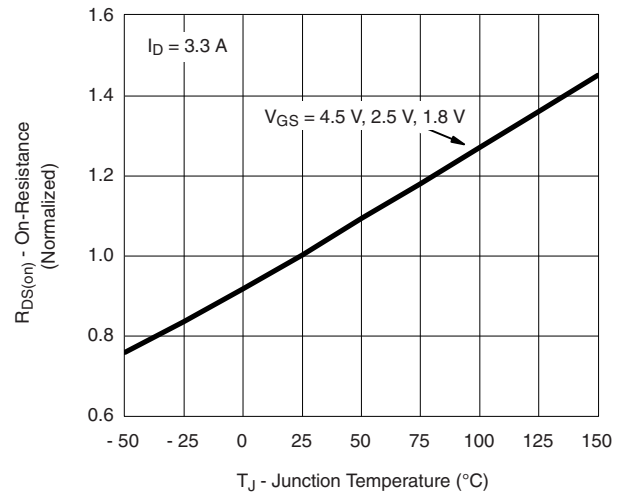
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current and Gate Voltage****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

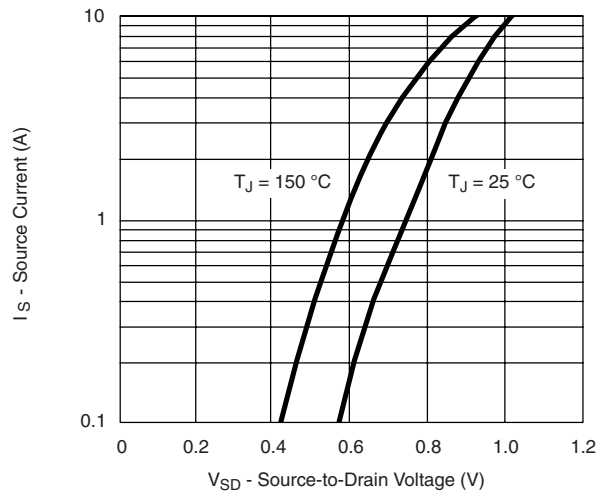
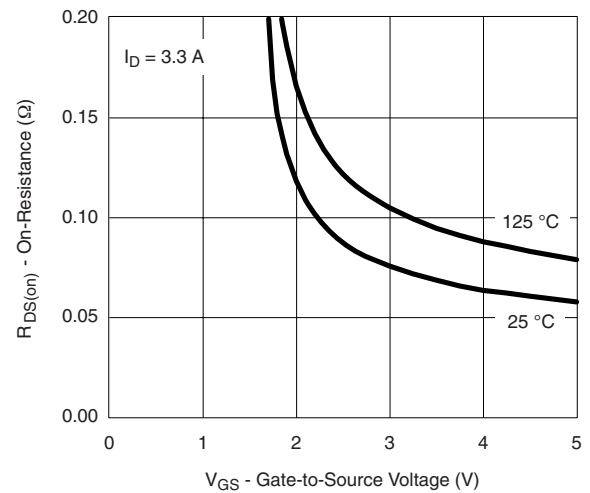
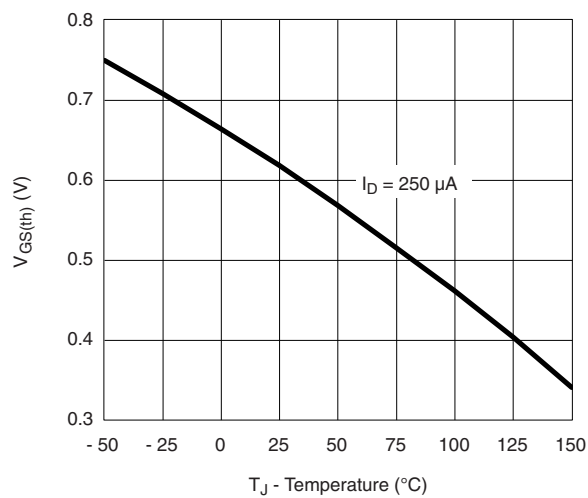
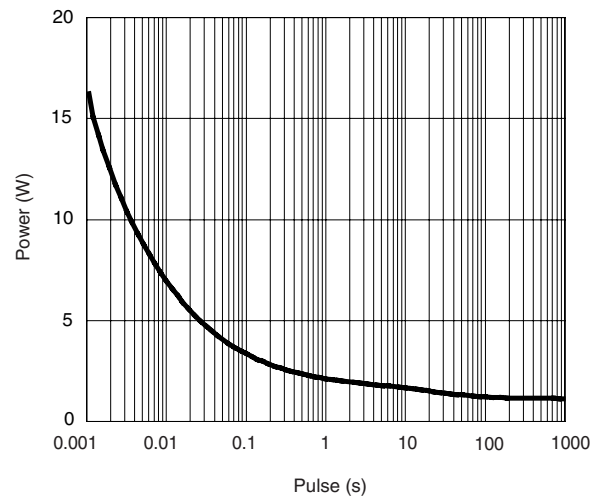
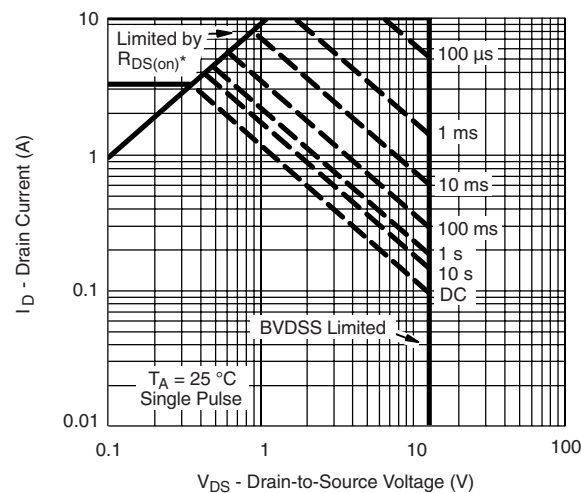
**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power (Junction-to-Ambient)*** $V_{GS} > \text{minimum } V_{GS} \text{ at which } R_{DS(on)} \text{ is specified}$ **Safe Operating Area, Junction-to-Ambient**

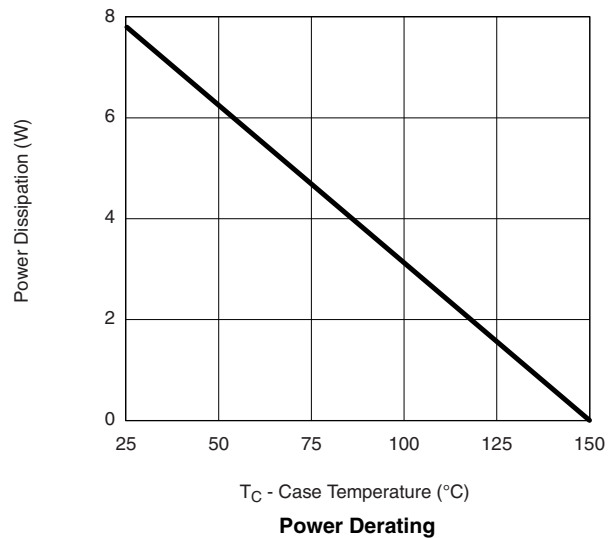
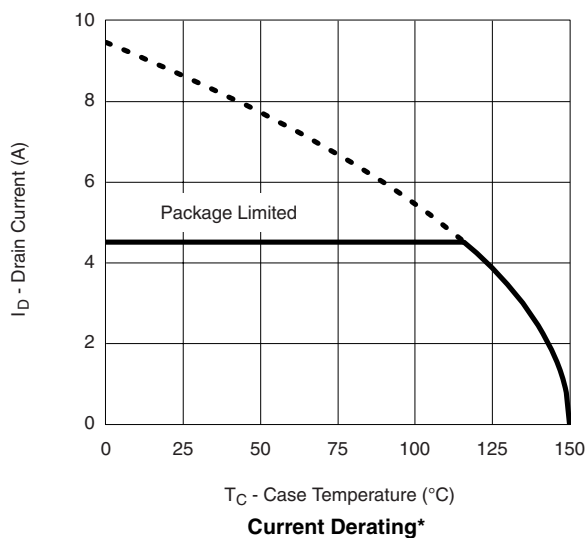
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

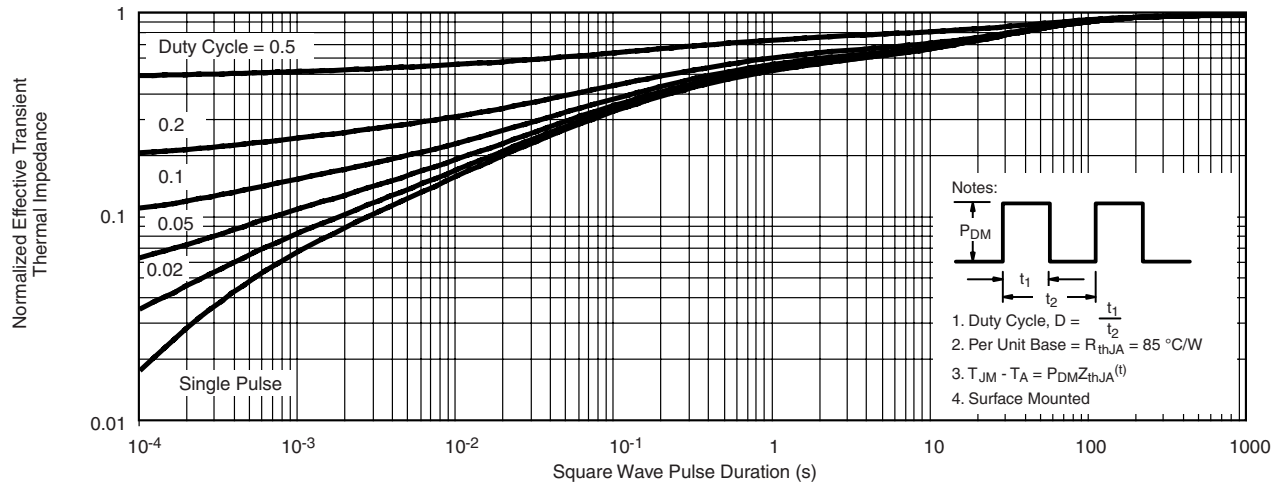
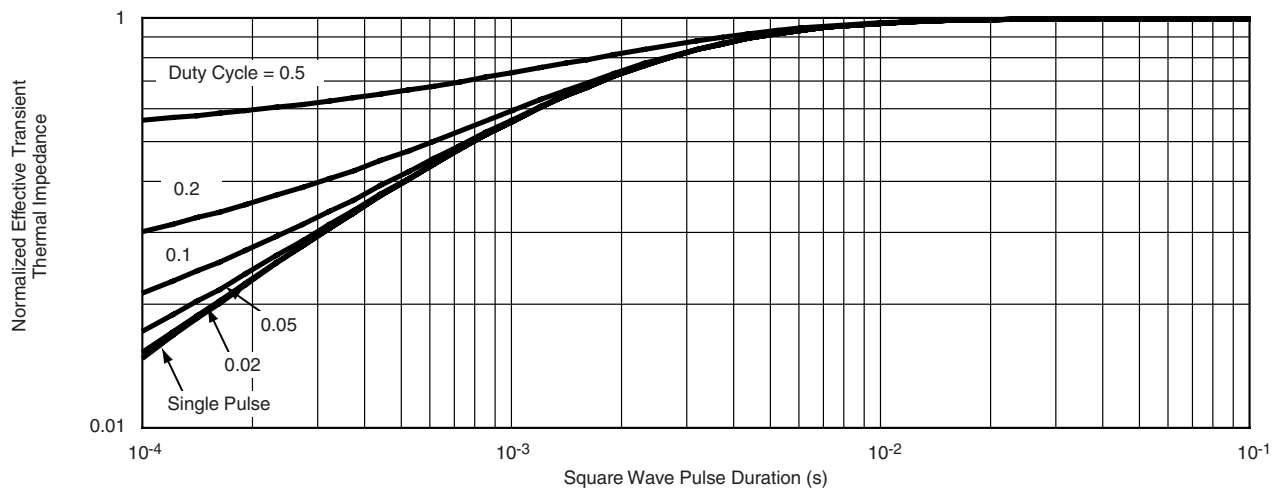
**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Foot**

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current and Gate Voltage****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient*** $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Ambient**

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

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