## FEATURES

**Very low offset voltage: 10 µV max over temperature**
**Very low input offset voltage drift: 50 nV/°C max**
**High CMRR: 96 dB min**
**Digitally programmable gain and output offset voltage**
**Gain Range from 28 to 1300**
**Single-wire serial interface**
**Stable with any capacitive load**
**SOIC_N and LFCSP_VQ packages**
**2.7 V to 5.5 V operation**

## APPLICATIONS

**Automotive sensors**
**Pressure and position sensors**
**Precision current sensing**
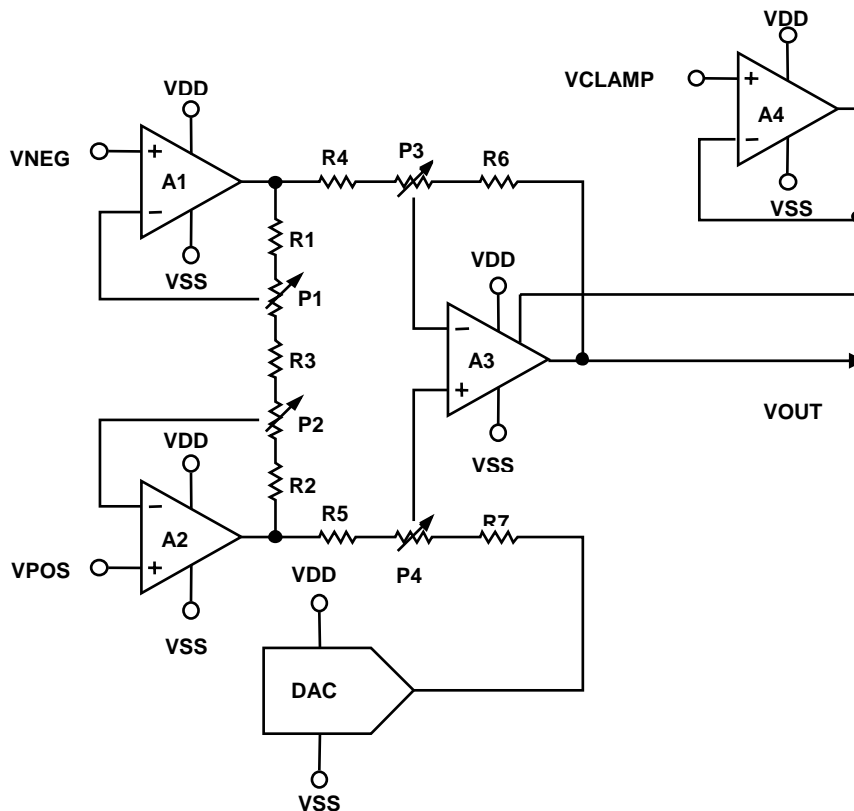**Thermocouple amplifiers**
**Industrial weigh scales**
**Strain gages**

## FUNCTIONAL BLOCK DIAGRAM



*Figure 1.*

# TABLE OF CONTENTS

## REVISION HISTORY

**XXXX—Revision 0: Initial Version**

# GENERAL DESCRIPTION

The AD8557 is a zero-drift, sensor signal amplifier with digitally programmable gain and output offset. Designed to easily and accurately convert variable pressure sensor and strain bridge outputs to a well-defined output voltage range, the AD8557 accurately amplifies many other differential or single-ended sensor outputs. The AD8557 uses the ADI patented low noise auto-zero and DigiTrim® technologies to create an incredibly accurate and flexible signal processing solution in a very compact footprint.

Gain is digitally programmable in a wide range from 28 to 1300 through a serial data interface. Gain adjustment can be fully simulated in-circuit and then permanently programmed with reliable polyfuse technology. Output offset voltage is also digitally programmable and is ratiometric to the supply voltage. When used in conjunction with an ADC referenced to the same supply, the system accuracy becomes immune to normal supply voltage variations. Output offset voltage can be adjusted with a resolution of better than 0.4% of the difference between VDD

and VSS. A lockout trim after gain and offset adjustment further ensures field reliability.

In addition to extremely low input offset voltage and input offset voltage drift and very high dc and ac CMRR, the AD8557 also includes a pull-up current source at the input pins and a pull-down current source at the VCLAMP pin. Output clamping set via an external reference voltage allows the AD8557 to drive lower voltage ADCs safely and accurately.

When used in conjunction with an ADC referenced to the same supply, the system accuracy becomes immune to normal supply voltage variations. Output offset voltage can be adjusted with a resolution of better than 0.4% of the difference between VDD and VSS. A lockout trim after gain and offset adjustment further ensures field reliability.

The AD8557 is fully specified from −40°C to +125°C. Operating from single-supply voltages of 2.7 V to 5.5 V, the AD8557 is offered in the 8-lead SOIC_N, and 4 mm × 4 mm 16-lead LFCSP_VQ.

# SPECIFICATIONS

VDD = 5.0 V, VSS = 0.0 V, $V_{CM}$ = 2.5 V, $V_O$ = 2.5 V, Gain = 28, $T_A$ = 25°C, unless otherwise specified.

**Table 1. Electrical Specifications**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INPUT STAGE | | | | | | |
| Input Offset Voltage | $V_{OS}$ | −40°C ≤ $T_A$ ≤ +125°C | | 2 | 10 | µV |
| Input Offset Voltage Drift | $T_CV_{OS}$ | | | | 50 | nV/°C |
| Input Bias Current | $I_B$ | −40°C ≤ $T_A$ ≤ +125°C | 8 | 18 | 28 | nA |
| Input Offset Current | $I_{OS}$ | −40°C ≤ $T_A$ ≤ +125°C | | 1 | 8 | nA |
| Input Voltage Range | | | 0.8 | | 3.6 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = 0.9 V to 3.6 V, $A_v$ = 28 | 70 | 82 | | dB |
| | | $V_{CM}$ = 0.9 V to 3.6 V, $A_v$ = 1300 | 96 | 112 | | dB |
| Linearity | | $V_O$ = 0.2 V to 3.4 V | | 20 | | ppm |
| | | $V_O$ = 0.2 V to 4.8 V | | 1000 | | ppm |
| Differential Gain Accuracy | | Second stage gain = 10 to 70 | | | 1.6 | % |
| Differential Gain Accuracy | | Second stage gain = 100 to 250 | | | 2.5 | % |
| Differential Gain Temperature Coefficient | | Second stage gain = 10 to 250 | | 15 | 40 | ppm/°C |
| DAC | | | | | | |
| Accuracy | | Offset codes = 8 to 248 | | 0.7 | 0.8 | % |
| Ratiometricity | | Offset codes = 8 to 248 | | 50 | | ppm |
| Output Offset | | Offset codes = 8 to 248 | | 5 | 35 | mV |
| Temperature Coefficient | | | | 20 | 80 | ppm FS/°C |
| VCLAMP | | | | | | |
| Input Bias Current | ICLAMP | | 100 | 166 | 330 | nA |
| Input Voltage Range | | | 1.25 | | 2.64 | V |
| OUTPUT STAGE | | | | | | |
| Short-Circuit Current | $I_{SC}$ | Source | | -40 | -25 | mA |
| | $I_{SC}$ | Sink | 40 | 50 | | mA |
| Output Voltage, Low | $V_{OL}$ | $R_L$ = 10 kΩ to 5 V | | | 30 | mV |
| Output Voltage, High | $V_{OH}$ | $R_L$ = 10 kΩ to 0 V | 4.94 | | | V |
| POWER SUPPLY | | | | | | |
| Supply Current | $I_{SY}$ | $V_O$ = 2.5 V, VPOS = VNEG = 2.5 V, VDAC code = XXXX | | 1.8 | | mA |
| Power Supply Rejection Ratio | PSRR | | | 125 | | dB |
| | | −40°C ≤ $T_A$ ≤ +125°C | 105 | | | |
| DYNAMIC PERFORMANCE | | | | | | |
| Gain Bandwidth Product | GBP | First gain stage | | 2 | | MHz |
| | | Second gain stage | | 8 | | MHz |
| Settling Time | $t_s$ | To 0.1%, 4 V output step | | 8 | | µs |
| NOISE PERFORMANCE | | | | | | |
| Input Referred Noise | | f = 1 kHz | | 32 | | nV/√Hz |
| Low Frequency Noise | $e_n$ p-p | f = 0.1 Hz to 10 Hz | | 0.5 | | µV p-p |
| Total Harmonic Distortion | THD | $V_{IN}$ = 16.75 mV rms, f = 1 kHz | | -100 | | dB |
| DIGITAL INTERFACE | | | | | | |
| Input Current | | | | 2 | | µA |
| DIGIN Pulse Width to Load 0 | $tw_0$ | | 0.05 | | 10 | µs |
| DIGIN Pulse Width to Load 1 | $tw_1$ | | 50 | | | µs |
| Time Between Pulses at DIGIN | $tw_s$ | | 10 | | | µs |
| DIGIN Low | | | | | 1 | V |
| DIGIN High | | | 4 | | | V |
| DIGOUT Logic 0 | | | | | 1 | V |

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DIGOUT Logic 1 | | | 4 | | | V |

VDD = 2.7 V, VSS = 0.0 V, $V_{CM}$ = 1.35 V, $V_O$ = 1.35 V, Gain = 28, $T_A$ = 25°C, unless otherwise specified.

**Table 2. Electrical Specifications**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INPUT STAGE | | | | | | |
| Input Offset Voltage | $V_{OS}$ | −40°C ≤ $T_A$ ≤ +125°C | | 2 | 10 | μV |
| Input Offset Voltage Drift | $T_C V_{OS}$ | | | | 50 | nV/°C |
| Input Bias Current | $I_B$ | −40°C ≤ $T_A$ ≤ +125°C | 8 | 18 | 28 | nA |
| Input Offset Current | $I_{OS}$ | −40°C ≤ $T_A$ ≤ +125°C | | 0.2 | 1 | nA |
| Input Voltage Range | | | 0.5 | | 1.6 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = 0.9 V to 3.6 V, $A_V$ = 28 | 70 | 82 | | dB |
| | | $V_{CM}$ = 0.9 V to 3.6 V, $A_V$ = 1300 | 96 | 112 | | dB |
| Linearity | | $V_O$ = 0.2 V to 3.4 V | | 20 | | ppm |
| | | $V_O$ = 0.2 V to 4.8 V | | 1000 | | ppm |
| Differential Gain Accuracy | | Second stage gain = 10 to 250 | | | 1.6 | % |
| Differential Gain Temperature Coefficient | | Second stage gain = 10 to 250 | | 15 | 40 | ppm/°C |
| DAC | | | | | | |
| Accuracy | | Offset codes = 8 to 248 | | 0.7 | 0.8 | % |
| Ratiometricity | | Offset codes = 8 to 248 | | 50 | | ppm |
| Output Offset | | Offset codes = 8 to 248 | | 5 | 35 | mV |
| Temperature Coefficient | | | | 20 | 80 | ppm FS/°C |
| VCLAMP | | | | | | |
| Input Bias Current | ICLAMP | | 100 | 166 | 330 | nA |
| Input Voltage Range | | | 1.25 | | 2.64 | V |
| OUTPUT STAGE | | | | | | |
| Short-Circuit Current | $I_{SC}$ | Source | | -12 | -7 | mA |
| | | Sink | 15 | 20 | | mA |
| Output Voltage, Low | $V_{OL}$ | $R_L$ = 10 kΩ to 5 V | | | 30 | mV |
| Output Voltage, High | $V_{OH}$ | $R_L$ = 10 kΩ to 0 V | 2.64 | | | V |
| POWER SUPPLY | | | | | | |
| Supply Current | $I_{SY}$ | $V_O$ = 2.5 V, VPOS = VNEG = 2.5 V, VDAC code = XXXX | | 1.8 | | mA |
| Power Supply Rejection Ratio | PSRR | | | 125 | | dB |
| | | −40°C ≤ $T_A$ ≤ +125°C | 105 | | | |
| DYNAMIC PERFORMANCE | | | | | | |
| Gain Bandwidth Product | GBP | First gain stage | | 2 | | MHz |
| | | Second gain stage | | 8 | | MHz |
| Settling Time | $t_s$ | To 0.1%, 4 V output step | | 8 | | μs |
| NOISE PERFORMANCE | | | | | | |
| Input Referred Noise | | f = 1 kHz | | 32 | | nV/√Hz |
| Low Frequency Noise | $e_n$ p-p | f = 0.1 Hz to 10 Hz | | 0.5 | | μV p-p |
| Total Harmonic Distortion | THD | $V_{IN}$ = 16.75 mV rms, f = 1 kHz | | -100 | | dB |
| DIGITAL INTERFACE | | | | | | |
| Input Current | | | | 2 | | μA |
| DIGIN Pulse Width to Load 0 | $tw_0$ | | 0.05 | | 10 | μs |
| DIGIN Pulse Width to Load 1 | $tw_1$ | | 50 | | | μs |
| Time Between Pulses at DIGIN | $tw_s$ | | 10 | | | μs |
| DIGIN Low | | | | | 1 | V |
| DIGIN High | | | 4 | | | V |
| DIGOUT Logic 0 | | | | | 1 | V |
| DIGOUT Logic 1 | | | 4 | | | V |

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| Supply Voltage | 6 V |
| Input Voltage | VSS − 0.3 V to VDD + 0.3 V |
| Differential Input Voltage[1] | ±5.0 V |
| Output Short-Circuit Duration to VSS or VDD | Indefinite |
| ESD (Human Body Model) | 2000 V |
| Storage Temperature Range | −65°C to +150°C |
| Operating Temperature Range | −40°C to +125°C |
| Junction Temperature Range | −65°C to +150°C |
| Lead Temperature Range | 300°C |

[1] Differential input voltage is limited to ±5.0 V or ± the supply voltage, which-ever is less.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 3. Thermal Resistance**

| Package Type | $\theta_{JA}$[1] | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 8-Lead SOIC_N (R) | 158 | 43 | °C/W |
| 16-Lead LFCSP_VQ (CP) | 44 | 31.5 | °C/W |

[1] $\theta_{JA}$ is specified for the worst-case conditions, that is, $\theta_{JA}$ is specified for device soldered in circuit board for LFCSP_VQ package.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS
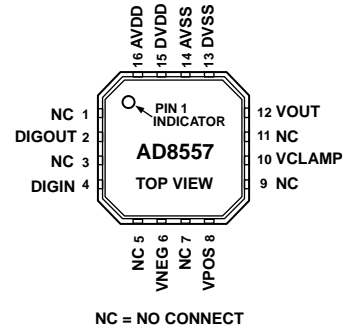


*Figure 2. 8-Lead SOIC_N Pin Configuration*



*Figure 3. 16-Lead LFCSP_VQ Pin Configuration*

**Table 4. Pin Function Descriptions**

| Pin No. | | Mnemonic | Description |
|---|---|---|---|
| **SOIC_N** | **LFCSP_VQ** | | |
| 1 | | VDD | Positive Supply Voltage. |
| 2 | 2 | DIGOUT | In read mode this pin functions as a digital output. |
| 3 | 4 | DIGIN | Digital Input. |
| 4 | 6 | VNEG | Negative Amplifier Input (Inverting Input). |
| 5 | 8 | VPOS | Positive Amplifier Input (Noninverting Input). |
| 6 | 10 | VCLAMP | Set Clamp Voltage at Output. |
| 7 | 12 | VOUT | Amplifier Output. |
| 8 | | VSS | Negative Supply Voltage. |
| | 13, 14 | DVSS, AVSS | Negative Supply Voltage. |
| | 15, 16 | DVDD, AVDD | Positive Supply Voltage. |
| | 1, 3, 5, 7, 9, 11 | NC | Do Not Connect. |

# TYPICAL PERFORMANCE CHARACTERISTICS

*Figure 4. Input Offset Voltage Distribution*

*Figure 5. Input Offset Voltage vs. Common-Mode Voltage*

*Figure 6. Input Offset Voltage vs. Temperature*

*Figure 7. $T_CV_{OS}$ at $V_{SY}$ = 5 V*

*Figure 8. Output Buffer Offset vs. Temperature*

*Figure 9. Input Bias Current at VPOS, VNEG vs. Temperature*

*Figure 10. Input Bias Current at VPOS, VNEG vs. Common-Mode Voltage*

*Figure 11. Input Offset Current vs. Temperature*

*Figure 12. Digital Input Current vs. Digital Input Voltage (Pin 4)*

*Figure 13. VCLAMP Current over Temperature at $V_S$ = 5 V vs. VCLAMP Voltage*

*Figure 14. Supply Current ($I_{SY}$) vs. Supply Voltage*

*Figure 15. Supply Current ($I_{SY}$) vs. Temperature*

*Figure 16. CMRR vs. Frequency*

*Figure 17. CMRR vs. Frequency*

*Figure 18. CMRR vs. Temperature at Different Gains*

*Figure 19. Input Voltage Noise Density vs. Frequency (0 Hz to 10 kHz)*

*Figure 20. Input Voltage Noise Density vs. Frequency (0 Hz to 500 kHz)*

*Figure 21. Low Frequency Input Voltage Noise (0.1 Hz to 10 Hz)*

*Figure 22. Low Frequency Input Voltage Noise (0.1 Hz to 10 Hz)*

*Figure 23. Closed-Loop Gain vs. Frequency Measured at Filter Pin*

*Figure 24. Closed-Loop Gain vs. Frequency Measured at Output Pin*

*Figure 25. Output Buffer Gain vs. Frequency*

*Figure 26. Output Buffer Positive Overshoot*

*Figure 27. Output Buffer Negative Overshoot*

*Figure 28. Output Voltage to Supply Rail vs. Load Current*

*Figure 29. Output Short-Circuit vs. Temperature*

*Figure 30. Power-On Response at 25℃*

*Figure 31. Power-On Response at 125℃*

*Figure 32. Power-On Response at −40℃*

*Figure 33. PSRR vs. Temperature*

*Figure 34. PSRR vs. Frequency*

*Figure 35. Small Signal Response*

*Figure 36. Small Signal Response*

www.DataSheet4U.com

*Figure 37. Large Signal Response*

*Figure 43. Positive Overload Recovery (Gain = 1280)*

*Figure 38. Large Signal Response*

*Figure 44. Settling Time 0.1%*

*Figure 39. Output Impedance vs. Frequency*

*Figure 45. Settling Time 0.01%*

*Figure 40. Negative Overload Recovery (Gain = 70)*

*Figure 46. THD vs. Frequency*

*Figure 41. Positive Overload Recovery (Gain = 70)*

*Figure 42. Negative Overload Recovery (Gain = 1280)*

## THEORY OF OPERATION

A1, A2, R1, R2, R3, P1, and P2 form the first gain stage of the differential amplifier. A1 and A2 are auto-zeroed op amps that minimize input offset errors. P1 and P2 are digital potentiometers, guaranteed to be monotonic. Programming P1 and P2 allows the first stage gain to be varied from 2.8 to 5.2 with 7-bit resolution (see Table 5 and Equation 1), giving a fine gain adjustment resolution of 0.37%. R1, R2, R3, P1, and P2 each have a similar temperature coefficient, so the first stage gain temperature coefficient is lower than 100 ppm/°C.

$$GAIN1 \approx 2.8 \times \left(\frac{5.2}{2.8}\right)^{\left(\frac{Code}{127}\right)} \quad (1)$$

A3, R4, R5, R6, R7, P3, and P4 form the second gain stage of the differential amplifier. A3 is an auto-zeroed op amp that minimizes input offset errors and also includes an output buffer. P3 and P4 are digital potentiometers, which allow the second stage gain to be varied from 10 to 250 in eight steps (see Table 6). R4, R5, R6, R7, P3, and P4 each have a similar temperature coefficient, so the second stage gain temperature coefficient is lower than 100 ppm/°C. The output stage of A3 is supplied from a buffered version of VCLAMP instead of VDD, allowing the positive swing to be limited.

A4 implements a voltage buffer, which provides the positive supply to the output stage of A3. Its function is to limit VOUT to a maximum value, useful for driving analog-to-digital converters (ADC) operating on supply voltages lower than

VDD. The input to A4, VCLAMP, has a very high input resistance. It should be connected to a known voltage and not left floating. However, the high input impedance allows the clamp voltage to be set using a high impedance source, such as, a potential divider. If the maximum value of VOUT does not need to be limited, VCLAMP should be connected to VDD.

An 8-bit digital-to-analog converter (DAC) is used to generate a variable offset for the amplifier output. This DAC is guaranteed to be monotonic. To preserve the ratiometric nature of the input signal, the DAC references are driven from VSS and VDD, and the DAC output can swing from VSS (Code 0) to VDD (Code 255). The 8-bit resolution is equivalent to 0.39% of the difference between VDD and VSS, for example, 19.5 mV with a 5 V supply. The DAC output voltage (VDAC) is given approximately by

$$VDAC \approx \left(\frac{Code + 0.5}{256}\right)(VDD - VSS) + VSS \quad (2)$$

Where the temperature coefficient of *VDAC* is lower than 200 ppm/°C.

The amplifier output voltage (VOUT) is given by

$$VOUT = GAIN(VPOS - VNEG) + VDAC \quad (3)$$

where *GAIN* is the product of the first and second stage gains.

{insert picture}

*Figure 47. Functional Schematic*

## GAIN VALUES

Table 5. First Stage Gain vs. First Stage Gain Code

| First Stage Gain Code | First Stage Gain | First Stage Gain Code | First Stage Gain | First Stage Gain Code | First Stage Gain | First Stage Gain Code | First Stage Gain |
|---|---|---|---|---|---|---|---|
| 0 | | 32 | | 64 | | 96 | |
| 1 | | 33 | | 65 | | 97 | |
| 2 | | 34 | | 66 | | 98 | |
| 3 | | 35 | | 67 | | 99 | |
| 4 | | 36 | | 68 | | 100 | |
| 5 | | 37 | | 69 | | 101 | |
| 6 | | 38 | | 70 | | 102 | |
| 7 | | 39 | | 71 | | 103 | |
| 8 | | 40 | | 72 | | 104 | |
| 9 | | 41 | | 73 | | 105 | |
| 10 | | 42 | | 74 | | 106 | |
| 11 | | 43 | | 75 | | 107 | |
| 12 | | 44 | | 76 | | 108 | |
| 13 | | 45 | | 77 | | 109 | |
| 14 | | 46 | | 78 | | 110 | |
| 15 | | 47 | | 79 | | 111 | |
| 16 | | 48 | | 80 | | 112 | |
| 17 | | 49 | | 81 | | 113 | |
| 18 | | 50 | | 82 | | 114 | |
| 19 | | 51 | | 83 | | 115 | |
| 20 | | 52 | | 84 | | 116 | |
| 21 | | 53 | | 85 | | 117 | |
| 22 | | 54 | | 86 | | 118 | |
| 23 | | 55 | | 87 | | 119 | |
| 24 | | 56 | | 88 | | 120 | |
| 25 | | 57 | | 89 | | 121 | |
| 26 | | 58 | | 90 | | 122 | |
| 27 | | 59 | | 91 | | 123 | |
| 28 | | 60 | | 92 | | 124 | |
| 29 | | 61 | | 93 | | 125 | |
| 30 | | 62 | | 94 | | 126 | |
| 31 | | 63 | | 95 | | 127 | |

Table 6. Second Stage Gain and Gain Ranges vs. Second Stage Gain Code

| Second Stage Gain Code | Second Stage Gain | Minimum Combined Gain | Maximum Combined Gain |
|---|---|---|---|
| 0 | | | |
| 1 | | | |
| 2 | | | |
| 3 | | | |
| 4 | | | |
| 5 | | | |
| 6 | | | |
| 7 | | | |

## OPEN WIRE FAULT DETECTION

The inputs to A1 and A2, VNEG and VPOS, each have a com-parator to detect whether VNEG or VPOS exceeds a threshold voltage, nominally VDD – 2.0 V. If (VNEG > VDD – 2.0 V) or (VPOS > VDD – 2.0 V), VOUT is clamped to VSS. The output current limit circuit is disabled in this mode, but the maximum sink current is approximately 10 mA when VDD = 5 V. The inputs to A1 and A2, VNEG and VPOS, are also pulled up to VDD by currents IP1 and IP2. These are both nominally 49 nA and matched to within 3 nA. If the inputs to A1 or A2 are accidentally left floating, as with an open wire fault, IP1 and IP2 pull them to VDD which would cause VOUT to swing to VSS, allowing this fault to be detected. It is not possible to disable IP1 and IP2, nor the clamping of VOUT to VSS, when VNEG or VPOS approaches VDD.

## SHORTED WIRE FAULT DETECTION

The AD8557 provides fault detection in the case where VPOS, VNEG, or VCLAMP shorts to VDD and VSS. Figure 48 shows the voltage regions at VPOS, VNEG, and VCLAMP that trigger an error condition. When an error condition occurs, the VOUT pin is shorted to VSS. Table 7 lists the voltage levels shown in Figure 48.
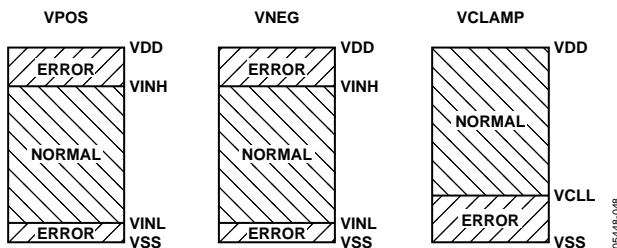


*Figure 48. Voltage Regions at VPOS, VNEG, and VCLAMP
that Trigger a Fault Condition*

**Table 7. Typical VINL, VINH, and VCLL Values (VDD = 5 V)**

| Voltage | Min (V) | Max (V) | VOUT Condition |
|---------|---------|---------|----------------|
| VINH | 3.9 | 4.2 | Short to VSS fault detection |
| VINL | 0.195 | 0.55 | Short to VSS fault detection |
| VCLL | 1.0 | 1.2 | Short to VSS fault detection |

## FLOATING VPOS, VNEG, OR VCLAMP FAULT DETECTION

A floating fault condition at the VPOS, VNEG, or VCLAMP pins is detected by using a low current to pull a floating input into an error voltage range, defined in the previous section. In this way, the VOUT pin is shorted to VSS when a floating input is detected. Table 8 lists the currents used.

**Table 8. Floating Fault Detection at VPOS, VNEG, and VCLAMP**

| Pin | Typical Current | Goal of Current |
|-----|-----------------|-----------------|
| VPOS | 16 nA pull-up | Pull VPOS above VINH |
| VNEG | 16 nA pull-up | Pull VNEG above VINH |
| VCLAMP | 0.2 µA pull-down | Pull VCLAMP below VCLL |

## DEVICE PROGRAMMING

### *Digital Interface*

The digital interface allows the first stage gain, second stage gain, and output offset to be adjusted and allows desired values for these parameters to be permanently stored by selectively blowing polysilicon fuses. To minimize pin count and board space, a single-wire digital interface is used. The digital input pin, DIGIN, has hysteresis to minimize the possibility of inadvertent triggering with slow signals. It also has a pull-down current sink to allow it to be left floating when programming is not being performed. The pull-down ensures inactive status of the digital input by forcing a dc low voltage on DIGIN.

A short pulse at DIGIN from low to high and back to low again, such as between 50 ns and 10 µs long, loads a 0 into a shift register. A long pulse at DIGIN, such as 50 µs or longer, loads a 1 into the shift register. The time between pulses should be at least 10 µs. Assuming VSS = 0 V, voltages at DIGIN between VSS and $0.2 \times$ VDD are recognized as a low, and voltages at DIGIN between $0.8 \times$ VDD and VDD are recognized as a high. A timing diagram example, Figure 49, shows the waveform for entering code 010011 into the shift register.
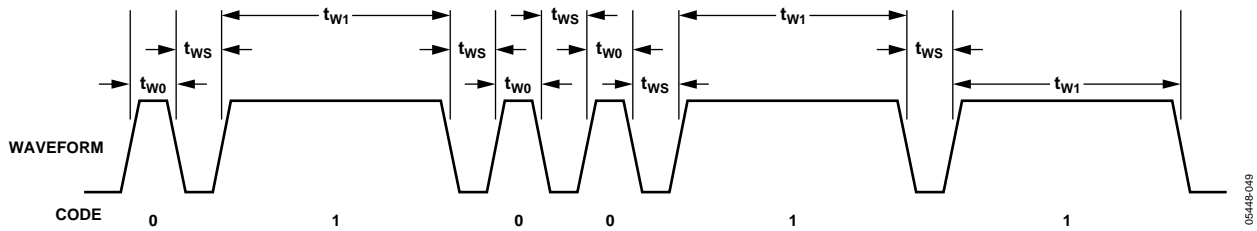
*Figure 49. Timing Diagram for Code 010011*

**Table 9. Timing Specifications**

| Timing Parameter | Description | Specification |
|---|---|---|
| $t_{W0}$ | Pulse Width for Loading 0 into Shift Register | Between 50 ns and 10 μs |
| $t_{W1}$ | Pulse Width for Loading 1 into Shift Register | ≥50 μs |
| $t_{WS}$ | Width Between Pulses | ≥10 μs |

**Table 10. 38-Bit Serial Word Format**

| Field No. | Bits | Description |
|---|---|---|
| 0 | 0 to 11 | 12-Bit Start of Packet 1000 0000 0001 |
| 1 | 12 to 13 | 2-Bit Function<br>00: Change Sense Current<br>01: Simulate Parameter Value<br>10: Program Parameter Value<br>11: Read Parameter Value |
| 2 | 14 to 15 | 2-Bit Parameter<br>00: Second Stage Gain Code<br>01: First Stage Gain Code<br>10: Output Offset Code<br>11: Other Functions |
| 3 | 16 to 17 | 2-Bit Dummy 10 |
| 4 | 18 to 25 | 8-Bit Value<br>Parameter 00 (Second Stage Gain Code): 3 LSBs Used<br>Parameter 01 (First Stage Gain Code): 7 LSBs Used<br>Parameter 10 (Output Offset Code): All 8 Bits Used<br>Parameter 11 (Other Functions)<br>Bit 0 (LSB): Master Fuse<br>Bit 1: Fuse for Production Test at Analog Devices |
| 5 | 26 to 37 | 12-Bit End of Packet 0111 1111 1110 |

A 38-bit serial word is used, divided into 6 fields. Assuming each bit can be loaded in 60 μs, the 38-bit serial word transfers in 2.3 ms. Table 10 summarizes the word format.

Field 0 and Field 5 are the start-of-packet field and end-of-packet field, respectively. Matching the start-of-packet field with 1000 0000 0001 and the end-of-packet field with 0111 1111 1110 ensures that the serial word is valid and enables decoding of the other fields.

Field 3 breaks up the data and ensures that no data combination can inadvertently trigger the start-of-packet and end-of-packet fields. Field 0 should be written first and Field 5 written last.

Within each field, the MSB must be written first and the LSB written last. The shift register features power-on reset to minimize the risk of inadvertent programming; power-on reset occurs when VDD is between 0.7 V and 2.2 V.

### Initial State

Initially, all the polysilicon fuses are intact. Each parameter has the value 0 assigned (see Table 11).

**Table 11. Initial State Before Programming**

| Second Stage Gain Code = 0 | Second Stage Gain = 17.5 |
|---|---|
| First stage gain code = 0 | First stage gain = 4.0 |
| Output offset code = 0 | Output offset = VSS |
| Master fuse = 0 | Master fuse not blown |

When power is applied to a device, parameter values are taken either from internal registers, if the master fuse is not blown, or from the polysilicon fuses, if the master fuse is blown. Programmed values have no effect until the master fuse is blown. The internal registers feature power-on reset, so the unprogrammed devices enter a known state after power-up. Power-on reset occurs when VDD is between 0.7 V and 2.2 V.

### Simulation Mode

The simulation mode allows any parameter to be temporarily changed. These changes are retained until the simulated value is reprogrammed, the power is removed, or the master fuse is blown. Parameters are simulated by setting Field 1 to 01, selecting the desired parameter in Field 2, and the desired value for the parameter in Field 4. Note that a value of 11 for Field 2 is ignored during the simulation mode. Examples of temporary settings follow:

- Setting the second stage gain code (Parameter 00) to 011 and the second stage gain to 50 produces:
  1000 0000 0001 01 00 10 0000 0011 0111 1111 1110

- Setting the first stage gain code (Parameter 01) to 000 1011 and the first stage gain to 4.166 produces:
  1000 0000 0001 01 01 10 0000 1011 0111 1111 1110

  A first stage gain of 4.166 with a second stage gain of 50 gives a total gain of 208.3. This gain has a maximum tolerance of 2.5%.

- Set the output offset code (Parameter 10) to 0100 0000 and the output offset to 1.260 V when VDD = 5 V and VSS = 0 V. This output offset has a maximum tolerance of 0.8%:
  1000 0000 0001 01 10 10 0100 0000 0111 1111 1110

### Programming Mode

Intact fuses give a bit value of 0. Bits with a desired value of 1 need to have the associated fuse blown. Since a relatively large current is needed to blow a fuse, only one fuse can be reliably blown at a time. Thus, a given parameter value may need several 38-bit words to allow reliable programming. A 5.25 V (±0.25 V) supply is required when blowing fuses to minimize the on resistance of the internal MOS switches that blow the fuse. The power supply voltage must not exceed the absolute maximum rating and must be able to deliver 250 mA of current.

At least 10 μF (tantalum type) of decoupling capacitance is needed across the power pins of the device during programming. The capacitance can be on the programming apparatus as long as it is within 2 inches of the device being programmed. An additional 0.1 μF (ceramic type) in parallel with the 10 μF is recommended within ½ inch of the device being programmed. A minimum period of 1 ms should be allowed for each fuse to blow. There is no need to measure the supply current during programming.

The best way to verify correct programming is to use the read mode to read back the programmed values. Then, remeasure the gain and offset to verify these values. Programmed fuses have no effect on the gain and output offset until the master fuse is blown. After blowing the master fuse, the gain and output offset are determined solely by the blown fuses, and the simulation mode is permanently deactivated.

Parameters are programmed by setting Field 1 to 10, selecting the desired parameter in Field 2, and selecting a single bit with the value 1 in Field 4.

As an example, suppose the user wants to permanently set the second stage gain to 50. Parameter 00 needs to have the value 0000 0011 assigned. Two bits have the value 1, so two fuses need to be blown. Since only one fuse can be blown at a time, this code can be used to blow one fuse:
1000 0000 0001 10 00 10 0000 0010 0111 1111 1110

The MOS switch that blows the fuse closes when the complete packet is recognized, and opens when the start-of-packet, dummy, or end-of-packet fields are no longer valid. After 1 ms, this second code is entered to blow the second fuse:
1000 0000 0001 10 00 10 0000 0001 0111 1111 1110

To permanently set the first stage gain to a nominal value of 4.151, Parameter 01 needs to have the value 000 1011 assigned. Three fuses need to be blown, and the following codes are used, with a 1 ms delay after each code:
1000 0000 0001 10 01 10 0000 1000 0111 1111 1110
1000 0000 0001 10 01 10 0000 0010 0111 1111 1110
1000 0000 0001 10 01 10 0000 0001 0111 1111 1110

To permanently set the output offset to a nominal value of 1.260 V when VDD = 5 V and VSS = 0 V, Parameter 10 needs to have the value 0100 0000 assigned. If one fuse needs to be blown, use the following code:
1000 0000 0001 10 10 10 0100 0000 0111 1111 1110

Finally, to blow the master fuse to deactivate the simulation mode and prevent further programming, use code:
1000 0000 0001 10 11 10 0000 0001 0111 1111 1110

There are a total of 20 programmable fuses. Since each fuse requires 1 ms to blow, and each serial word can be loaded in 2.3

ms, the maximum time needed to program the fuses can be as low as 66 ms.

### Read Mode

The values stored by the polysilicon fuses can be sent to the FILT/DIGOUT pin to verify correct programming. Normally, the FILT/DIGOUT pin is only connected to the second gain stage output via RF. During read mode, however, the FILT/DIGOUT pin is also connected to the output of a shift register to allow the polysilicon fuse contents to be read. Since VOUT is a buffered version of FILT/DIGOUT, VOUT also outputs a digital signal during read mode.

Read mode is entered by setting Field 1 to 11 and selecting the desired parameter in Field 2. Field 4 is ignored. The parameter value, stored in the polysilicon fuses, is loaded into an internal shift register, and the MSB of the shift register is connected to the FILT/DIGOUT pin. Pulses at DIGIN shift out the shift register contents to the FILT/DIGOUT pin, allowing the 8-bit parameter value to be read after seven additional pulses; shift-ing occurs on the falling edge of DIGIN. An eighth pulse at DIGIN disconnects FILT/DIGOUT from the shift register and terminates the read mode. If a parameter value is less than eight bits long, the MSBs of the shift register are padded with 0s.

For example, to read the second stage gain, this code is used:
1000 0000 0001 11 00 10 0000 0000 0111 1111 1110
Since the second stage gain parameter value is only three bits long, the FILT/DIGOUT pin has a value of 0 when this code is entered, and remains 0 during four additional pulses at DIGIN. The fifth, sixth, and seventh pulses at DIGIN return the 3-bit value at FILT/DIGOUT, the seventh pulse returns the LSB. An eighth pulse at DIGIN terminates the read mode.

### Sense Current

A sense current is sent across each polysilicon fuse to determine whether it has been blown. When the voltage across the fuse is less than approximately 1.5 V, the fuse is considered not blown, and Logic 0 is output from the OTP cell. When the voltage across the fuse is greater than approximately 1.5 V, the fuse is considered blown, and Logic 1 is output.

When the AD8557 is manufactured, all fuses have a low resistance. When a sense current is sent through the fuse, a voltage less than 0.1 V is developed across the fuse. This is much lower than 1.5 V, so Logic 0 is output from the OTP cell. When a fuse is electrically blown, it should have a very high resistance. When the sense current is applied to the blown fuse, the voltage across the fuse should be larger than 1.5 V, so Logic 1 is output from the OTP cell.

It is theoretically possible, though very unlikely, for a fuse to be incompletely blown during programming, assuming the required conditions are met. In this situation, the fuse could have a medium resistance, neither low nor high, and a voltage of

approximately 1.5 V could be developed across the fuse. Thus, the OTP cell could output Logic 0 or a Logic 1, depending on temperature, supply voltage, and other variables.

To detect this undesirable situation, the sense current can be lowered by a factor of 4 using a specific code. The voltage developed across the fuse would then change from 1.5 V to 0.38 V, and the output of the OTP would be a Logic 0 instead of the expected Logic 1 from a blown fuse. Correctly blown fuses would still output a Logic 1. In this way, incorrectly blown fuses can be detected. Another specific code would return the sense current to the normal (larger) value. The sense current cannot be permanently programmed to the low value. When the AD8557 is powered up, the sense current defaults to the high value.

The low sense current code is:
1000 0000 0001 00 00 10 XXXX XXX1 0111 1111 1110

The normal (high) sense current code is:
1000 0000 0001 00 00 10 XXXX XXX0 0111 1111 1110

### Programming Procedure

For reliable fuse programming, it is imperative to follow the programming procedure requirements, especially the proper supply voltage during programming.

1. When programming the AD8557, the temperature of the device must be between 10°C to 40°C.

2. Set VDD and VSS to the desired values in the application. Use simulation mode to test and determine the desired codes for the second stage gain, first stage gain, and output offset. The nominal values for these parameters are shown in Table 5, Table 6, Equation 2, and Equation 3; use the codes corresponding to these values as a starting point. However, since actual parameter values for given codes vary from device to device, some fine tuning is necessary for the best possible accuracy.

   One way to choose these values is to set the output offset to an approximate value, such as Code 128 for midsupply, to allow the required gain to be determined. Then set the second stage gain so the minimum first stage gain (Code 0) gives a lower gain than required, and the maximum first stage gain (Code 127) gives a higher gain than required. After choosing the second stage gain, the first stage gain can be chosen to fine tune the total gain. Finally, the output offset can be adjusted to give the desired value. After determining the desired codes for second stage gain, first stage gain, and output offset, the device is ready for permanent programming.

   **Important:** Once a programming attempt has been made for any fuse, there should be no further attempt to blow that fuse. If a fuse does not program to the expected state, discard

the unit. The expected incidence rate of attempted but unblown fuses is very small when following the proper programming procedure and conditions.

3. Set VSS to 0 V and VDD to 5.25 V (±0.25 V). Power supplies should be capable of supplying 250 mA at the required voltage and properly bypassed as described in the Programming Mode section. Use program mode to permanently enter the desired codes for the first stage gain, second stage gain, and output offset. Blow the master fuse to allow the AD8557 to read data from the fuses and to prevent further programming.

4. Set VDD and VSS to the desired values in the application. Use read mode with low sense current followed by high sense current to verify programmed codes.

5. Measure gain and offset to verify correct functionality.

### *Determining Optimal Gain and Offset Codes*

First, determine the desired gain:

1. Determine the desired gain, $G_A$ (using the measurements obtained from the simulation).

2. Use Table 6 to determine $G_2$, the second stage gain, such that $(4.00 \times 1.04) < (G_A/G_2) < (6.4/1.04)$. This ensures the first and last codes for the first stage gain are not used, thereby allowing enough first stage gain codes within each second stage gain range to adjust for the 3% accuracy.

Next, set the second stage gain:

1. Use the simulation mode to set the second stage gain to $G_2$.

2. Set the output offset to allow the AD8557 gain to be measured, for example, use Code 128 to set it to midsupply.

3. Use Table 5 or Equation 1 to set the first stage gain code $C_{G1}$, so the first stage gain is nominally $G_A/G_2$.

4. Measure the resulting gain ($G_B$). $G_B$ should be within 3% of $G_A$.

5. Calculate the first stage gain error (in relative terms) $E_{G1} = G_B/G_A - 1$.

6. Calculate the error (in the number of the first stage gain codes) $C_{EG1} = E_{G1}/0.00370$.

7. Set the first stage gain code to $C_{G1} - C_{EG1}$.

8. Measure the gain ($G_C$). $G_C$ should be closer to $G_A$ than to $G_B$.

9. Calculate the error (in relative terms) $E_{G2} = G_C/G_A - 1$.

10. Calculate the error (in the number of the first stage gain codes) $C_{EG2} = E_{G2}/0.00370$.

11. Set the first stage gain code to $C_{G1} - C_{EG1} - C_{EG2}$. The resulting gain should be within one code of $G_A$.

Finally, determine the desired output offset:

1. Determine the desired output offset $O_A$ (using the measurements obtained from the simulation).

2. Use Equation 2 to set the output offset code $C_{O1}$ such that the output offset is nominally $O_A$.

3. Measure the output offset ($O_B$). $O_B$ should be within 3% of $O_A$.

4. Calculate the error (in relative terms) $E_{O1} = O_B/O_A - 1$.

5. Calculate the error (in the number of the output offset codes) $C_{EO1} = E_{O1}/0.00392$.

6. Set the output offset code to $C_{O1} - C_{EO1}$.

7. Measure the output offset ($O_C$). $O_C$ should be closer to $O_A$ than to $O_B$.

8. Calculate the error (in relative terms) $E_{O2} = O_C/O_A - 1$.

9. Calculate the error (in the number of the output offset codes) $C_{EO2} = E_{O2}/0.00392$.

10. Set the output offset code to $C_{O1} - C_{EO1} - C_{EO2}$. The resulting offset should be within one code of $O_A$.
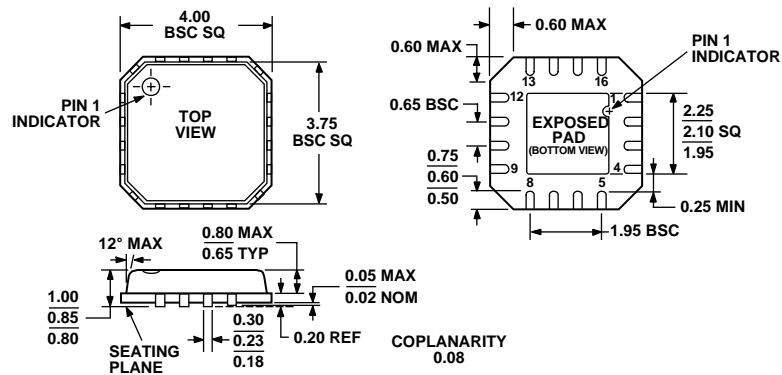
# OUTLINE DIMENSIONS
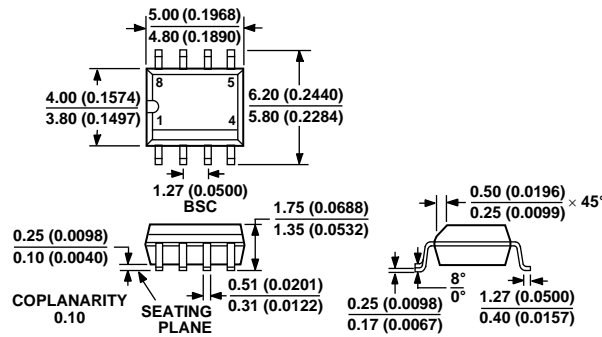


COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

*Figure 50. 8-Lead Standard Small Outline Package [SOIC_N]*
*Narrow Body*
*(R-8)*
*Dimensions shown in millimeters and (inches)*



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC

*Figure 51. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]*
*4 mm × 4 mm Body, Very Thin Quad*
*(CP-16-4)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD8557AR | -40°C to +125°C | 8-Lead SOIC | R-8 |
| AD8557AR-REEL | -40°C to +125°C | 8-Lead SOIC | R-8 |
| AD8557AR-REEL7 | -40°C to +125°C | 8-Lead SOIC | R-8 |
| AD8557AR-EVAL | | Evaluation Board | |
| AD8557ACP-R2 | -40°C to +125°C | 16-Lead LFCSP | CP-16 |
| AD8557ACP-REEL | -40°C to +125°C | 16-Lead LFCSP | CP-16 |
| AD8557ACP-REEL7 | -40°C to +125°C | 16-Lead LFCSP | CP-16 |

## NOTES

# NOTES

ANALOG
DEVICES

www.analog.com