CERAMIC SMD VOLTAGE CONTROL CRYSTAL OSCILLATOR

5.0 x 7.0 x 1.8mm

APVV SERIES : PRELIMINARY

FEATURES:

- CMOS, PECL or LVDS Output
- Sub 1pS (12kHz - 20MHz)
- Low Jitter
- Low Power (2.5, 3.3V)
- Wide Pull Range

APPLICATIONS:

- SONET, Fiber Channel, SERDES HDTV, OBSAI, CPRI, PCI Express, 1394

STANDARD SPECIFICATIONS: PARAMETERS

Frequency Range	38 MHz to 640 MHz
Operating Temperature	0°C to + 70°C (see options)
Storage Temperature	-55°C to +125°C
Frequency Pull Range	± 50 ppm (see options)
Pull Range Linearity	10% Max
Overall Frequency Stability	± 50 ppm max. (see options)
Supply Voltage (Vdd)	2.25V to 3.63 (2.5V to 3.3V ± 10%)
Phase Jitter RMS (12KHz-20MHz)	0.5pS Typ, 1pS Max
Period Jitter (peak to peak)	20pS typ., 30pS max up to 320 MHz; 50pS typ., 70pS max 321MHz to 640MHz
Tri-State Function	***For CMOS and LVDS*** = "1" (VIH ³ 0.7* Vdd) or open: Oscillation; "0" (VIL < 0.3* Vdd): No oscillation/Hi Z ***For PECL (See TriState Pin Operation table) = P Option (Standard PECL OE)*** "0" (VIL < 0.3* Vdd): or Open: Oscillation; "1" (VIH ³ 0.7* Vdd): No oscillation/Hi Z ***P1 Option*** = "1" (VIH ³ 0.7* Vdd) or open: Oscillation; "0" (VIL < 0.3* Vdd): No oscillation/Hi Z
PECL	
Supply Current (I_{DD})	65mA max (for 38MHz<Fo≤320MHz), 90mA max (320MHz<Fo<640MHz)
Symmetry (Duty Cycle)	45% min, 50% typical, 55% max.
Output Logic High	V_{DD} -1.025V min, V_{DD} -0.880V max.
Output Logic Low	V_{DD} -1.810V min, V_{DD} -1.620V max.
Rise time	1.5ns max, 0.6nSec typical
Fall time	1.5ns max, 0.6nSec typical
CMOS	
Supply Current	30mA max (38MHz<Fo<320MHz)
Symmetry (Duty Cycle)	45% min, 50% typ, 55% max,
Rise/ Fall Time	(0.3V ~ 3.0V w/15 pF load) 0.7nS Typ.; (20%-80% w/50Ω Load) 0.3nS Typ.
LVDS	
Supply Current (I_{DD})	45mA max(for 38MHz<Fo≤320MHz), 70mA max (320MHz<Fo<640MHz)
Output Clock Duty Cycle @ 1.25V	45% min, 50% typical, 55% max
Output Differential Voltage (V_{OD})	247mV min, 355mV typical, 454mV max
VDD Magnitude Change (ΔV_{OD})	-50mV min, 50mV max
Output High Voltage	V_{OH} = 1.6V max, 1.4V typical
Output Low Voltage	V_{OL} = 0.9V min, 1.1V typical
Offset Voltage [R_L = 100Ω]	V_{OS} = 1.125V min, 1.2V typical, 1.375V max
Offset Magnitude Voltage[RL = 100Ω]	ΔV_{OS} = 0mV min, 3mV typical, 25mV max
Power-off Leakage (I_{OXD}) [Vout=VDD or GND, VDD=0V]	±10µA max, ±1µA typical
Differential Clock Rise Time (t_r) [R_L=100Ω, CL=10pF]	0.7ns typical, 1.0ns max
Differential Clock Fall Time (t_f) [R_L=100Ω, CL=10pF]	0.7ns typical, 1.0ns max

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PIN ASSIGNMENTS:

PIN #	NAME	DESCRIPTION
1	Voltage Control	Voltage Control Input
2	OE	Output Enable
3	GND	Ground
4	Q	PECL, LVDS, or CMOS Output
5	$\overline{Q}$	Complimentary PECL, LVDS, or NC
6	V_{DD}	VDD Connection

TRI-STATE PIN OPERATION:

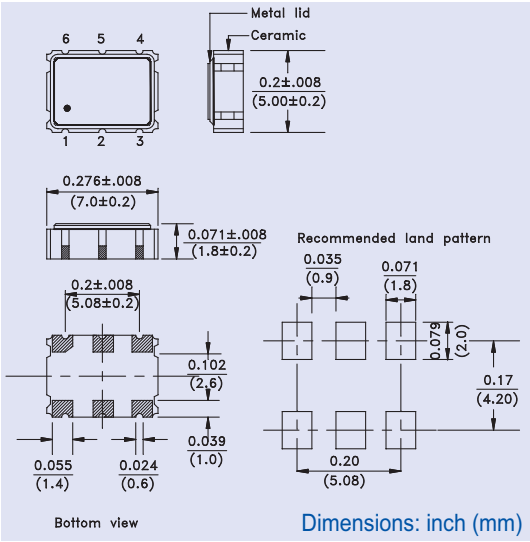
OUTPUT TYPE	PIN 1 LOGIC LEVEL*	OUTPUT STATE
PECL (P)	0 (Default)	Enabled
	1	Tri-state
LVDS & CMOS (V, C)	0	Tri-state
	1 (Default)	Enabled
PECL1 (P1)	1 (Default)	Enabled
	0	Tri-state

*Connect to VDD from logic level "1", connect to ground for logic level "0".

MARKING:

- HTU.th (Frequency: H=First “”100” digit of frequency (if applicable), T=First “10” digit of frequency, U=First “unit” of frequency, t=First “tenth” digit of freq, h=First “hundredth” digit of freq. Ex: 156.25 for 156.25MHz; 14.31 for 14.31818 MHz)
- APVV ZYX (Z: Month, A to L; Y: Year, 5 for 2005; X: Traceability Code)

OUTLINE DRAWING:



OPTIONS AND PART IDENTIFICATION (Left blank if standard):

APVV - Frequency - Temperature - Frequency Stability - Output - Pull Range - Packaging

Temperature:
L for -40°C to +85°C

Stability options:
R for ± 25 ppm max
S for ± 20 ppm max

Output options:
P = PECL
P1 = PECL1
V = LVDS
C = CMOS

Pull Range: **A** = ±100ppm

Packaging option: **T** for Tape and Reel (1,000pcs/reel)

Q1 2006 Availability currently limited to standard developed frequencies.
Please contact factory for more information.

ABRACON CORPORATION

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