DCL Digital Cell Library

IMP's Digital Cell Library (DCL) is designed to be compatible with IMP's Analog Cell Library (ACL). The dual layer metal, silicon gate CMOS Standard Cells offer high performance with low power consumption and high noise margins. The Digital Core Cells within each library offer equal input capacitance for easy calculation of internal circuit loading and rapid determination of drive requirements. IMP's Digital Pad Cells have been designed to minimize switching noise. They equalize input rise and fall delays thus providing consistent time response for TTL compatible signals.

The 3μ Digital Cell Library (DCL3) and the 2μ Digital Cell Library (DCL2) are designed in a single- or dual-poly, dual metal, P-well CMOS process. The 1.2μ Digital Cell Library (DCL1.2) is designed in a single- or dual-poly, dual-metal N-well CMOS process. The DCL3 cells are intended primarily for use with the ACL3 Analog Library at 10V (±10%). The DCL2 and the DCL1.2 cells are designed to operate at 5V (±10%). However, all the cells in each of the three libraries, DCL3, DCL2 and DCL1.2 can be operated at voltages as low as 2.5V with reduced performance.

The Digital Standard Cell Libraries, DCL3, DCL2 and DCL1.2, consist of three basic cell types: 1) Core, 2) Level translators, and 3) Pad. All cells are a fixed height, variable width design. The core cells are drawn and the interconnect is routed on a coarse grid. This feature simplifies placement and routing and eliminates the possibility of design rule violations being created during layout.

Core Cell layout has been done using IMP's Proprietary Cell Assembler (CASS). A GDS-II version of the cell layouts is normally generated.

Core Cells

Core Cells are the gates, flip-flops, MSI functions, amplifers, etc. that are used to accomplish the desired circuit function. V_{DD} and V_{SS} are routed horizontally in metal-1 through the cell near the top and bottom, and analog V_{DD} is routed in metal-1 below each cell to make separate substrate connections.

Pad Cells

Pad Cells are used to interface the core circuits to the outside world. Included in these cells are input buffers, output buffers, I/O buffers, power pads, etc. There are several types of pad cells for each input or output function. The pad router is a gridless router and can handle pad cells of variable sizes, for maximum packing densities. In general, the cells make possible a die with pads placed at a minimum spacing of 200 micron. Exceptions to this include the larger output buffers and the I/O buffers.

V_{DD} and V_{SS} are routed horizontally through each pad cell in metal-2. The widths of these power lines can be varied to match the current required by numerous banks of core cells as well as the pad cells. Unlike the core cells, the signal I/O is routed into or out of the cell in metal-1. However, the pad cells signal I/O is found only on the interior side of the cell.

Data Sheet Overview

For each Standard Cell circuit, there is a data sheet that contains all the information required to use the cell in an IC design. Included are:

- The *CELL NAME*.
- A brief description of the cell *FUNCTION* and/or *FEATURES*.
- The *SILOS SYNTAX* used to call the cell in the SILOS circuit description.
- A *TRUTH TABLE* description of the cell's logical function.
- A table of the *CAPACITIVE LOADS* presented by each of the cell's inputs. Capacitance information for tri-state cell outputs is also given. This data is used during timing analysis.
- A *LOGIC SYMBOL* drawing (to ensure standardized logic schematics).
- A table summarizing the cell's *AC PARAMETERS*. Data is included for best case and worst case. Derating tables are provided to make it possible to tailor this data for specific application environments.
- A *CIRCUIT SCHEMATIC* of the cell, which is included for all complex cells.

ACL Analog Cell Library

IMP's Analog Cell Library (ACL) is designed to be compatible with IMP's Digital Cell Library (DCL). The dual-poly, dual metal, silicon gate CMOS Standard Cells offer high performance with low power consumption and high noise margins.

The 3μ Analog Cell Library (ACL3) and the 2μ Analog Cell Library (ACL2) are designed in a double-poly, single-metal, P-well CMOS process. The 1.2μ Analog Cell Library (ACL1.2) is designed in a double-poly, single-metal N-well CMOS process. The ACL3 Library Cells are intended primarily for use with the DCL3 Digital Cell Library at 10V (±10%). The ACL2 Standard Cells are designed to operate at 5V (±10%). Many of the cells in the libraries can be operated at 2.5V with reduced performance.

The ACL cells are a fixed height, variable width design. The cells are drawn and the interconnect is routed on a coarse grid. This feature simplifies placement and routing and eliminates the possibility of design rule violations being created during layout.

The cells are designed such that when they are abutted and interconnect is placed on a grid, no design rule violations occur. A GDS-II version of the cell layouts is generated for use with STREAM-type systems.

Analog Cells

The Analog Cells are the comparators, voltage references, amplifiers, etc. that are used to accomplish the desired circuit function. GND, V_{DD} and V_{SS} are routed horizontally in metal-1 through the cell near the top and bottom. All signal input and output lines enter or exit the cell along both the top and bottom.

Data Sheet Overview

For each Standard Cell circuit, there is a data sheet that contains all the information required to use the cell in an IC design. Included are:

- The *CELL NAME*.
- A brief description of the cell *FUNCTION* and/or *FEATURES*.
- A *BLOCK DIAGRAM* drawing.
- A table summarizing the cell's *AC* and *DC PARAMETERS*. Data is included for best, typical, and worst case.

Cell Library Electrical Parameters

T-42-21

ACL3 and DCL3

Electrical Parameters (+25°C unless otherwise noted)

Process: Dual poly, Dual Metal P-well Silicon Gate CMOS

DESCRIPTION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Minimum geometry		3.0			micron
Operating voltage	V_{CC}	9.0[1]	10.0	11.0	volt
Absolute maximum voltage	V_{MAX}			12.0	volt
Junction depth	xj (N+)	0.4	0.5	0.6	micron
Junction depth	xj (P+)	0.6	0.75	0.9	micron
P-well depth	xj (pw)	3.0	4.0	5.0	micron
Gate oxide thickness	T_{OX}	44.0	48.0	52.0	nm

Note 1: This is the standard operating range. Lower operating voltages are possible, depending on the particular circuit design.

ACL2 and DCL2

Electrical Parameters (+25°C unless otherwise noted)

Process: Dual poly, Dual Metal P-well Silicon Gate CMOS

DESCRIPTION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Minimum geometry		2.0			micron
Operating voltage	V_{CC}	3.75	5.0	5.5	volt
Absolute maximum voltage	V_{MAX}			8.0	volt
Junction depth	xj (N+)		0.35		micron
Junction depth	xj (P+)		0.35		micron
P-well depth	xj (pw)	3.0	3.5	4.0	micron
Gate oxide thickness	T_{OX}	32.5	35.0	35.7	nm

Note 1: This is the standard operating range. Lower operating voltages are possible, depending on the particular circuit design.

Cell Library Electrical Parameters *(cont.)*

ACL1.2 and DCL1.2

Electrical Parameters (+25°C unless otherwise noted)

Process: Dual poly, Dual Metal N-well Silicon Gate CMOS

DESCRIPTION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Minimum geometry		1.2			micron
Operating voltage	V_{CC}	3.75[1]	5.0	5.5	volt
Absolute maximum voltage	V_{MAX}			8.0	volt
Junction depth	xj (N+)		0.30		micron
Junction depth	xj (P+)		0.30		micron
N-well depth	xj (pw)	3.0	3.5	4.0	micron
Gate oxide thickness	T_{OX}	22.5	25.0	27.5	nm

Note 1: This is the standard operating range. Lower operating voltages are possible, depending on the particular circuit design.