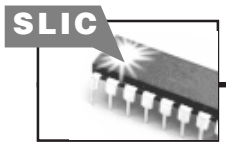
APPLICATION NOTE AND DEVELOPMENT SYSTEM
AVAILABLE
AN65 • LAPKIT DEMO



LapKit™ X88C75 SLIC® E² Microperipheral

Port Expander and E² Memory

FEATURES

- **Highly Integrated Microcontroller Peripheral**
  - **—8K x 8 E² Memory**
  - **—2 x 8 General Purpose Bidirectional I/O Ports**
  - **—16 x 8 General Purpose Registers**
  - **—Integerated Interrupt Controller Module**
  - **—Internal Programmable Address Decoding**
- **Concurrent Read During Write**
  - **—Dual Plane Architecture**
- **Isolates Read/Write Functions Between Planes**
- **Allows Continuous Execution Of Code From One Plane While Writing In The Other Plane**
- **Multiplexed Address/Data Bus**
  - **—Direct Interface to Popular 80C51 Family of Microcontrollers**
- **Software Data Protection**
  - **—Protect Entire Array During Power-up/-down**
- **Block Lock™ Data Protection**
  - **—Set Write Lockout in 1K Blocks**
- **Toggle Bit Polling**
- **High Performance CMOS**
  - **—Fast Access Time, 120 ns**
  - **—Low Power**
    - **60mA Active**
    - **100µA Standby**
- **PDIP, PLCC, and TQFP Packaging Available**

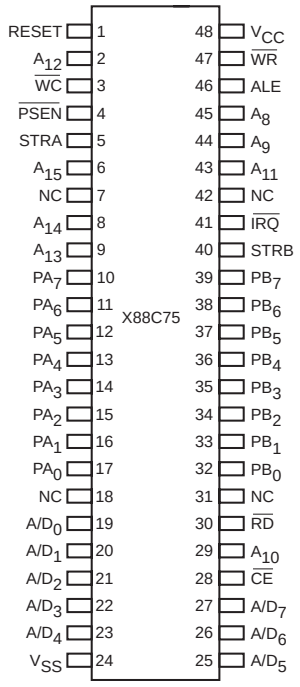
DESCRIPTION

The X88C75 SLIC is a highly integrated peripheral for the 80C51 family of microcontrollers. The device integrates 8K-bytes of 5V byte-alterable nonvolatile memory, two bidirectional 8-bit ports, 16 general purpose registers, programmable internal address decoding and a multiplexed address and data bus.

The 5V byte-alterable nonvolatile memory can be used as program storage, data storage, or a combination of both. The memory array is separated into two 4K-bytes sections which allows read accesses to one section while a write operation is taking place in the other section. The nonvolatile memory also features Software Data Protection to protect the contents during power transitions, and an advanced Block Protect register which allows Individual blocks of the memory to be configured as read-only or read/write.

PIN CONFIGURATIONS

DIP



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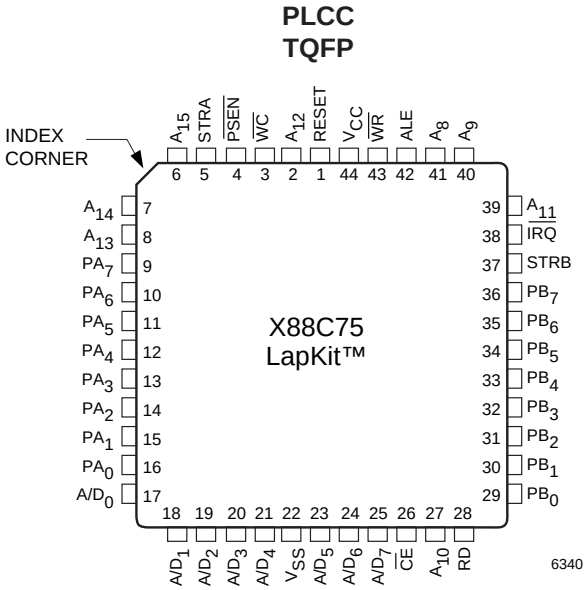
PLCC
TQFP



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Each bidirectional port consists of 8 general purpose I/O lines and 1 data strobe line. The ports also feature a configurable interrupt request output.

Access to the X88C75 is accomplished through the multiplexed address/data bus of the 80C51 type controllers. An internal programmable address decoder maps the internal memory and register locations into the desired address space.

ARCHITECTURAL OVERVIEW

The X88C75 incorporates the interface circuitry normally needed to decode the control signals and demultiplex the address/data bus to provide a “seamless” interface.

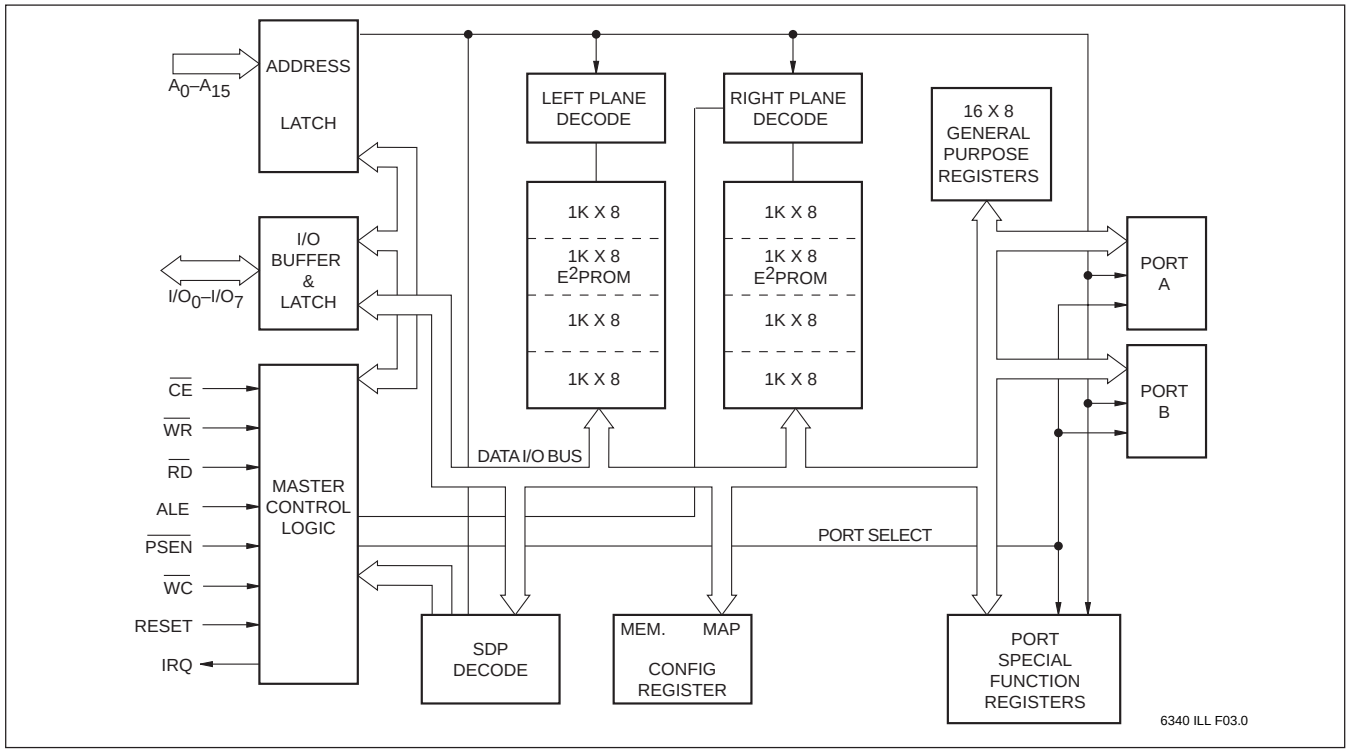
The control inputs on the X88C75 are configured such that it is possible to directly connect them to the proper interface signals of the 80C51 microcontroller. The reading of data from the chip is controlled either by the $\overline{PSEN}$ or the $\overline{RD}$ signal, which essentially maps the X88C75 into both the Program and the Data Memory address map.

Reading and writing of the nonvolatile memory array is analogous to RAM operation. During a write operation to either the nonvolatile memory or the control registers, ALE latches the address to be written into the X88C75. The rising edge of $\overline{WR}$ latches the data to be written.

The nonvolatile memory of the X88C75 is internally organized as two independent arrays of 4K-bytes with the A12 input selecting which of the two planes of memory is to be accessed. While the processor is executing code out of one plane, write operations can take place in the other plane; allowing the processor to continue execution of code out of the X88C75 during a byte or page write to the device. This feature is called Concurrent Read During Write.

The X88C75 also features an advanced implementation of the Software Data Protection scheme, called Block Lock Protect, which allows the nonvolatile memory array to be treated as 8 independent sections of 1K-bytes. Each of these sections can be independently enabled for write operations. This allows segmentation of the memory contents into writable and non-writable sections, thereby, allowing certain sections of the device to be secured so that updates can only occur in a controlled environment. (e.g. in an automotive application, only at an authorized service center). The Block Protect configuration is stored in a nonvolatile register, ensuring that the configuration data will be maintained after the device is powered-down.

FUNCTIONAL DIAGRAM



The X88C75 write control input, serves as an external control over the completion of a previously initiated page load cycle.

The X88C75 also features the industry standard 5V E² memory characteristics such as byte or page mode write and Toggle Bit Polling.

Read

A HIGH to LOW transition on ALE latches the address; the data will be output on the AD pins after either $\overline{RD}$ or $\overline{PSEN}$ goes LOW (t_{RDLV}).

Write

A write is performed by latching the addresses on the falling edge of ALE. The $\overline{WR}$ is strobed LOW followed by valid data being presented on the AD_0–AD_7 pins. The data will be latched into the X88C75 on the rising edge of $\overline{WR}$.

Page Write Operation

The X88C75 supports page mode write operations. This allows the microcontroller to write from one to thirty-two bytes of data to the X88C75. Each individual write within a page write operation must conform to the byte write timing requirements. The falling edge of $\overline{WR}$ starts a timer delaying the internal programming cycle 100µs: therefore, each successive write operation must begin within 100µs of the last byte written. The waveform on page 4 illustrates the sequence and timing requirements.

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
RESET	I	RESET is used to initialize the internal static registers and has no effect on the E² memory operations. The default active level is HIGH, but it can be reconfigured in EEM register.
$\overline{PSEN}$	I	Content of E² memory can be read by lowering the $\overline{PSEN}$ and holding both $\overline{RD}$ and $\overline{WR}$ HIGH. The device then places on the data bus (AD_7–AD_0) the contents of E² memory at the latched address.
STRA, STRB	I/O	The STRA controls port A and STRB controls port B. When ports are configured as inputs, a valid transition on their strobe pins will latch into their port data register the data present at the port input pins. Writing to an output port data register generates a pulse of fixed duration on its corresponding strobe pin. The output data presented at the output pins stay valid until the next data is written to the output port data register.
PA_7–PA_0	I/O	The I/O lines of port A. The output driver can be configured as either CMOS or open-drain using the AWO bit in CR. The I/O direction bit (DIRA) in CR is used to select port A I/O mode.
PB_7–PB_0	I/O	The I/O lines of port B. The output driver can be configured as either CMOS or open-drain using the BWO bit in CR. The I/O direction bit (DIRB) in CR is used to select port B I/O mode.
A_{15}–A_8	I	Non-multiplexed high-order Address Bus inputs for the upper byte of the address.
AD_7–AD_0	I/O	Multiplexed low-order Address and Data Bus. The addresses are latched when ALE makes a HIGH to LOW transition.
$\overline{WR}$	I	During a byte/page write cycle $\overline{WR}$ is brought LOW while $\overline{RD}$ is held HIGH and the data is placed on the Data Bus. The rising edge of $\overline{WR}$ will latch the data into the device.
$\overline{RD}$	I	The $\overline{RD}$ input is active LOW and is used to read content of either the E² memory or the SFR at the latched address. Both $\overline{PSEN}$ and $\overline{WR}$ signals must be held HIGH during $\overline{RD}$ controlled read operation.
$\overline{IRQ}$	O	The $\overline{IRQ}$ is an open-drain output. It can be configured to signal latching of new data into any of the ports, and/or completion of the E² memory internal write cycle.
$\overline{WC}$	I	$\overline{WC}$ input has to be held LOW during a write cycle. It can be permanently tied HIGH in order to disable write to the E² memory. Taking the $\overline{WC}$ HIGH prior to t_{BIC} (100µs; the time delay from the last write cycle to the start of internal programming cycle) will inhibit the write operation.
$\overline{CE}$	I	The device select ($\overline{CE}$) is an active LOW input. This signal has to be asserted prior to ALE HIGH to LOW transition in order to generate a valid internal device select signal. Holding this pin HIGH and ALE LOW will place the device in standby mode. The ports stay active at all times.
ALE	I	Address Latch Enable input is used to latch the addresses present on the address lines A_{15}–A_8 and AD_7–AD_0 into the device. The addresses are latched when ALE transitions from HIGH to LOW.

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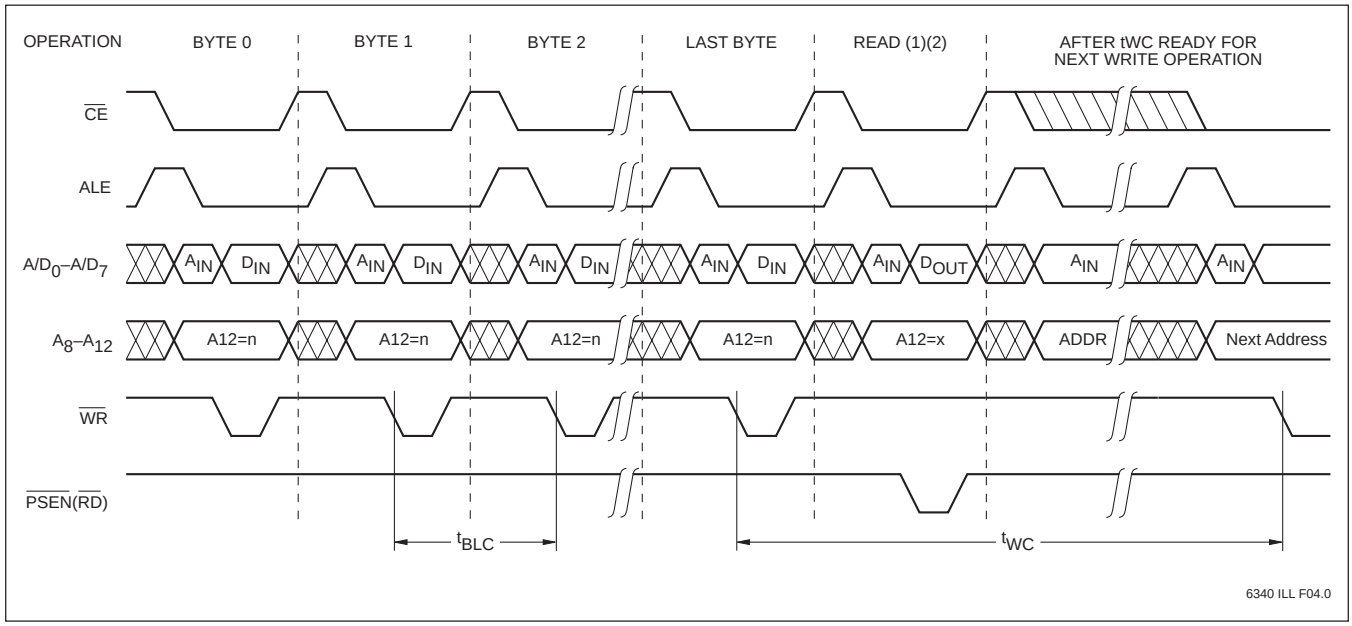
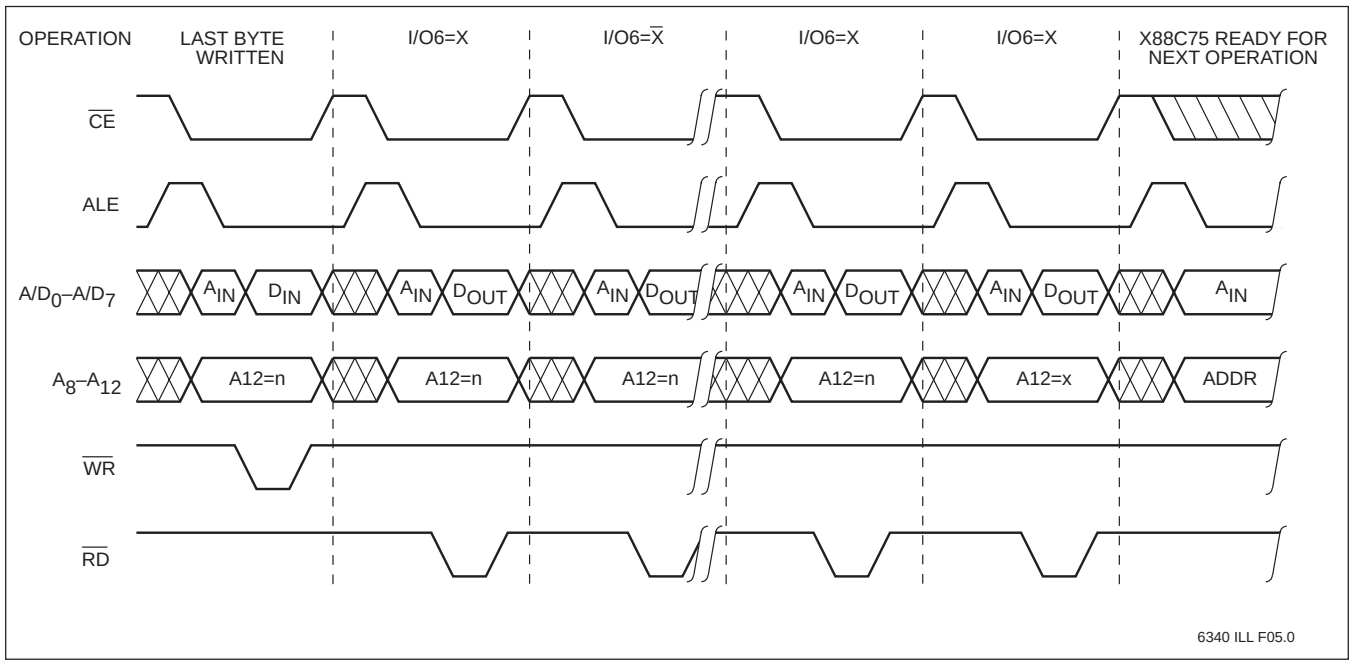
Figure 1. Page Write Operation



Toggle Bit Polling

Because the X88C75 typical write timing is less than the specified 5ms, Toggle Bit Polling has been provided to determine the early completion of a write cycle. During the internal programming cycle, I/O_6 will toggle from "1" to "0" and "0" to "1" on subsequent attempts to read from the memory plane that is being updated. When the internal cycle is complete, the toggling will cease and the device will be accessible for additional read or write operations. Due to the dual plane architecture, reads for polling must occur from the plane that was written; that is, the state of A_{12} during a write must match the state of A_{12} during polling.

Figure 2. Toggle Bit Polling



DATA PROTECTION

The X88C75 provides two levels of data protection through software control. There is a global software data protection feature similar to the industry standard for E²PROMs and a new Block Lock Protect write lockout protection providing a secondary level data security option.

Software Data Protection

Software Data Protection (SDP) can be employed to protect the entire array against inadvertent writes during power-up/power-down operations. The X88C75 is shipped from the factory with SDP enabled. With SDP enabled, inadvertent attempts to write to the X88C75 will be blocked.

The system can still write data, but only when the write operation (page or byte) is preceded by the three-byte command sequence. All write operations, both the command sequence and any data write operations must conform to the page write timing requirements.

The SDP mode is also enabled anytime one of the nonvolatile configuration registers are modified. These include writing to EE map, SFR map, and BPR.

Figure 3. Writing With SDP Enabled

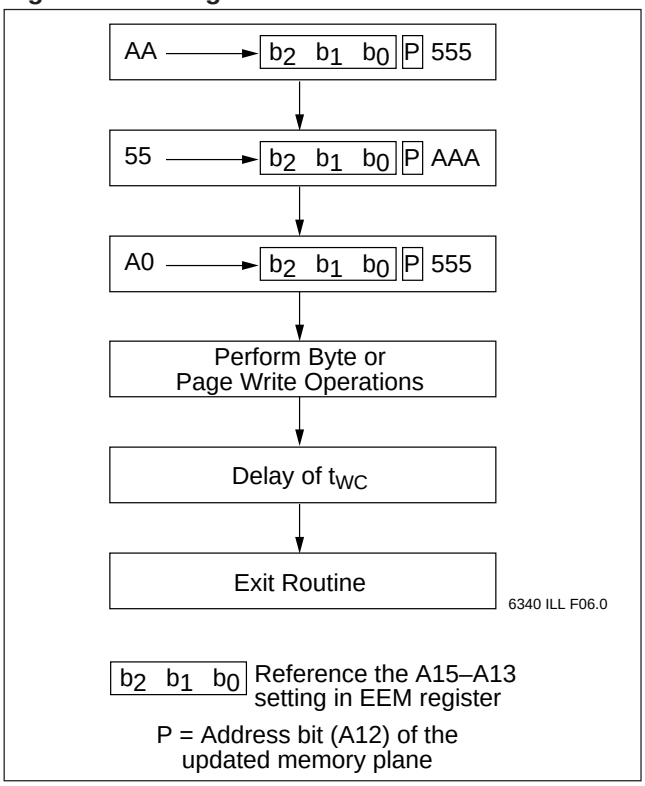
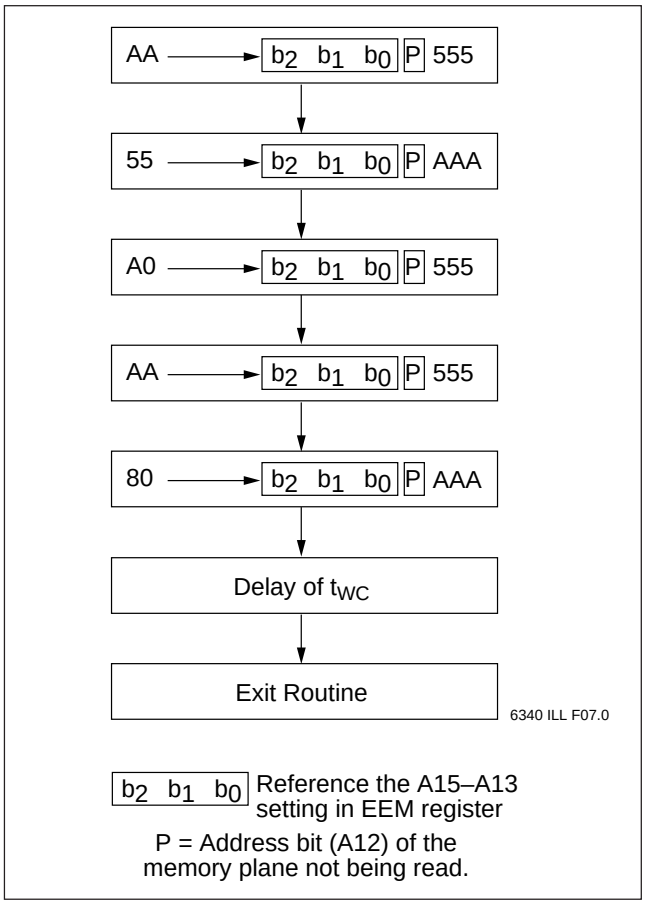


Figure 4. Sequence to Deactivate Software Data Protection



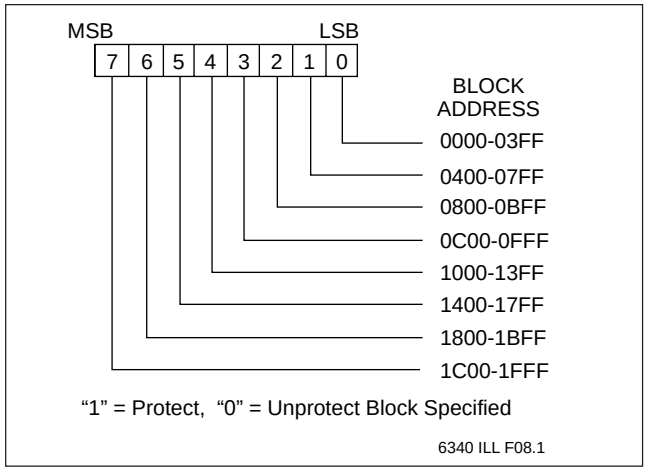
Block Lock Protect Write Lockout

The X88C75 provides a second level of data security referred to as Block Lock Protect write lockout (or Block Protect). This is accessed through an extension of the SDP command sequence. Block Protect allows the user to lockout writes to 1K x 8 blocks of memory. Unlike SDP which prevents inadvertent writes, but still allows easy system access to writing the memory, Block Protect will lockout all attempts unless it is specifically disabled by issuing the deactivation sequence. This feature can be used to set a higher level of protection in a system where a portion of the memory is used to store the system kernel and protect it from the application programs residing in the other blocks.

Setting write lockout is accomplished by writing a five-byte command sequence opening access to the Block Protect Register (BPR). After the fifth byte is written, the user writes to the BPR, selecting which blocks to protect or unprotect. All write operations, both the command sequence and writing the data to the BPR, must conform

to the page write timing requirements. It should be noted that accessing the BPR automatically sets the upper level SDP. If for some reason the user does not want SDP enabled, they may reset it using the normal reset command sequence. This will not affect the state of the BPR and any 1K x 8 blocks that were set to the write lockout state will remain in the write lockout state.

Figure 5. Block Protect Register Format



The BPR format and block map are illustrated above. The command sequence is illustrated to the right.

Figure 6. Setting BPR Command Sequence

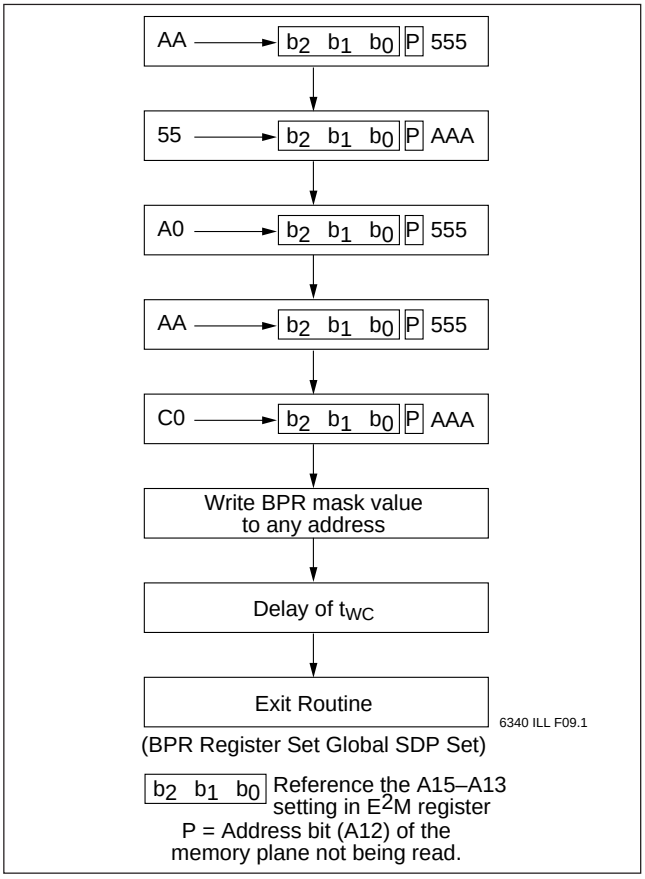


Figure 7. Microcontroller Map

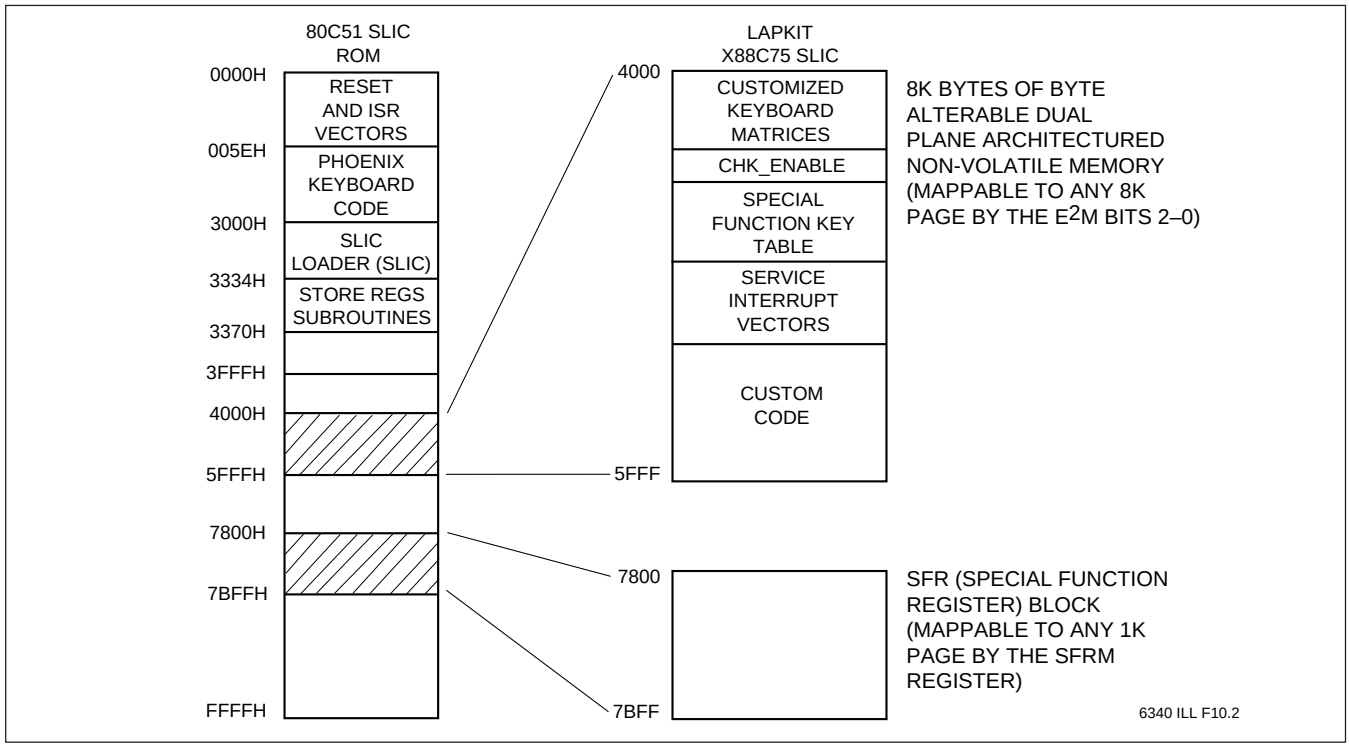
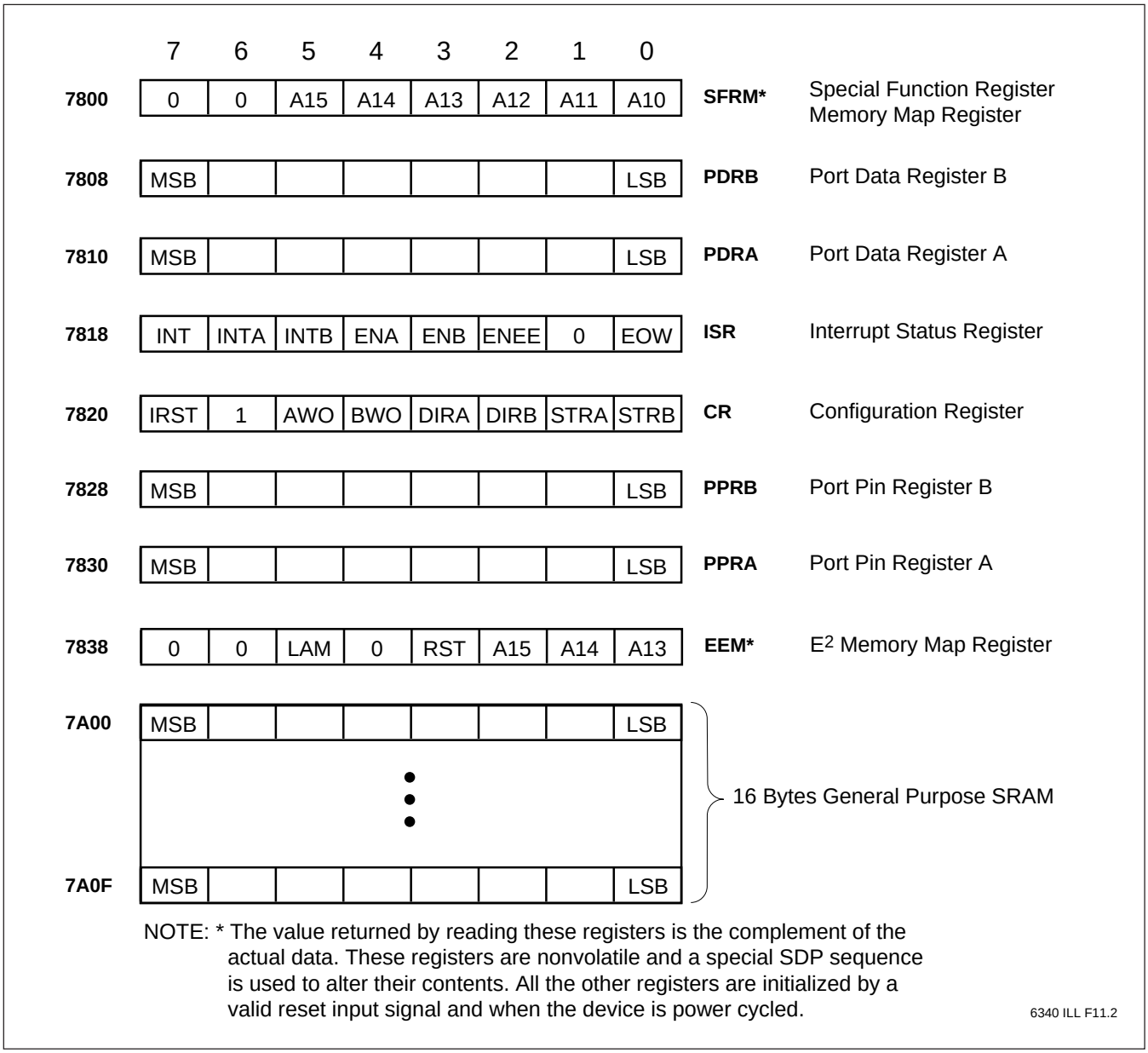


Figure 8. On Chip Registers



NOTE: * The value returned by reading these registers is the complement of the actual data. These registers are nonvolatile and a special SDP sequence is used to alter their contents. All the other registers are initialized by a valid reset input signal and when the device is power cycled.

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Programmable Address Decoding

The X88C75 features an internal programmable address decoder which allows the nonvolatile memory array and the internal registers to be mapped in various locations of the 64K-byte memory map. The register set is mappable into a 1K-byte block, while the nonvolatile memory array is mappable into an 8K-byte block. The mapping is controlled by two nonvolatile configuration registers, the SFR Map Register and the E² Memory Map Register. Their bits are mapped as follows:

SFR Map Register (SFRM) **Default = 1E**

7	6	5	4	3	2	1	0
0	0	A15	A14	A13	A12	A11	A10

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A15-A10

The A15-A10 are upper address bits for the 1K-byte page where the SFR memory is mapped.

BITS 7:6

Setting these two bits to any combination other than “00” or “11” will interfere with device proper operation.

E² Memory Map Register (EEM) Default = 0A

7	6	5	4	3	2	1	0
0	0	LAM	0	RST	A15	A14	A13

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A15-A13

Modifying these three bits changes the location of the program memory within the address map.The A15-A13 correspond to the upper three address bits of the 8K-byte page where program memory will be mapped.

RST

The RST bit controls the polarity of the RESET input pin.

“0” = RESET is Active LOW
“1” = RESET is Active HIGH

LAM

Port B can be configured as either a general purpose I/O port (normal I/O mode), or latched address mode (LAM). The LAM option programs port B to output the demultiplexed low order byte of the address latched into the X88C75 by ALE. The LAM bit selects between these two modes.

“0” = PORT B is I/O Port
“1” = Port B outputs low address byte (A7-A0)

Setting the Mapping Registers

The mapping registers are written using a modified version of the Software Data Protection sequence. All timings must adhere to the normal Software Data Protection sequence.

The complemented contents of the SFR map register and the E² memory map register can be read by the microcontroller at their corresponding SFR addresses. The physical memory location of these registers can be derived by adding the following offset to the SFR base address:

SFR Map Register	00H
E² Memory Map Register	38H

If the regions specified in the map registers overlap, only the SFR will be accessible.

Figure 9. Setting the SFR Map Register

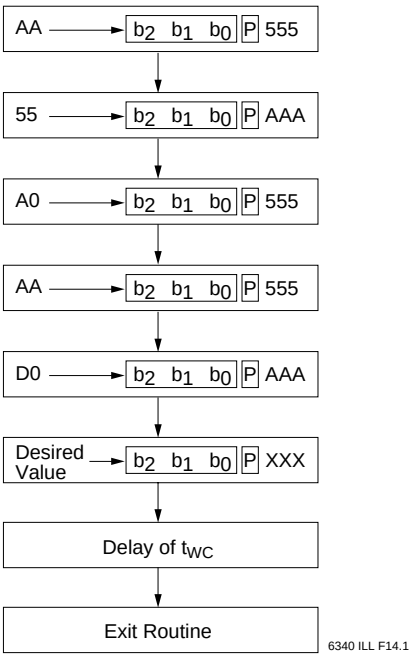
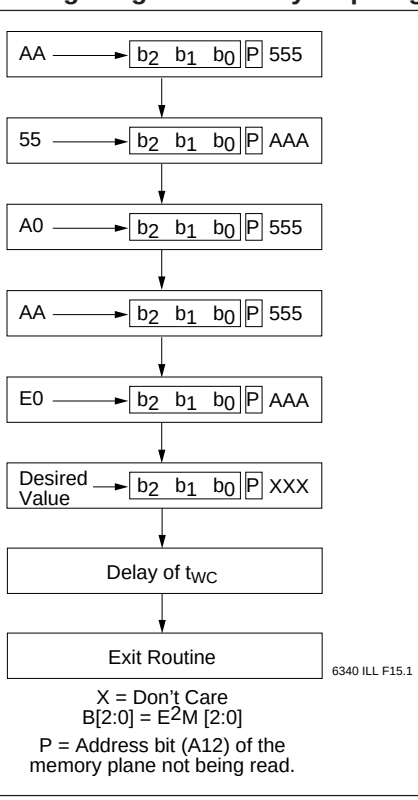


Figure 10. Setting Program Memory Map Register



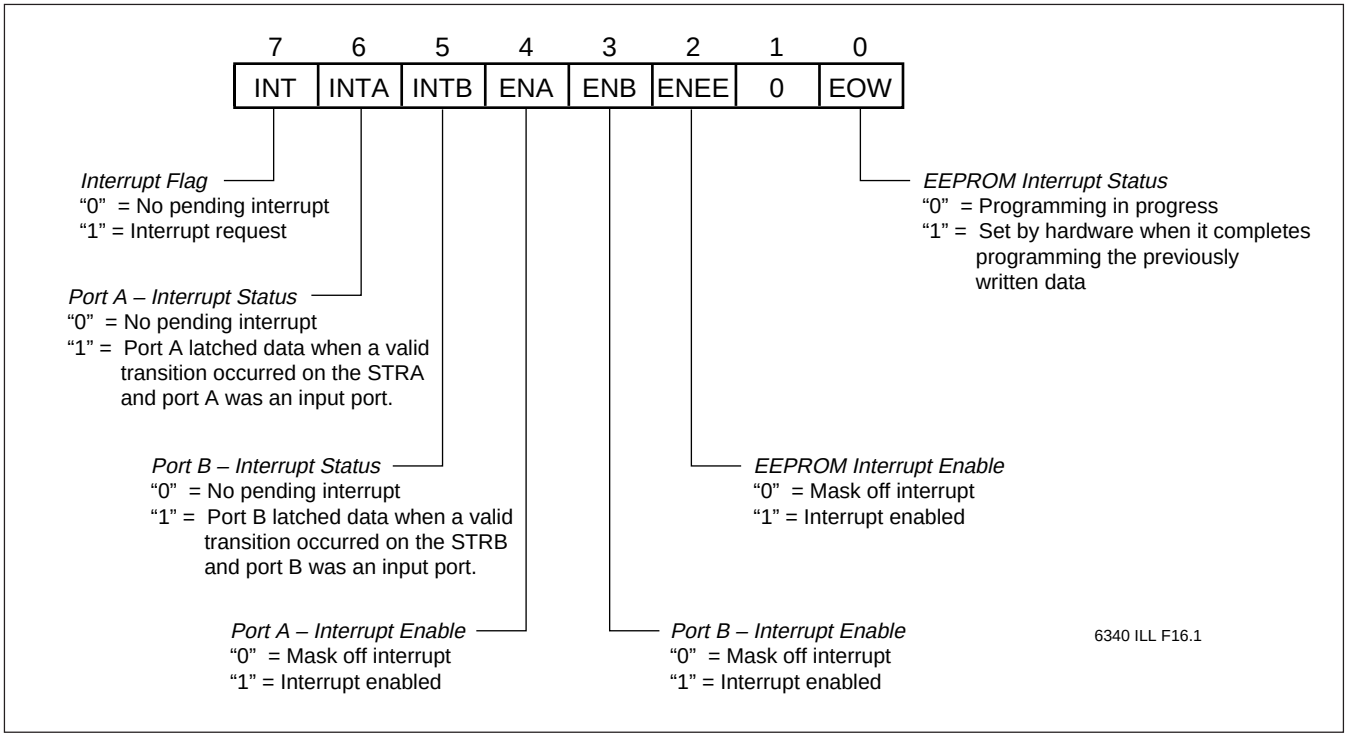
Interrupt Status Register (ISR)

The Interrupt Status Register is a volatile register used to configure the interrupt condition for the I/O ports as well as to determine the interrupt status of the ports. The X88C75 ports can generate an interrupt to the microcontroller upon the proper transition (as specified in the configuration register) on either STRA or STRB pins when the corresponding I/O port is configured as an input.

The INT flag is set when any of the input strobes are toggled provided that their corresponding interrupt enable bits (ENA, ENB) are set. The INT flag is cleared when latched data is read (PDR) or pending interrupt status flag (INTA, INTB) in ISR is forced to "0" by the interrupt service routine. Interrupt service routine should examine the interrupt status flags (INTA, INTB) and identify the source of pending interrupt.

The E² memory interrupt status flag (EOW) is another means to detect the early completion of a write cycle. When ENEE is enabled, the hardware will set the EOW flag, and interrupt the microcontroller at the end of an internal programming cycle. Toggle Bit Polling can be replaced by this hardware interrupt, which reduces the software overhead. The EOW flag should be cleared by software. The interrupt status register bits are mapped as follows.

Figure 11. Interrupt Status Register



Configuration Register (CR)

The Configuration Register is a volatile register used to configure the operation of the I/O ports. The configuration register allows the microcontroller to designate whether each of the two ports is an input or output, what type of output drive is to be used, and what is the polarity of the two strobe lines, STRA and STRB. The bit map of configuration register is shown below.

The IRST bit in the configuration register controls the method used to clear the port interrupt request flags(INTA, INTB). The interrupts are reset by either reading the interrupt source or writing to the Interrupt Status Register. The interrupt must be disabled prior to changing strobe polarity bits(STPA, SPTB), or port direction bits (DIRA, DIRB) in CR. Otherwise, any attempt to modify status of these bits may cause an interrupt to occur.

Port Data Registers (PDR)

The PDRA/PDRB are byte-wide latches which hold port data. When a port is configured as output, the outputs of its PDR latch are connected to the port pins. Writing to PDR generates a pulse on the port strobe pin and latches the data. If a port is configured as an input, the inputs of its PDR latch are connected to the port pins. External data is latched into PDR on the positive edge of its clock. The port strobe input and strobe polarity bit(STPA, STPB) are XORed to generate the PDR input clock.

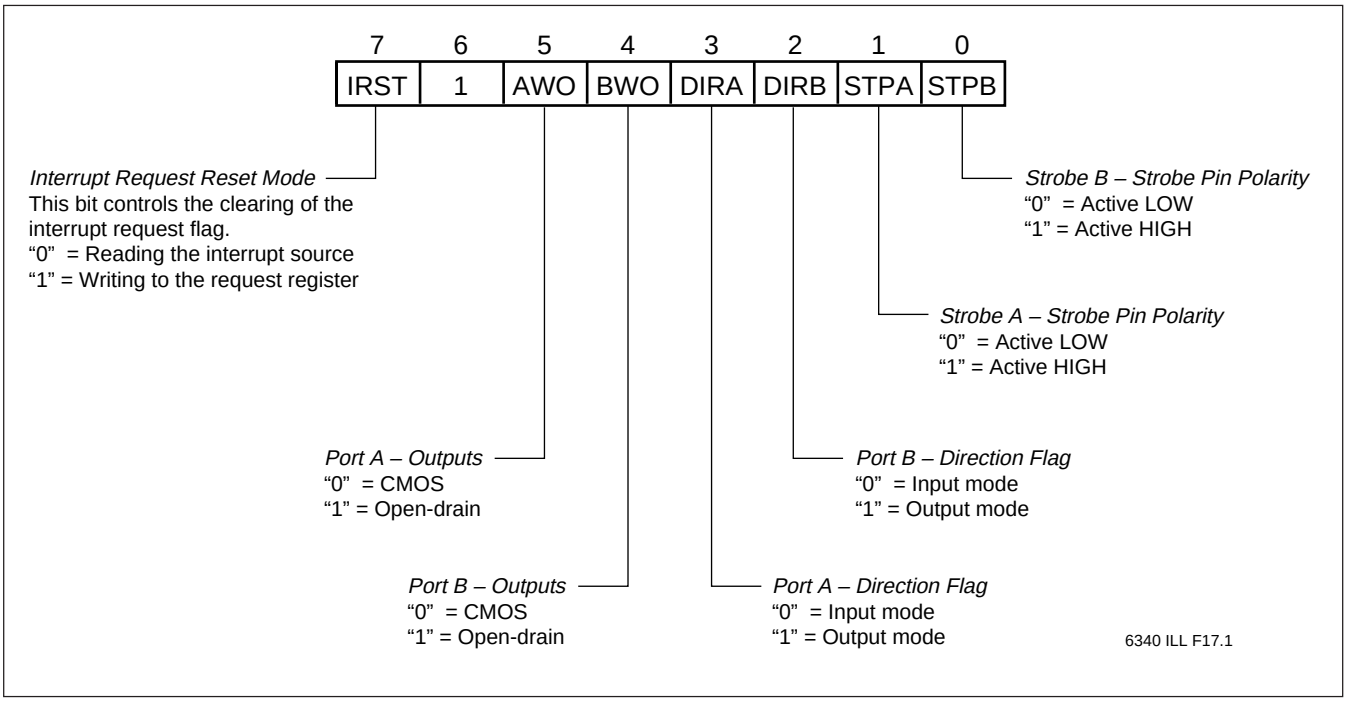
Port Pin Registers (PPR)

The read-only Port Pin Registers are used for reading the current status of the external I/O port pins. Accessing the PPR causes the values on the port pins to be placed on the data bus.

The port direction control bits in configuration register set the direction for the entire port and no control mechanism is provided to program the direction of individual pins. However, the ports have a flexible architecture which allows operating the I/O ports in bidirectional mode using the PPR read feature.

A port can be operated in input/output mode by configuring it as an open-drain output port. The port wire-OR bit (AWO, or BWO in CR) and its port data direction bit (DIRA, or DIRB in CR) should be set to “1”. The PDR bits which correspond to the port pins assigned as inputs should be programmed to “1”. For monitoring the status of the input pins, the PPR can be read. In this application the port strobe pin and the PDR latch are in output mode. In open-drain mode, there are weak internal pull-ups on the port pins, however external pull-ups must be used for proper switching of the I/O lines.

Figure 12. Configuration Register



STATIC RAM BLOCK

There are 16 bytes of volatile static RAM registers mapped to the SFR region. They reside in the 200H-20FH area offset from the SFR base address. Accessing these registers has to be done through external RAM operations for both writes and reads.

PRINCIPLES OF OPERATION

I/O Port Operation

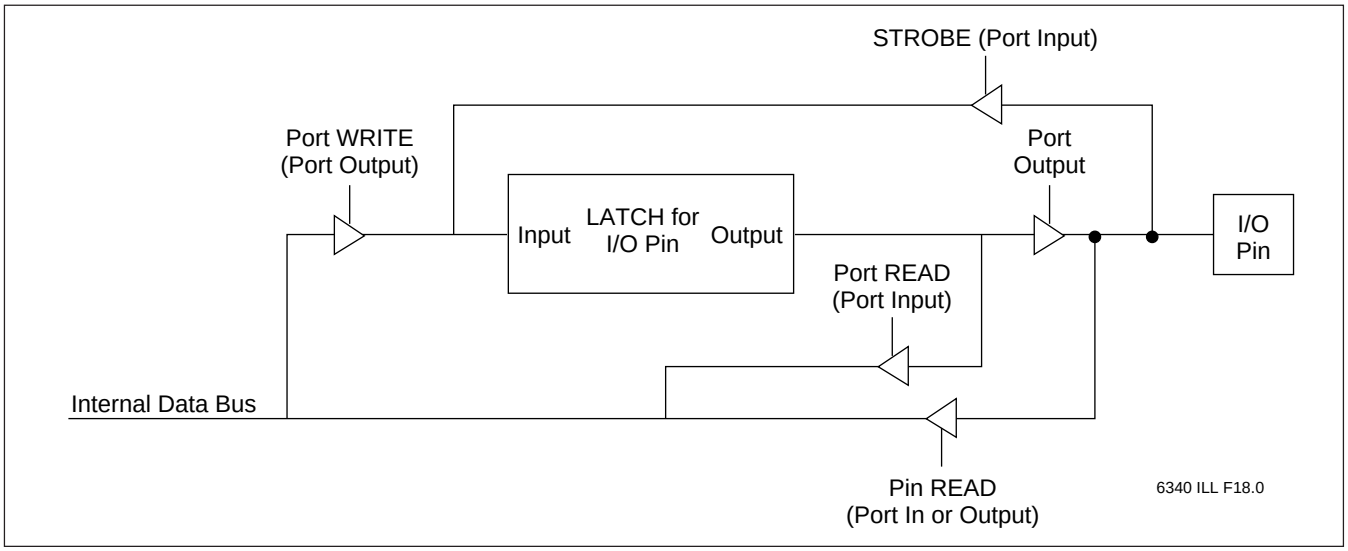
The expansion ports are accessible to the software using their assigned memory mapped addresses. Each port occupies two addresses in the SFR plane, the Port Data Register and Port Pin Register. These registers and their location in the 1K-byte register memory space is shown on page 7.

The ports can be configured as either inputs or outputs, the DIRA and DIRB bits in the configuration register are used to select between the modes. The input signal on the strobe pin, when the corresponding port is configured as an input, is fed to the clock input of the port latch. These are transparent latches and the trailing edge of the strobe pulse is used to latch the data present on the input pins. The strobe signal polarity is configurable using the STPA and STPB bits in the configuration register.

Writing to the port data register of an output port will generate a pulse of fixed duration on its strobe pin. The data also simultaneously arrives at the port output pins. The latched data stays there until new data is written to the port data register. The strobe pulse shape is controlled by the state of the STPA and STPB bits in the configuration register. A “1” forces the valid transition on the corresponding strobe pin as active HIGH ( ), and a “0” sets it to active LOW ( ).

When an external strobe signal is applied to an input port, the latching of input data is followed by the setting of the interrupt flags. The INTA and INTB interrupt flags are used by ports A and B respectively, and are set along with the INT interrupt flag at the end of strobe pulse input. External interrupt ($\overline{IRQ}$) is generated if the interrupt enable flags (ENA and ENB) are set by the software. The former enables the port A interrupt and the latter enables the port B interrupt.

Figure 13. Block Diagram of the I/O Ports



The port output drivers can be either CMOS or open-drain. The wire-OR bits (AWO, BWO) in the configuration register are used to make the selection. When the bits are "0" the CMOS drivers are enabled. Setting these bits will enable the open-drain output drivers. Small pull-up resistors should be used on the pins of open-drain ports.

IRQ

The $\overline{IRQ}$ pin is an active LOW open-drain output. In embedded systems applications, this signal is connected to the microcontroller interrupt input pin through either a direct connection or via an interrupt controller.

Table 1 depicts the three sources of interrupts and their associated flags. Under normal conditions, the INT and port interrupt flags are set, if the port which is configured as an input has its strobe line toggled. If the port interrupt enable flag is set, or gets set while the INT flag is set, then the $\overline{IRQ}$ signal is asserted. The $\overline{IRQ}$ stays valid as long as the interrupt flags are not cleared by the software or the hardware.

Another interrupt source is the End Of Write flag (EOW) which is set by the hardware at the end of every internal programming cycle. The interrupt from this source is controlled by the ENEE bit in ISR. If ENEE is enabled, then EOW can generate an external interrupt. The interrupt is cleared by setting EOW to "0".

Table 1. X88C75 Interrupt Sources

Interrupt Source	Interrupt Enable	Status Flag	INT Flag
PORT A	ENA	INTA	"1"
PORT B	ENB	INTB	"1"
EOW	ENEE	EOW	—

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PORTS A & B INTERRUPTS

The X88C75 features two 8-bit I/O ports which are equipped with a configurable interrupt module. The interrupts are used to signal the reception of new data at an input port data latch. When a port is configured as an output, it can no longer generate any interrupts.

The input port interrupt mechanism is controlled by the external strobe pins (STRA, STRB). Detecting a valid transition on the pin will set the interrupt flags and latch in the input data. The external interrupts from the ports can be masked off using the interrupt enable bits (ENA, ENB) in ISR.

Once an external interrupt is asserted, clearing the interrupt flags will cause the $\overline{IRQ}$ signal to return to its idle state. There are two ways of resetting the interrupt flags. The selection is made using the IRST bit in the configuration register. If IRST is set, then the interrupt flags are cleared by writing "0" to the bit positions corresponding to the interrupt flags (INTA, INTB) in ISR. When the IRST is cleared, reading the PDR automatically clears the interrupt flags.

SOFTWARE CONTROLLED PORT OPERATIONS

The individual clock signals, that control the PDR input latches and load the external data present on the port pins, are generated by XORing the strobe polarity bit and the strobe input of the port. The strobe polarity bits (STPA, STPB) in CR can be used to program the active edge of the strobe inputs. However, if the external strobe input is permanently tied to V_{SS} or V_{CC}, then the strobe polarity bit controls the PDR input latch clock signal.

When a port strobe and its polarity bit have identical logic levels, the corresponding PDR latch is active and any change in the port inputs will show up at the PDR latch outputs. Holding the strobe input at current levels and changing the strobe polarity bit value will generate a positive transition on the PDR clock signal, causing the latch outputs to reflect the previous logic state of the port pins. The clock transition sets the interrupt flags, and if the interrupts have been enabled, then an external interrupt signal will be asserted.

This feature allows the port input operation by permanently tying the STRx inputs to V_{CC} or V_{SS}, and using the STPx bits in CR to control PDR latches. Another advantage of this feature are software generated interrupts. Since the clocking of the PDR latch causes the corresponding port INTx flags to be set, by enabling the interrupts the microcontroller is forced to execute the ISR responsible to service the newly latched data.

END OF WRITE (EOW) INTERRUPT

The internal programming cycle requires several milliseconds for either a single byte write or a page write. The updated memory plane is inaccessible while the programming is in progress. However, the opposite plane is still available for program fetch and data read operations.

The X88C75 has two means of signaling end of an internal programming cycle. In the Toggle Bit Polling technique, the last written byte is successively read. Bit 6 of read data toggles while the programming cycle is still in progress. The software has to continually monitor device responses and determine if it can again access the plane.

In the other method, at the end of an internal programming cycle, the hardware sets the EOW flag. The software can either poll this flag or enable the interrupts by setting the ENEE bit in ISR. Effective use of EOW is made by clearing it prior to initiating a write operation. If the interrupt is enabled, an external interrupt will be asserted at the completion of the internal write cycle. The interrupt is cleared by setting EOW to “0”.

USING A PORT IN BIDIRECTIONAL MODE

In order to use a port in bidirectional mode, it has to be configured as an open drain output port. Small pull-up resistors are required on all port output pins. Bit positions in the Port Data Register corresponding to port inputs should contain “1”. The inputs are then read by accessing PPR. Data is not latched into the device, so the inputs must stay valid throughout the read cycle. The port strobe pin is configured as an output and cannot be used as port latch clock input.

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
- X88C75 ..... –10°C to +85°C
- X88C75I ..... –65°C to +135°C

Storage Temperature ..... –65°C to +150°C

Voltage on any Pin with
- Respect to V_{SS} ..... –1V to +7V

D.C. Output Current 5mA

Lead Temperature
- (Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

6340 PGM T03.1

Supply Voltage	Limits
X88C75	5V ±10%

6340 PGM T04.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Current (Active)		60	mA	$\overline{CE}$ = $\overline{RD}$ = V_{IL}, All I/O's = Open,Other Inputs = V_{CC}
$I_{SB1(CMOS)}$	V_{CC} Current (Standby)		100	µA	$\overline{CE}$ = V_{IH}, All I/O's = Open, Other Inputs = V_{IH}, ALE = V_{IL}
$I_{SB2(TTL)}$	V_{CC} Current (Standby)		2	mA	$\overline{CE}$ = V_{IH}, All I/O's = Open, Other Inputs = V_{IH}, ALE = V_{IL}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{RD}$ = $\overline{PSEN}$ = V_{IH}
V_{IL}(3)	Input LOW Voltage	–1	0.8	V	
V_{IH}(3)	Input HIGH Voltage	2	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –400µA

6340 PGM T05.2

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(4)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(4)	Input Capacitance	6	pF	V_{IN} = 0V

6340 PGM T06.0

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(4)	Power-Up to Read	1	ms
t_{PUW}(4)	Power-Up to Write	5	ms

6340 PGM T07.0

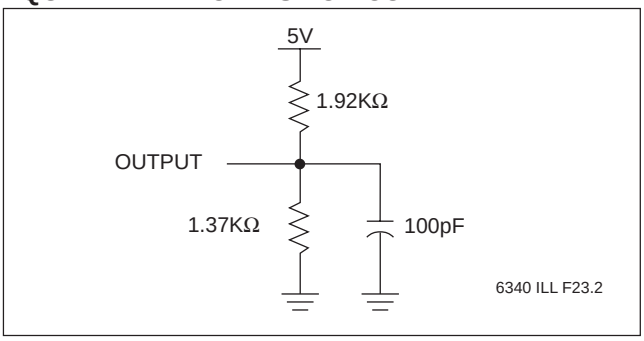
Notes: (3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(4) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

6340 PGM T08.1

EQUIVALENT A.C. TEST CIRCUIT



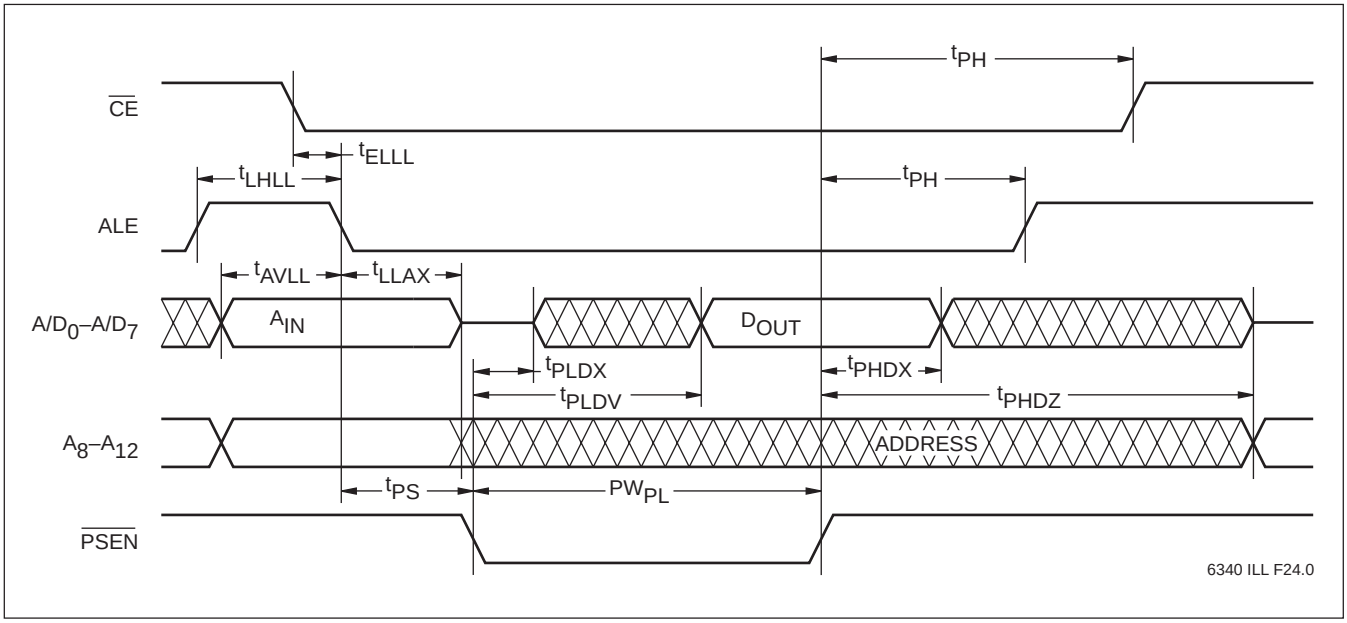
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

$\overline{PSEN}$ Controlled Read Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{PLDV}	$\overline{PSEN}$ Read Access Time		120	ns
t_{PHDX}	Data Hold Time	0		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
PW_{PL}	$\overline{PSEN}$ Pulse Width	150		ns
t_{PS}	$\overline{PSEN}$ Setup Time	30		ns
t_{PH}	$\overline{PSEN}$ Hold Time	20		ns
t_{PHDZ} (5)	$\overline{PSEN}$ Disable to Output in High Z		50	ns
t_{PLDX} (5)	$\overline{PSEN}$ to Output in Low Z	10		ns

6340 PGM T09.0

$\overline{PSEN}$ Controlled Read Timing Diagram



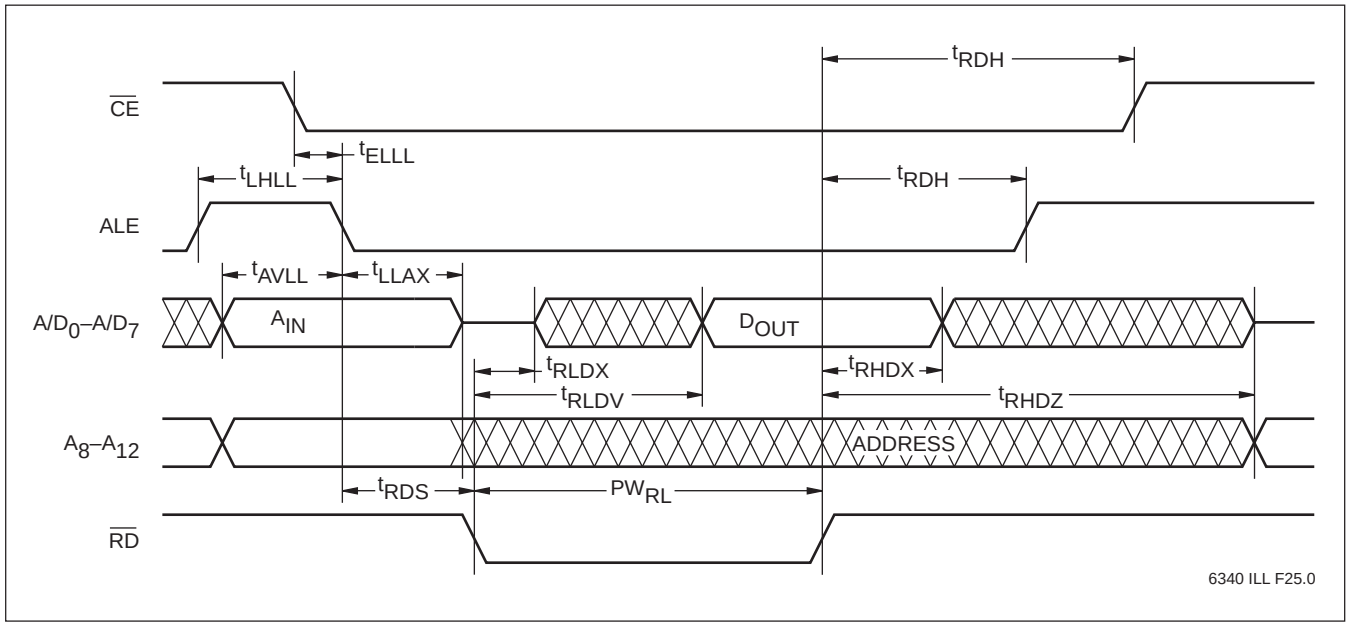
Note: (5) This parameter is periodically sampled and not 100% tested.

$\overline{RD}$ Controlled Read Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{RLDV}	$\overline{RD}$ Read Access Time		120	ns
t_{RHDX}	Data Hold Time	0		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
PW_{RL}	$\overline{RD}$ Pulse Width	150		ns
t_{RDS}	$\overline{RD}$ Setup Time	30		ns
t_{RDH}	$\overline{RD}$ Hold Time	20		ns
t_{RHDZ} (6)	$\overline{RD}$ Disable to Output in High Z		50	ns
t_{RLDX} (6)	$\overline{RD}$ to Output in Low Z	0		ns

6340 PGM T10.0

$\overline{RD}$ Controlled Read Timing Diagram



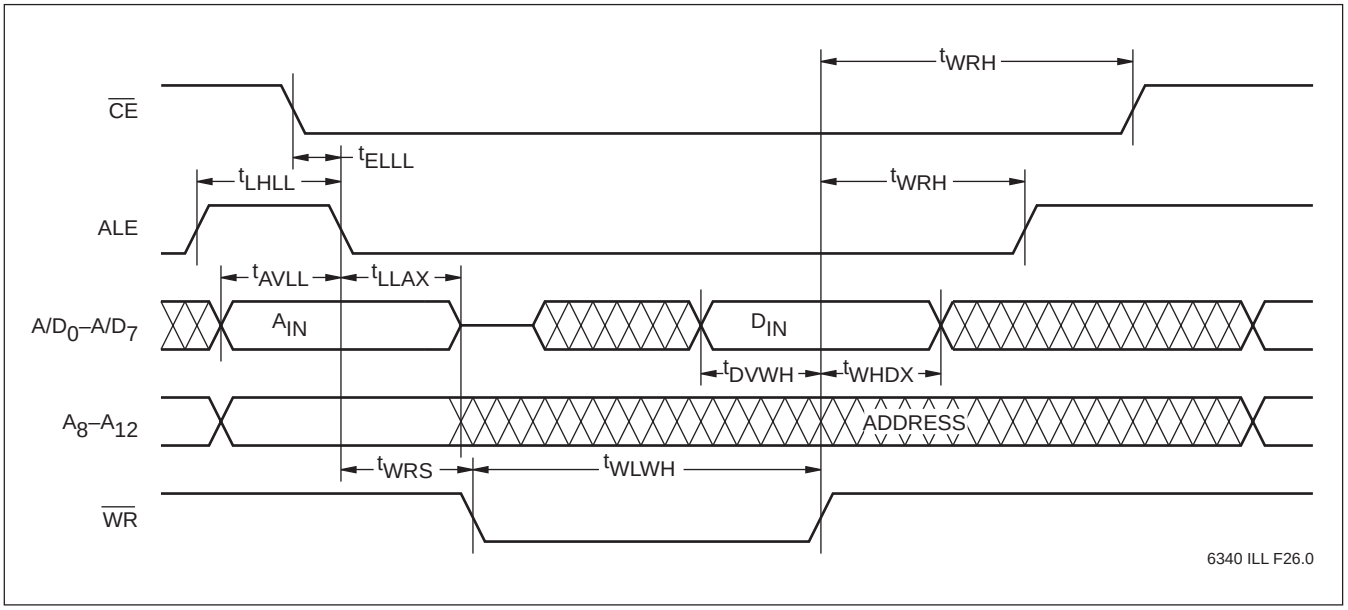
Note: (6) This parameter is periodically sampled and not 100% tested.

$\overline{WR}$ Controlled Write Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{DVWH}	Data Setup Time	50		ns
t_{WHDX}	Data Hold Time	30		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	120		ns
t_{WRS}	$\overline{WR}$ Setup Time	30		ns
t_{WRH}	$\overline{WR}$ Hold Time	20		ns
t_{BLC}	Byte Load Time (Page Write)	0.5	100	µs
t_{WC} (7)	Write Cycle Time		5	ms

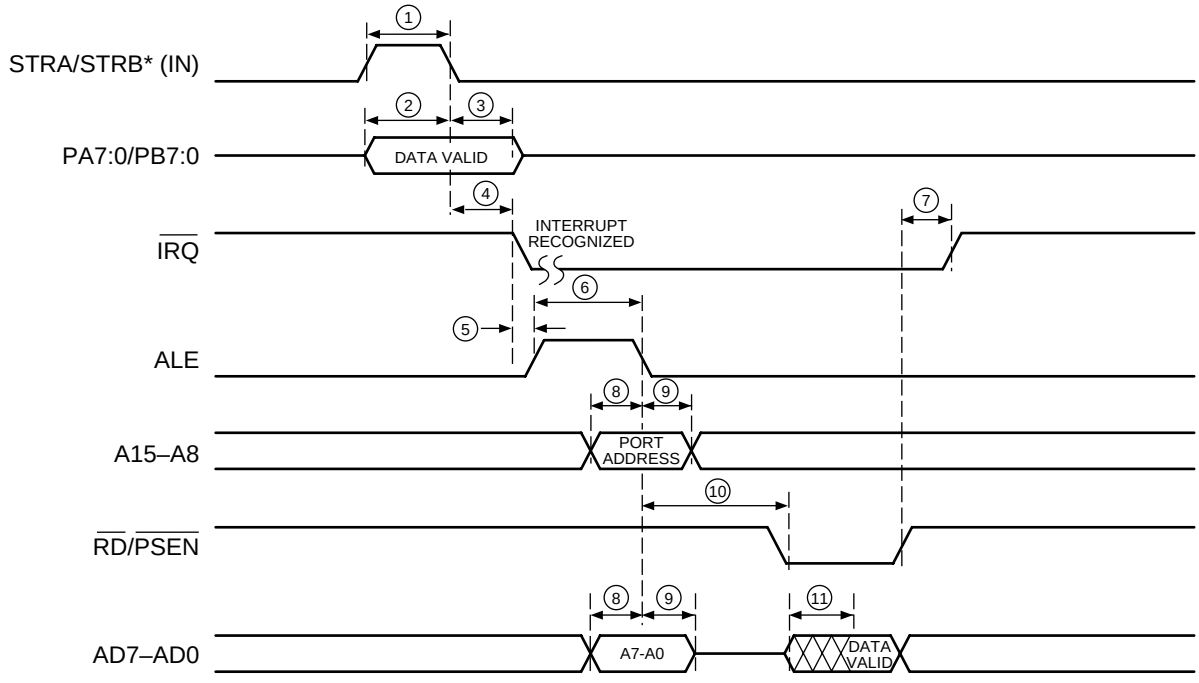
6340 PGM T11.0

$\overline{WR}$ Controlled Write Timing Diagram



Note: (7) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

Port Read Diagram



NOTE: *Figure shows active HIGH strobes.

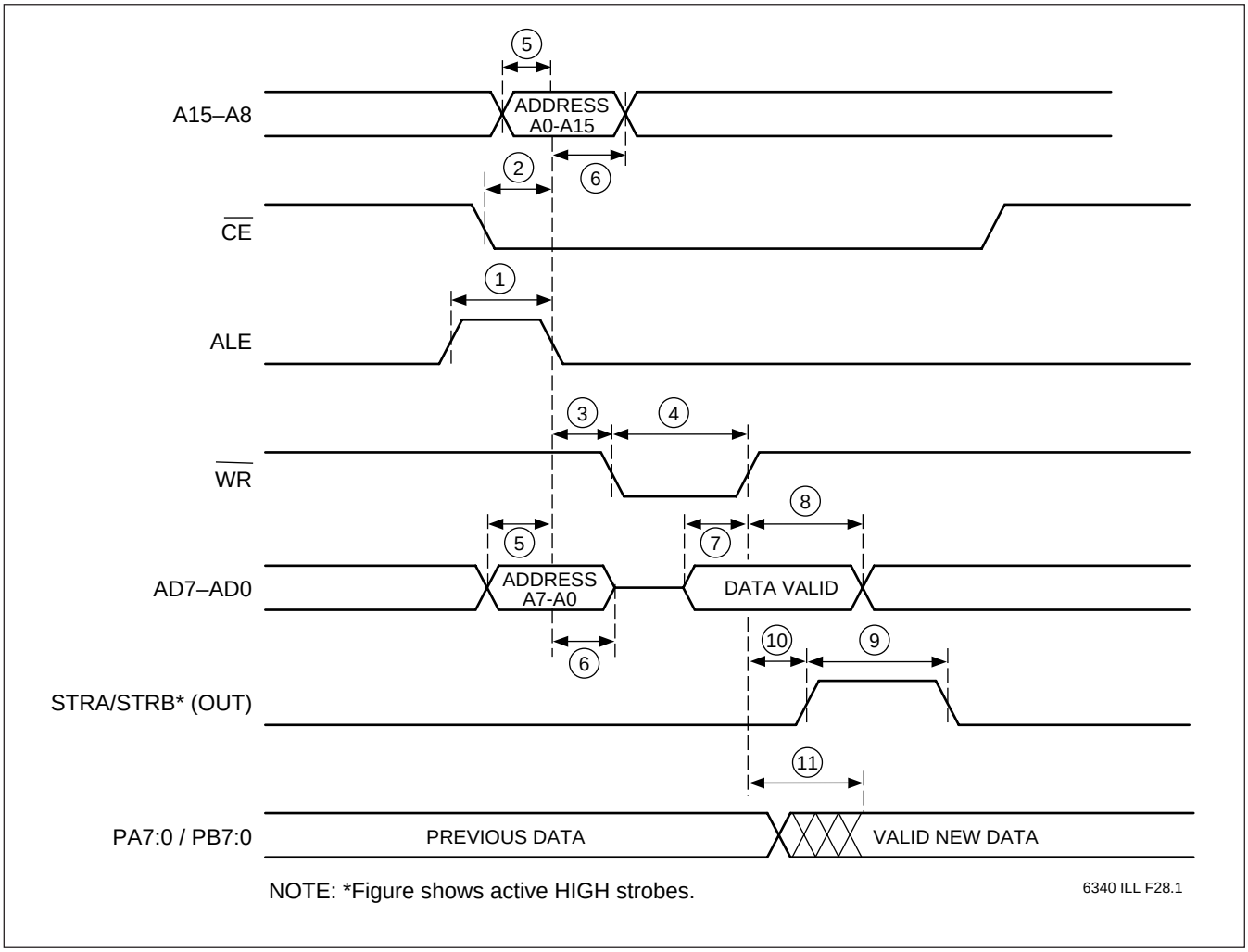
6340 ILL F27.1

PORT READ TIMING

No.	Symbol	Parameter	Min.	Max.	Units
1	t_{SVSX}	Strobe Pulse Width	80		ns
2	t_{DVSV}	Data Port Setup	20		ns
3	t_{SVDX}	Data Port Hold Time	30		ns
4	t_{SVIV}	Interrupt Request to Strobe		50	ns
5	t_{IAD}	$\overline{IRQ}$ to ALE	0		ns
6	t_{LHLL}	ALE Pulse Width	80		ns
7	t_{RXIX}	$\overline{RD}$ to $\overline{IRQ}$	30		ns
8	t_{AVLL}	Address setup time	20		ns
9	t_{LLAX}	Address hold time	30		ns
10	t_{LLWL}	ALE to $\overline{RD}$ LOW	30		ns
11	t_{RLDV}	$\overline{RD}$ Access Time		120	ns

6340 PGM T12.2

Port Write Diagram



NOTE: *Figure shows active HIGH strobes.

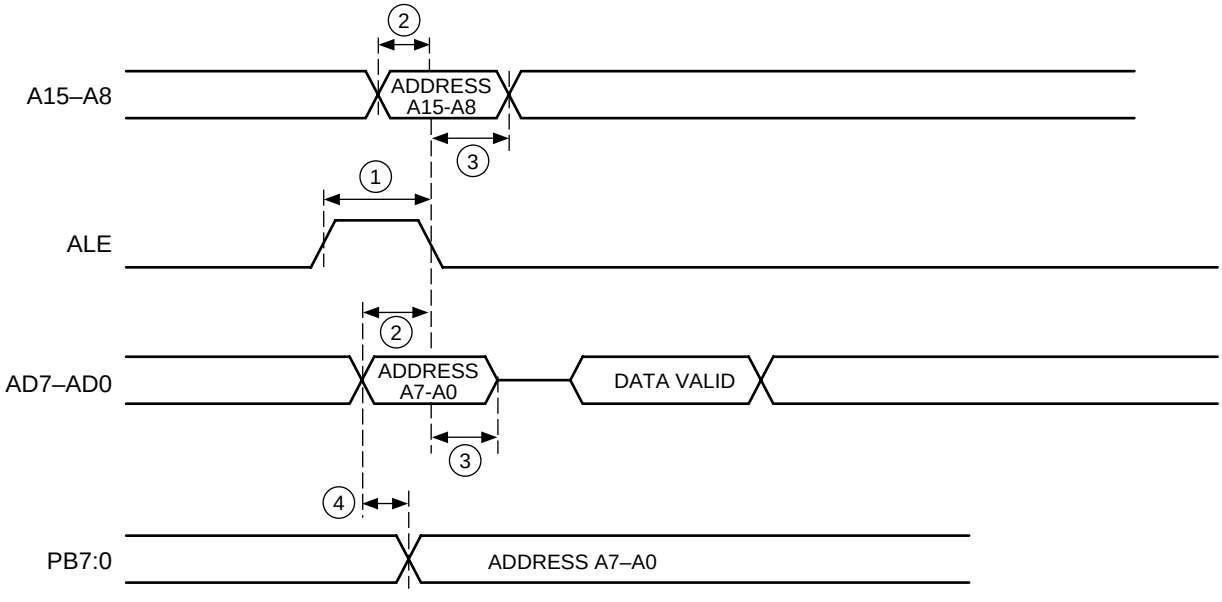
6340 ILL F28.1

PORT WRITE TIMING

No.	Symbol	Parameter	Min.	Max.	Units
1	t_{LHLL}	ALE Pulse Width	80		ns
2	t_{WCS}	Write Chip Select Setup Time	20		ns
3	t_{LLWL}	ALE to $\overline{WR}$	10		ns
4	t_{WLWH}	$\overline{WR}$ Pulse Width	120		ns
5	t_{AVLL}	Write Address Setup Time	20		ns
6	t_{LLAX}	Write Address Hold Time	30		ns
7	t_{DVWH}	Data Setup Time	50		ns
8	t_{WHDX}	Data Hold Time	10		ns
9	t_{SVSX}	Strobe Pulse Width	120		ns
10	t_{QVSV}	Strobe Access Time		40	ns
11	t_{POS}	Port Output Setup Time		40	ns

6340 PGM T13.1

LAM (Latch Address Mode) Diagram



LAM TIMING

No.	Symbol	Parameter	Min.	Max.	Units
1	t_{LHLL}	ALE Pulse Width	80		ns
2	t_{AVLL}	Address Setup Time	20		ns
3	t_{LLAX}	Address Hold Time	30		ns
4	t_{POS}	Port Output Setup Time		20	ns

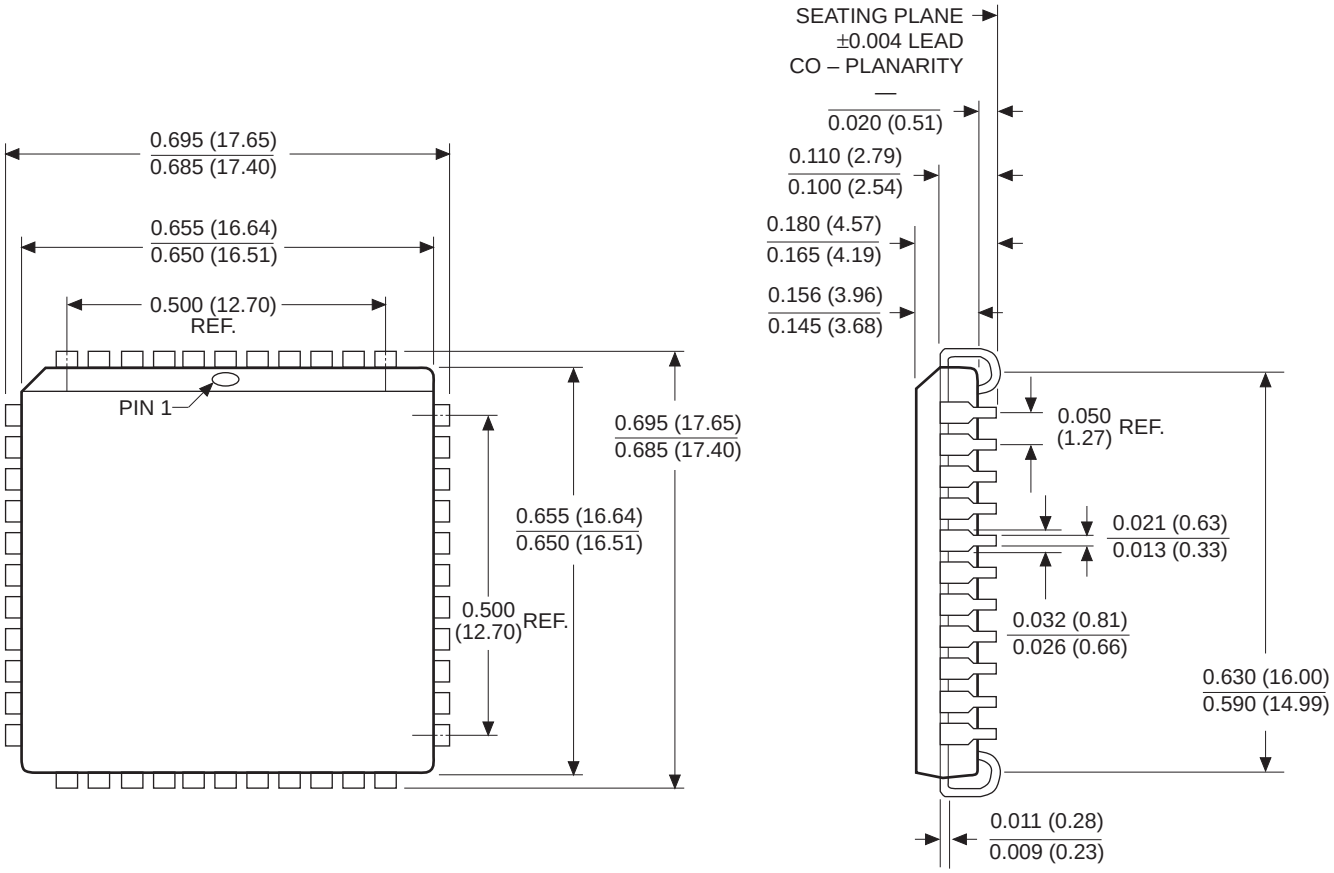
6340 PGM T14.1

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

PACKAGING INFORMATION

44-PIN PLASTIC LEADED CHIP CARRIER PACKAGE TYPE J

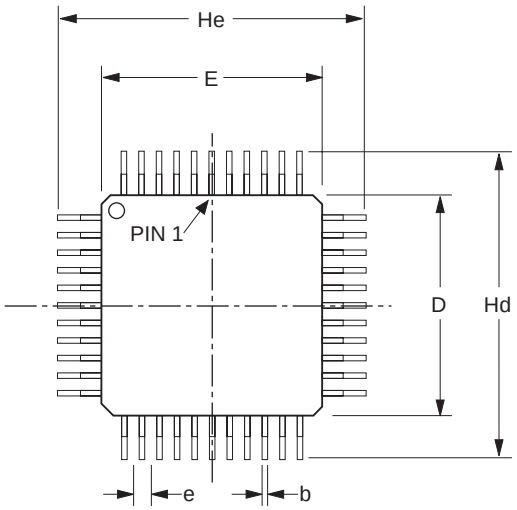


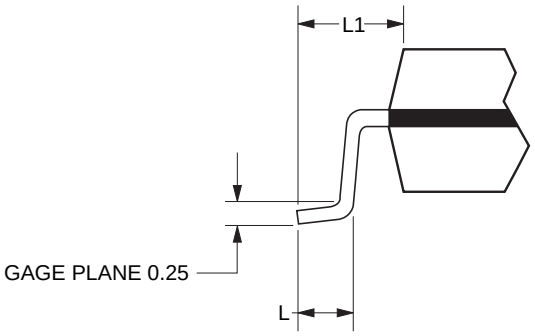
NOTES:
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY**

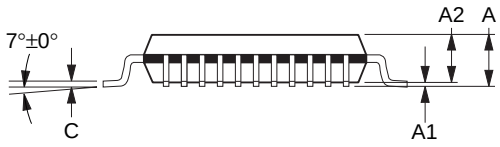
3926 ILL F29.2

PACKAGING INFORMATION

44-LEAD THIN QUAD FLAT PACK (TQFP) PACKAGE TYPE L







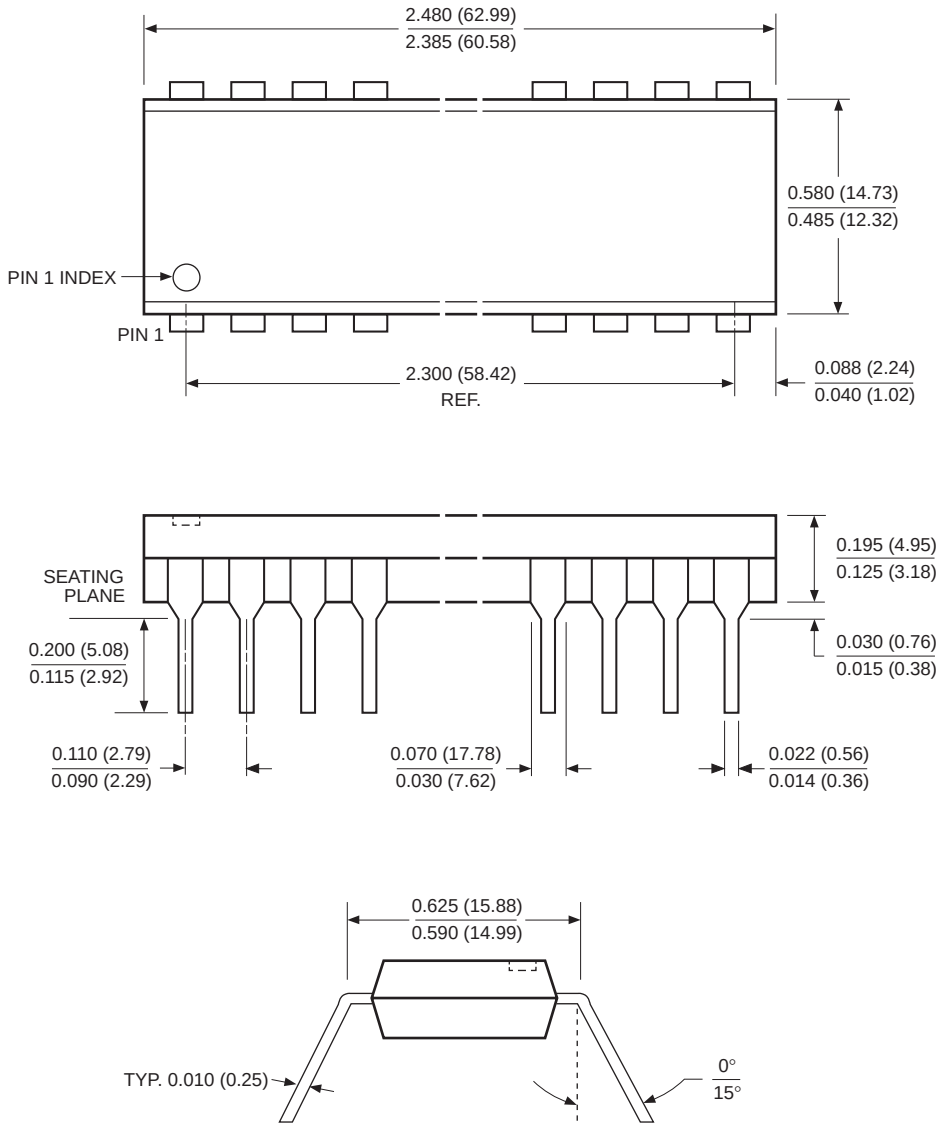
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.00	1.20	0.039	0.047
A_1	0.05	0.15	0.002	0.006
A_2	0.95	1.05	0.037	0.041
b	0.22	0.38	0.009	0.015
c	0.090	0.200	0.004	0.008
D	9.90	10.10	0.390	0.398
E	9.90	10.10	0.390	0.398
e	0.80 TYP		0.031 TYP	
Hd	11.90	12.10	0.468	0.476
He	11.90	12.10	0.468	0.476
L	0.45	0.75	0.018	0.030
L_1	1.00 TYP		0.039 TYP	
0	0	7	0	7

NOTES:
1. GAGE PLANE DIMENSION IS IN MM.
2. LEAD COPLANARITY SHALL BE 0.10MM [0.004] MAXIMUM.

3926 ILL F36.3

PACKAGING INFORMATION

48-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

3926 FHD F43.1

ORDERING INFORMATION