M64894FP/GP

Serial Input PLL Frequency Synthesizer for TV/VCR

REJ03F0166-0200
Rev.2.00
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Description

The M64894 is a semiconductor integrated circuit consisting of PLL frequency synthesizer for TV/VCR using I^2C BUS control. It contains the prescaler with operating up to 1.3 GHz. 4 band drivers and tuning amplifier for direct tuning. Built-in 4 band drivers.

Features

- 4 integrated PNP band drivers (I_O = 40 mA, Vsat = 0.2 V Typ@V_{CC1} to 13.2 V)
- Built-in high-withstanding voltage tuning Amplifier
- Low power dissipation (I_{CC} = 20 mA, V_{CC} = 5 V)
- Built-in prescaler with input amplifier (Fmax = 1.3 GHz)
- I^2C bus control (Read and write mode)
- X'tal 4 MHz is used to realize 3 type of tuning steps (Division ratio 1/512, 1/640, 1/1024)
- Built-in 5-level A/D converter
- Programmable chip address
- 16-pin small SOP/SSOP package

Function

- 2-modulus prescaler (1/32 and 1/33)
- Built-in 4 MHz crystal oscillator and reference divider
- Programmable divider (10-bit M counter, 5-bit S counter)
- Tri-state phase comparator
- Lock detector
- Band switch driver
- Op.Amp for direct tuning
- I^2C bus receiver
- 5-level A/D converter

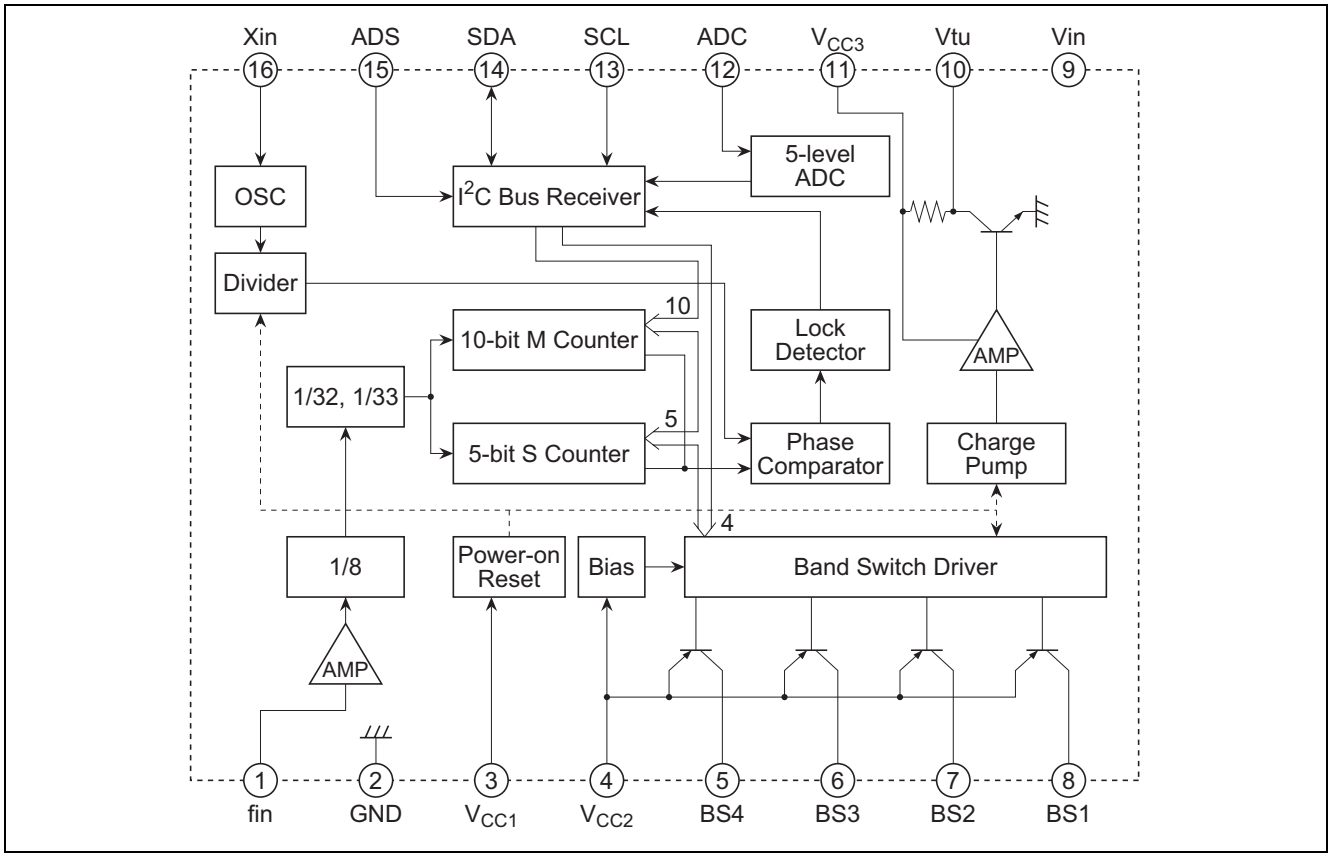
Application

TV, VCR tuners

Recommended Operating Condition

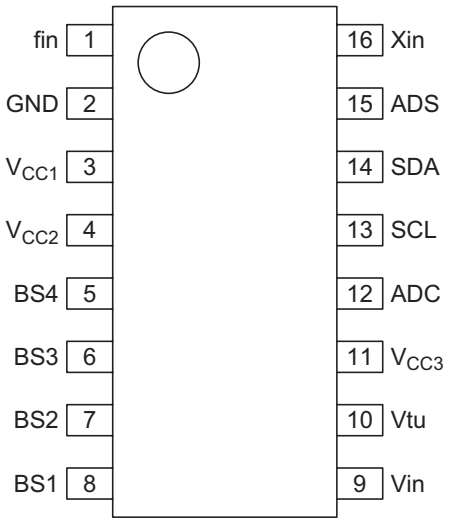
- Supply voltage range
  - V_{CC1} = 4.5 to 5.5 V
  - V_{CC2} = V_{CC1} to 13.2 V
  - V_{CC3} = 28 to 35 V
- Rated supply voltage
  - V_{CC1} = 5 V
  - V_{CC2} = 12 V
  - V_{CC3} = 33 V

Block Diagram



Pin Arrangement

M64894FP/GP



(Top view)

Outline: PRSP0016DA-A (16P2S-A) [FP]
PRSP0016JA-A (16P2Z-A) [GP]

Pin Description

Pin No.	Symbol	Pin name	Function
1	fin	Prescaler input	Input for the VCO frequency.
2	GND	GND	Ground to 0 V.
3	V_{CC1}	Power supply voltage 1	Power supply voltage terminal. 5.0 V ± 0.5 V
4	V_{CC2}	Power supply voltage 2	Power supply for band switching, V_{CC1} to 13.2 V
5 6 7 8	BS4 BS3 BS2 BS1	Band switching outputs	PNP open collector method is used. When the band switching data is “H”, the output is ON. When it is “L”, the output is OFF.
9	Vin	Filter input (Charge pump output)	This is the output terminal for the LPF input and charge pump output. When the phase of the programmable divider output (f 1/N) is ahead compared to the reference frequency (f_{REF}), the “source” current state becomes active. If it is behind, the “sink” current becomes active. If the phases are the same, the high impedance state becomes active.
10	Vtu	Tuning output	This supplies the tuning voltage.
11	V_{CC3}	Power supply voltage 3	Power supply voltage for tuning voltage 28 to 35 V
12	ADC/ftest	AD converter input/ Test port	A/D conversion of the input voltage. In control byte data input, the programmable freq. Divider output and reference freq. output is selected by the test mode.
13	SCL	Clock input	Data is read into the shift register when the clock signal falls.
14	SDA	Data input	Input for band SW and programmable freq. divider set up. In lead mode, it outputs lock detector output and power down flag and a state of 5 level A/D converter.
15	ADS	Address switching input	Chip address sets it up with the input condition of terminal.
16	Xin	This is connected to the crystal oscillator	4.0 MHz crystal oscillator is connected.

Absolute Maximum Ratings

(Ta = –20°C to +75°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Condition
Supply voltage 1	V_{CC1}	6.0	V	Pin3
Supply voltage 2	V_{CC2}	14.4	V	Pin4
Supply voltage 3	V_{CC3}	36.0	V	Pin11
Input voltage	V_I	6.0	V	Not to exceed V_{CC1}
Output voltage	V_O	6.0	V	f_{REF} output
Voltage applied when the band output is OFF	V_{BSOFF}	14.4	V	
Band output current	I_{BSON}	50.0	mA	Per 1 band output circuit
ON the time when the band output is ON	t_{BSON}	10	s	50mA per 1 band output circuit 3circuit are pn at same time
Power dissipation	Pd	450 (470)	mW	Ta = +75°C
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–40 to +125	°C	

Recommended Operation Conditions

(Ta = –20°C to +75°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions
Supply voltage 1	V_{CC1}	4.5 to 5.5	V	Pin3
Supply voltage 2	V_{CC2}	V_{CC1} to 13.2	V	Pin4
Supply voltage 3	V_{CC3}	28 to 35	V	Pin11
Operating frequency (1)	fopr1	4.0	MHz	Crystal oscillation circuit
Operating frequency (2)	fopr2	80 to 1,300	MHz	
Band output current 5 to 8	I_{BDL}	0 to 40	mA	Normally 1 circuit is on. 2 circuits on at the same time are max. It is prohibited to have 3 or more circuits turned on at the same time.

Electrical Characteristics

(Ta = –20°C to +75°C, V_{CC1} = 5.0 V, V_{CC2} = 12 V, V_{CC3} = 33 V, unless otherwise noted)

Item		Symbol	Test Pin	Limits			Unit	Test Conditions
				Min.	Typ.	Max.		
Input pin	"H" input voltage	V_{IH}	13 to 14	3.0	—	V_{CC1} + 0.3	V	
	"L" input voltage	V_{IL}	13 to 14	—	—	1.5	V	
	"H" input current	I_{IH}	13 to 14	—	—	10	µA	V_{CC1} = 5.5V, Vi = 4.0V
	"L" input current	I_{IL}	13, 14	—	–4/–14	–10/30	µA	V_{CC1} = 5.5V, Vi = 0.4V
SDA output	"H" output voltage	V_{OL}	14	—	—	0.4	µA	V_{CC1} = 5.5V, I_O = 3mA
	"L" output voltage	V_{LO}	14	—	—	10	µA	V_{CC1} = 5.5V, V_O = 5.5V
Band SW	Output voltage	V_{BS}	5 to 8	11.6	11.8	—	V	V_{CC2} = 12V, I_O = –40mA
	Leak current	I_{OLK1}	5 to 8	—	—	–10	µA	V_{CC2} = 12V band SW is OFF
Tuning output	Output voltage "H"	V_{TOH}	10	32.5	—	—	V	V_{CC3} = 33V
	Output voltage "L"	V_{TOL}	10	—	0.2	0.4	V	V_{CC3} = 33V
Charge pump	"H" output current	I_{OH}	9	—	270	370	µA	V_{CC1} = 5.0V, V_O = 2.5V
	"L" output current	I_{OL}	9	—	70	110	µA	V_{CC1} = 5.0V, V_O = 2.5V
	Leak current	I_{CPLK}	9	—	—	50	nA	V_{CC1} = 5.5V, V_O = 2.5V
Supply current 1		I_{CC1}	3	—	20	30	mA	V_{CC1} = 5.5V
Supply current 2	4 circuits: OFF	I_{CC2A}	4	—	—	0.3	mA	V_{CC2} = 12V
	1circuits: ON, Output: OPEN	I_{CC2B}	4	—	6.0	8.0	mA	V_{CC2} = 12V
	Output current 40mA	I_{CC2C}	4	—	46.0	48.0	mA	V_{CC2} = 12V I_O = –40mA
Supply current 3		I_{CC3}	11	—	3.0	4.0	mA	V_{CC3} = 12V Output ON

Note: Typical values are measured at V_{CC1} = 5.0 V, V_{CC2} = 12 V, V_{CC3} = 33 V, Ta = +25°C.

Switching Characteristics

(Ta = –20°C to +75°C, V_{CC1} = 5.0 V, V_{CC2} = 12 V, V_{CC3} = 33 V, unless otherwise noted)

Item	Symbol	Test Pin	Limits			Unit	Test Conditions	
			Min.	Typ.	Max.			
Prescaler operating frequency	fopr	1	80	—	1300	MHz	V_{CC1} = 4.5 to 5.5V Vin = Vinmin to Vinmax	
Operating input voltage	Vin	1	–24	—	4	dBm	V_{CC1} = 4.5 to 5.5V	80 to 100MHz
			–27	—	4			100 to 200MHz
			–30	—	4			200 to 800MHz
			–27	—	4			800 to 1000MHz
			–18	—	4			1000 to 1300MHz
Clock pulse frequency	t_{SCL}	13	0	—	100	kHz	V_{CC1} = 4.5 to 5.5V	
Bus free time	t_{BUF}	14	4.7	—	—	µs	V_{CC1} = 4.5 to 5.5V	
Data hold time	t_{HDSTA}	13	4	—	—	µs	V_{CC1} = 4.5 to 5.5V	
SCL low hold time	t_{LOW}	13	4.7	—	—	µs	V_{CC1} = 4.5 to 5.5V	
SCL high hold time	t_{HIGH}	13	4	—	—	µs	V_{CC1} = 4.5 to 5.5V	
Set up time	t_{SUSTA}	13, 14	4.7	—	—	µs	V_{CC1} = 4.5 to 5.5V	
Data hold time	t_{HDDAT}	13, 14	0	—	—	s	V_{CC1} = 4.5 to 5.5V	
Data set up time	t_{SUDAT}	13, 14	250	—	—	ns	V_{CC1} = 4.5 to 5.5V	
Rise time	t_r	13, 14	—	—	1000	ns	V_{CC1} = 4.5 to 5.5V	
Fall time	t_f	13, 14	—	—	300	ns	V_{CC1} = 4.5 to 5.5V	
Set up time	t_{SUSTO}	13, 14	4	—	—	µs	V_{CC1} = 4.5 to 5.5V	

Method of Setting Data

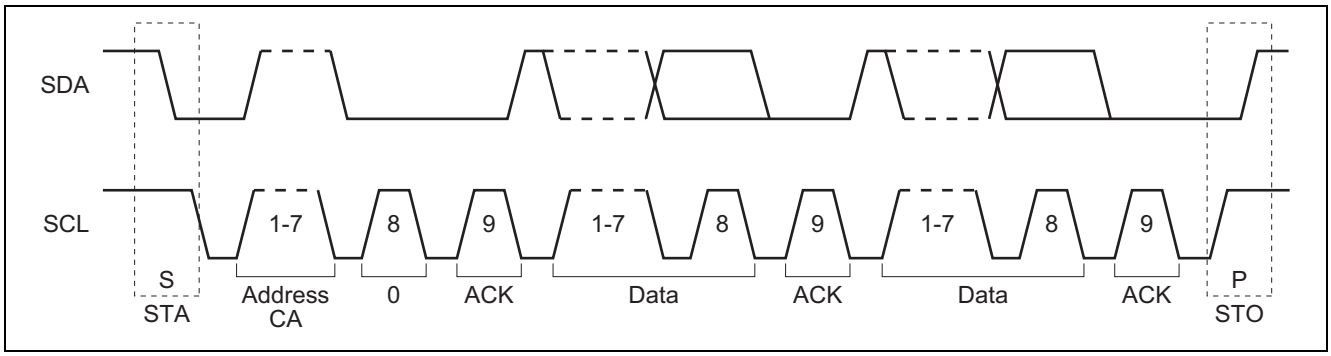
The input information to consist of 2 or data of 4 bytes to lead to chip address is received in I^2C bus receiver. It shows a definition of bus protocol admitted in the following.

1_STA	CA	CB	BB	STO		
2_STA	CA	D1	D2	STO		
3_STA	CA	CB	BB	D1	D2	STO
4_STA	CA	D1	D2	CB	BB	STO

STA : Start condition
STO : Stop condition
CA : Chip address
CB : Control data byte
BB : Band SW data byte
D1 : Divider data byte
D2 : Divider data byte

The information of 5 bytes necessary for circuit operation is chip address and control data, band SW data of 2 bytes and divider byte of 2 bytes. After the chip address input, 2 or data of 4 bytes are received.

Function bit is contained the first and the third data byte to distinguish between divider data and control data, band data, and “0” goes ahead of divider data, and “1” goes ahead of control data, band SW data.



Write Mode Format

Byte	MSB								LSB
Address byte	1	1	0	0	0	MA1	MA0	0	A
Divider byte 1	0	N14	N13	N12	N11	N10	N9	N8	A
Divider byte 2	N7	N6	N5	N4	N3	N2	N1	N0	A
Control byte1	1	CP	T2	T1	T0	RSa	RSb	OS	A
Band SW byte	X	X	X	X	BS4	BS3	BS2	BS1	A

Read Mode Format

Byte	MSB								LSB
Address byte	1	1	0	0	0	MA1	MA0	1	A
Status byte 1	POR	FL	X	X	X	A2	A1	A0	A

Data Cording Example

Write Mode Format Example

Byte	MSB								LSB	Condition in Data Setting
Address Byte	1	1	0	0	0	1	1	0	1	ADS input V_{CC1}
Divider byte 1	0	1	0	0	0	0	0	0	1	Dividing ratio N = 16544
Divider byte 2	1	0	1	0	0	0	0	0	1	
Control byte 1	1	1	0	0	0	0	1	0	1	C.P.current 270µA f_{REF} division ratio 1/1024
Band SW byte	0	0	0	0	1	0	0	0	1	BS4 output ON

Note: f_{VCO} = N 8 f_{REF} = 16544 8 (4MHz/1024) = 517MHz

Read Mode Format Example

Byte	MSB								LSB	Condition in Data Setting
Address byte	1	1	0	0	0	1	1	1	1	
Status byte 1 input	1	1	1	1	1	1	1	1	1	
Status byte 1 output	0	1	1	1	1	0	1	1	1	FL “1” output at locked ADC input at open

Test Mode Data Set Up Method

Test Mode Bit Set Up

X : Random, 0 or 1. normal “0”

MA1, MA0 : Programmable address bit

Address Input Voltage	MA1	MA0
0 to 0.1 ± V_{CC1}	0	0
Always valid	0	1
0.4 ± V_{CC1} to 0.6*V_{CC1}	1	0
0.9 ± V_{CC1} to V_{CC1}	1	1

Note: N14 to N0: How to set dividing ratio of the programmable the divider

Dividing ratio N = N14 (2^{14} = 16384) + +N0 (2^0 = 1)

Therefore, the range of division N is 1,024 to 32,768

Example) f_{VCO} = f_{REF} • 8 • N

= 3.90625 • 8 • N

= 31.25 • N (kHz)

CP: Setting Up The Charge Pump Current of The Phase Comparator

CP	Charge pump current	Mode
0	70 µA	Test
1	270 µA	Normal

T2, T1, T0: Setting Up for The Test Mode

T2	T1	T0	Charge Pump	Pin 12 Condition	Mode
0	0	X	Normal operation	ADC input	Normal operation
0	1	X	High impedance	ADC input	Test mode
1	1	0	Sink	ADC input	Test mode
1	1	1	Source	ADC input	Test mode
1	0	0	High impedance	f_{REF} output	Test mode
1	0	1	High impedance	f1/N output	Test mode

RSa, RSb: Set Up for The Reference Frequency Division Ratio

RSa	RSb	Division Ratio
1	1	1/512
0	1	1/1024
X	0	1/640

OS: Set Up The Tuning Amplifier

OS	Tuning Voltage Output	Mode
0	ON	Normal
1	OFF	Test

POR : Power on reset flag. “1” output at reset
FL : Lock detector flag. “1” output at locked, “0” output at unlocked

A2, A1, A0: 5 Level A/D Converter Output Data

ADC Input Voltage	A2	A1	A0
$0.6 \pm V_{CC1}$ to V_{CC1}	1	0	0
$0.45 \pm V_{CC1}$ to $0.6 \pm V_{CC1}$	0	1	1
$0.3 \pm V_{CC1}$ to $0.45 \pm V_{CC1}$	0	1	0
$0.15 \pm V_{CC1}$ to $0.3 \pm V_{CC1}$	0	0	1
0 to $0.15 \pm V_{CC1}$	0	0	0

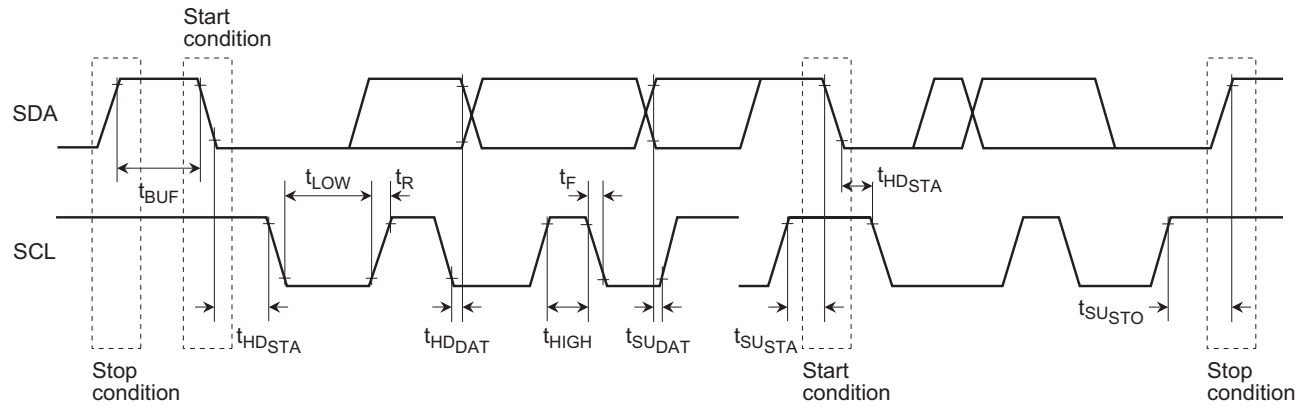
Note: The voltage accuracy allowance range: $0.03 \pm V_{CC1}$ (V)

Power On Reset Operation

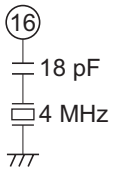
(Initial state the power is turned ON)

BS4 to BS1 : OFF
Charge pump : High impedance
Tuning amplifier : OFF
Charge pump current : 270 µA
Frequency division ratio : 1/1024

Timing Diagram

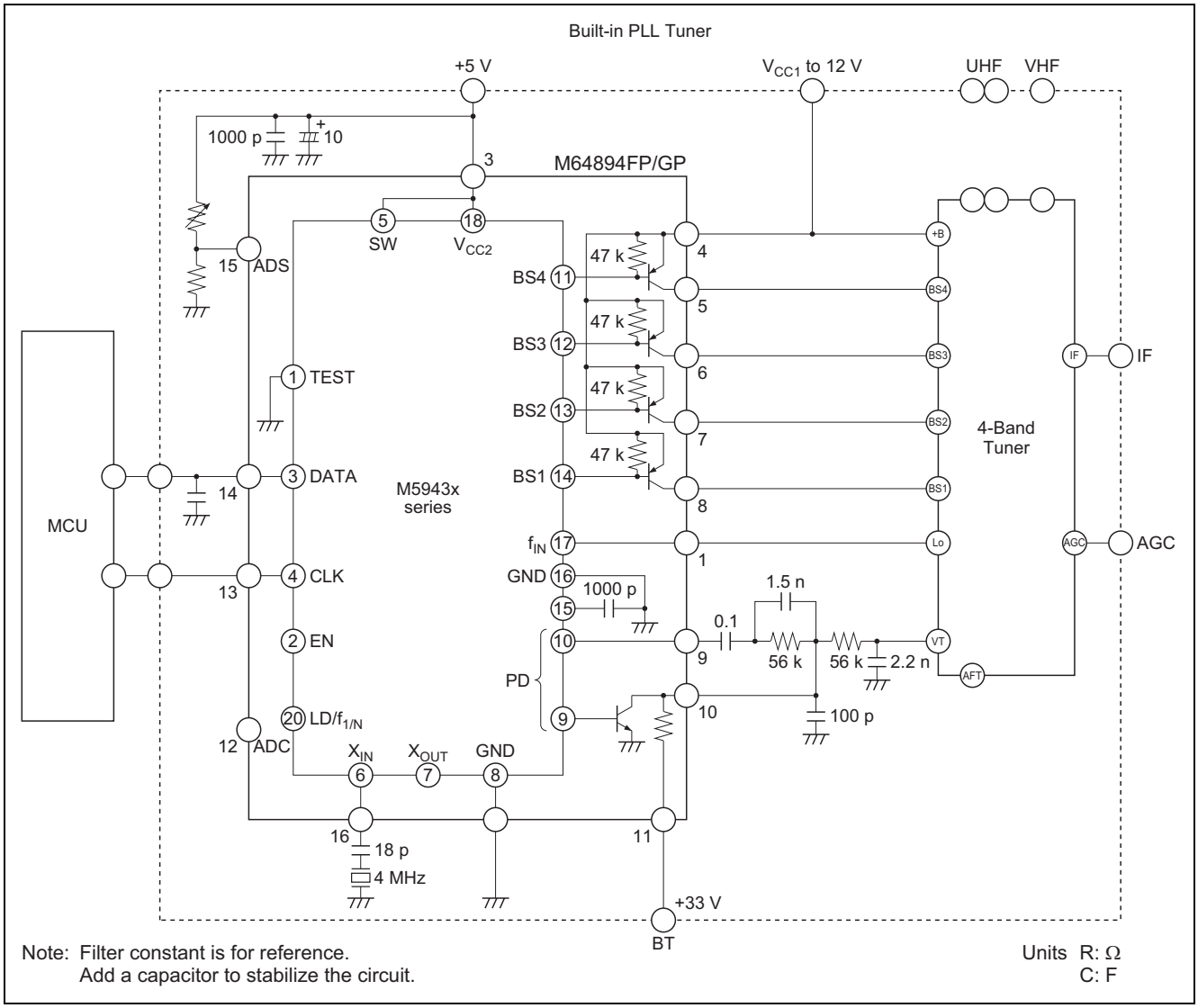


Crystal Oscillator Connection Diagram



Crystal oscillator characteristics
Actual resistance: less than 300 Ω
Load capacitance: 20 pF

Application Example

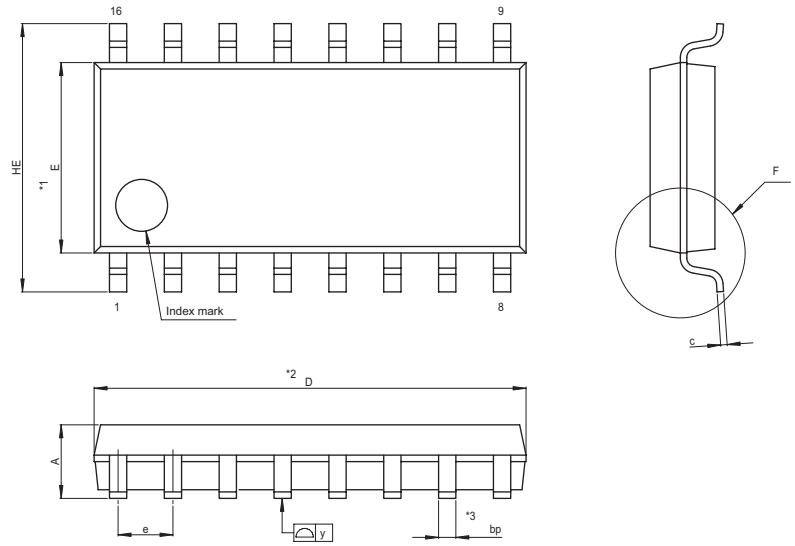


Note: Filter constant is for reference.
Add a capacitor to stabilize the circuit.

Units R: Ω
C: F

Package Dimensions

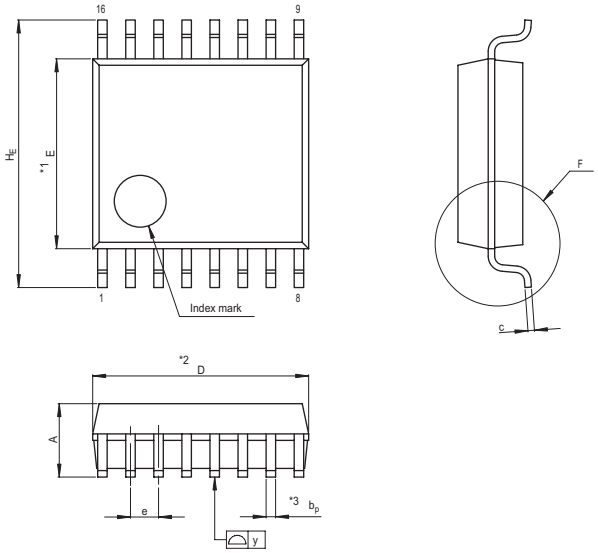
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-4.4x10-1.27	PRSP0016DA-A	16P2S-A	0.15g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.8	10.0	10.2
E	4.2	4.4	4.6
A_2	—	1.5	—
A_1	0.05	—	—
A	—	—	1.9
b_p	0.35	0.4	0.5
c	0.13	0.15	0.2
θ	0°	—	10°
H_E	5.9	6.2	6.5
e	1.07	1.27	1.47
y	—	—	0.1
L	0.2	0.4	0.6

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SSOP16-4.4x5-0.65	PRSP0016JA-A	16P2Z-A	0.08g



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Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.8	5.0	5.2
E	4.2	4.4	4.6
A_2	—	1.5	—
A	—	—	1.9
A_1	0.05	—	—
b_p	0.17	0.22	0.32
c	0.13	0.15	0.2
θ	0°	—	10°
H_E	5.9	6.2	6.5
e	0.5	0.65	0.8
y	—	—	0.10
L	0.2	0.4	0.6

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