

# □ MN101D07G, MN101D07H

Type	MN101D07G	MN101D07H	MN101DF07Z
Internal ROM type	Mask ROM		FLASH
ROM (byte)	128K	160K	224K
RAM (byte)	4K	5K	6K
Package (Lead-free)	LQFP112-P-2020		
Minimum Instruction Execution Time	[With main clock operated] 0.1397 μs (at 4.0 V to 5.5 V, 14.32 MHz) 71.5 μs (at 3.0 V to 5.5 V, 14.32 MHz internal frequency di Vision) [When sub-clock operated] 61 μs (at 2.2 V to 5.5 V, 32.768 kHz)		0.1397 μs (at 4.0 V to 5.5 V, 14.32 MHz) 71.5 μs (at 3.0 V to 5.5 V, 14.32 MHz internal frequency di Vision) 61 μs (at 2.5 V to 5.5 V, 32.768 kHz)

## ■ Interrupts

RESET, Runaway, External 0 to 4, key input (P50 to P54), Timer 0 to 4, Timer 6, Timer 7, Capstan FG, Control, HSW, Cylinder(Drum) FG, Servo V-sync, Synchronous output, OSD, XDS, Serial 0 to 2, A/D (common with PWM 4 reference frequency), OSD V-sync

## ■ Timer Counter

Timer counter 0 : 16-bit × 1

(timer function, clock function [max. 2 s or max. 36 h at cascade-connecting with timer 6])

Clock source..... 1/2, (1/4,) 1/8, (1/16) of system clock frequency; overflow of timer counter 6; 1/512 of XI oscillation clock or OSC oscillation clock frequency

Interrupt source ..... overflow of timer counter 0

Timer counter 1 : 16-bit × 1 (timer function, linear timer counter function)

Clock source..... 1/2, (1/4,) 1/8, (1/16) of system clock frequency; CTL signal

Interrupt source ..... overflow of timer counter 1

Timer counter 2 : 16-bit × 1

(timer function, input capture

(DCTL specified edge), duty judgment of DCTL signal)

Clock source..... 1/2, (1/4,) 1/8, (1/16,) 1/12, (1/24) of system clock frequency

Interrupt source ..... overflow of timer counter 2; input of DCTL specified edge; underflow of timer 2 shift register 4-bit counter; coincidence of timer 2 shift register with timer 2 shift register compare register

Timer counter 3 : 16-bit × 1

(timer function, detection of serial indexing, generation of remote control output carrier frequency)

Clock source..... 1/2, (1/4,) 1/8, (1/16) of system clock frequency; XI oscillation clock

Interrupt source ..... overflow of timer counter 3

Timer counter 4 : 16-bit × 1 (timer function, event count [P15 input], generation of serial transmission clock)

Clock source..... 1/8, (1/16) of system clock frequency; external clock input

Interrupt source ..... overflow of timer counter 4; coincidence of timer counter 4 with OCR4

Timer counter 5 : 19-bit × 1 (watchdog, stable oscillation waiting function)

Clock source..... system clock

Watchdog interrupt source... 1/2<sup>16</sup>, 1/2<sup>19</sup> of timer counter 5 frequency

Clear by stable oscillation ... after 256 counts by timer counter 5 (218 counts of OSC oscillation clock)

Timer counter 6 : 16-bit × 1 (clock function [max. 2 s])

Clock source..... 1/512 of OSC oscillation clock frequency; XI oscillation clock; 1/4, (1/8,) 1/64, (1/128) of system clock frequency

Interrupt source ..... 1/2<sup>13</sup>, 1/2<sup>14</sup>, 1/2<sup>15</sup> overflow of timer counter 6

Timer counter 7 : 8-bit × 1 or 4-bit × 2 (timer function, event count)

Clock source..... 1/4, (1/8,) 1/16, (1/32) of system clock frequency; external clock input

Interrupt source ..... overflow of timer counter 7 (although when 4-bit × 2, there is one interrupt vector. )

■ Serial interface

Serial 0 : 8-bit × 1 (synchronous type/start-stop synchronous type) (transfer direction of MSB/LSB selectable)

Synchronous type clock source ..... 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency; 2-division timer 4 output; NSBT0 pin input  
 Clock for UART ..... 8-division of above clock; 2-division timer 4 output; NSBT0 pin input

Serial 1 : 8-bit × 1 (synchronous type/remote control transmission/simple remote control receive)  
 (transfer direction of MSB/LSB selectable, start condition function)

Clock source ..... 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency; 2-division timer 4 output; NSBT1 pin input  
 Remote control clock ..... 2-division timer 4 output

Serial 2 : 8-bit × 1 (I<sup>2</sup>C)

(master transmission/reception, slave transmission/reception)

Clock source ..... 1/144 to 1/252 of system clock, SCK pin input

■ OSD

OSD mode : Accommodation with menu(internal synchronous) or super impose(external synchronous) display

Applicable broadcasting system....NTSC, PAL, PAL-M, PAL-N  
 Screen configuration .....24 characters × 2n rows (n = 1 to 6)  
 Character type .....max. 512 character types (variable)  
 Character size ..... 12 × 18 dots  
 Enlarged characters .....each × 2, × 3 or × 4 settings in horizontal and vertical  
 Character interpolation.....none  
 Line background color ..... 8-hue settable (settable in the row unit at menu display)  
 Line background intensity..... 8 gradations settable in the row unit(at output of composite video signal)  
 Screen background color..... 8-hue settable (at output of composite video signal)  
 Character color ..... white (at output of composite video signal)  
 Character intensity ..... 8 gradations settable in the row unit  
 Frame function ..... 1-dot frame in 4 or 8 directions (at output of composite video signal)  
 Frame intensity ..... 4 gradations settable in the row unit  
 Box shade function ..... settable in the character unit (at output of composite video signal with 129 or more characters  
 (character types))  
 Blinking.....none (covered by software)  
 Inverted character..... settable in the character unit  
 Halftone..... settable in the row unit in 2 intensity gradations (at output of external synchronous composite  
 video signal)

CCD mode : Supports Closed Caption in the U.S.A.

Screen configuration .....2 characters × 16 rows  
 Character type .....max. 128 character types (variable)  
 Character size ..... 2 × 26 dots (including 8 dots in the underlined area)  
 Enlarged characters ..... none  
 Character interpolation..... none  
 Line background color ..... 8-hue settable  
 Line background intensity..... 8 gradations settable in the screen unit (at output of composite video signal)  
 Screen background color..... 8-hue settable (at output of composite video signal)  
 Character color ..... 8 colors (at RGB output), White (at output of composite video signal)  
 Character intensity ..... 8 gradations settable in the screen unit(at output of composite video signal)  
 Frame function ..... none  
 Box shade function ..... none  
 Inverted character..... none  
 Halftone..... settable in the row unit in 2 intensity gradations (at output of external synchronous composite  
 video signal)  
 Others ..... Underline, italic, blinking function and scroll

Common

Input ..... composite video signal input (output level : 1 V[p-p] / 2 V[p-p])  
 Clamp method ..... sync tip clamp, clamp level in 4 levels  
 Output ..... composite video output, output of Y/C split video signal, digital output (6 pins)  
 Measure against image fluctuation..... built-in AFC circuit  
 Dot clock ..... 1/2 of OSC oscillation clock (automatic phase adjustment)

■ XDS

Built-in U.S. closed caption data slicer (optional 2 line data can be extracted.)

■ I/O Pins

I/O	85	Common use : 71
Input	2	Common use : 2

■ A/D converter

8-bit × 14-ch. (without S/H)

■ PWM

13-bit × 2-ch. (at repetition cycle 572 ms at 14.32 MHz),  
 10-bit × 2-ch. (at repetition cycle 71.5 ms at 14.32 MHz),  
 8-bit × 1-ch. (at repetition cycle 71.5 ms, 0.572 ms, 1.14 ms, 2.29 ms at 14.32 MHz)

■ ICR

18-bit × 6-ch.

■ OCR

16-bit × 2 (8-bit synchronous output; 4-bit 3-state synchronous output),  
 16-bit × 1 (weak electric field V-sync backup), 16-bit × 1 (Rec CTL)

■ Special Ports

Buzzer output; 3-state output VLP pin; remote control receive;  
 CTL signal input terminal; Capstan FG input terminal; Cylinder(Durm) PG/FG input terminals;  
 HSW output terminal; Head Amp/Rotary control output terminals;  
 output of 1/2 OSC oscillation clock (2 V[p-p]); output of 1/4 OSC oscillation clock (1 V[p-p])

■ ROM Correction

Correcting address designation : up to 3 addresses possible  
 Correction method : correction program being saved in internal RAM

■ Electrical Characteristics (Supply current)

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	14.32 MHz operation without load, VDD = 5 V		60	100	mA
	IDD2	1/1024 of 14.32 MHz operation without load VDD = 3.0 V		2	5	mA
	IDD3	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		50	100	μA
Supply current at STOP	IDSP	Stop of oscillation without load, VDD = 5 V, Ta = 55°C			10	μA
Supply current at HALT	IDHT0	14.32 MHz oscillation without load, VDD = 5 V		5	15	mA
	IDHT1	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		5	20	μA

(Ta = 25°C±2°C, VSS = 0 V)

■ Electrical Characteristics (A/D converter characteristics)

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Conversion relative error	ΔNLAD				±3	LSB
A/D Conversion Time	tAD	fosc = 14.32 MHz		8		μs
Analog Input Voltage					5	V

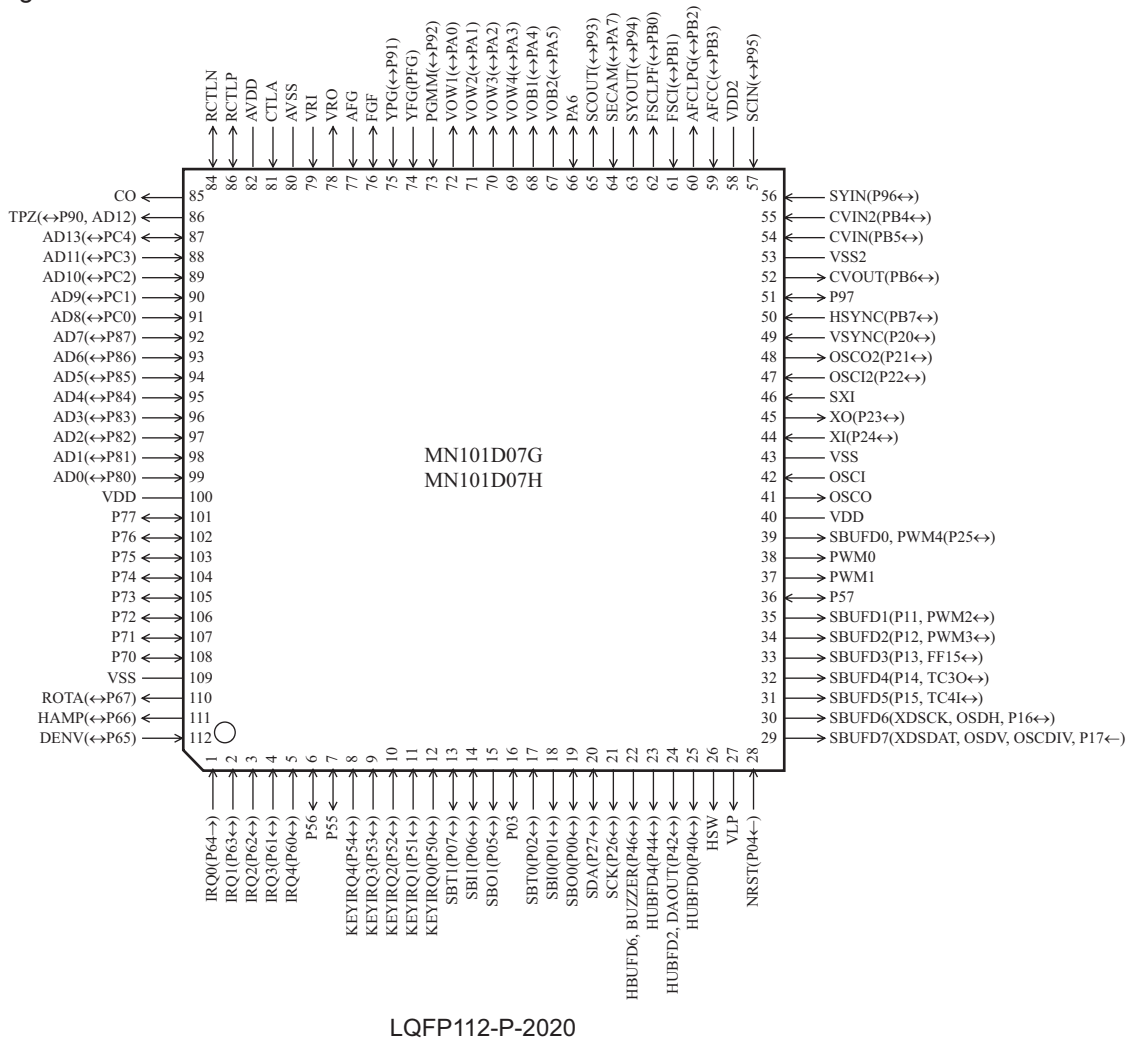
(Ta = 25°C±2°C, VDD = 5.0 V, VSS = 0 V)

■ Development tools

In-circuit Emulator

PX-ICE101C/D + PX-PRB101D07-LQFP112-P-2020-M

■ Pin Assignment



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